

SN74LVCC3245A

OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

SCAS585F – NOVEMBER 1996 – REVISED AUGUST 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

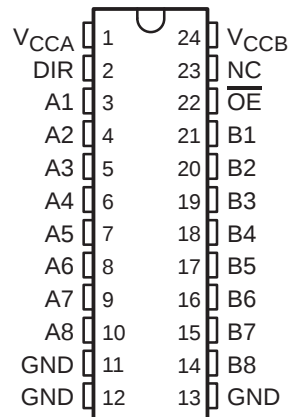
description

This 8-bit (octal) noninverting bus transceiver contains two separate supply rails. The B port is designed to track V_{CCB} , which accepts voltages from 3 V to 5.5 V, and the A port is designed to track V_{CCA} , which operates at 2.3 V to 3.6 V. This allows for translation from a 3.3-V to a 5-V system environment and vice versa, or from a 2.5-V to a 3.3-V system environment and vice versa.

The SN74LVCC3245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

The SN74LVCC3245A is characterized for operation from -40°C to 85°C .

DB, DW, OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation



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**TEXAS
INSTRUMENTS**

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SCAS585F – NOVEMBER 1996 – REVISED AUGUST 1998

The diagram shows the internal logic of the 74VHC147 decoder. It features two AND gates and two inverters. The inputs are DIR (pin 2), A1 (pin 3), and B1 (pin 21). The output of the first AND gate is connected to pin 22 (OE). The output of the second AND gate is connected to pin 21 (B1). The diagram is part of a larger circuit with other channels, indicated by the text "To Seven Other Channels" at the bottom.

Supply voltage range, V_{CCA} and V_{CCB}	−0.5 V to 6 V
Input voltage range, V_I : All A port (see Note 2)	−0.5 V to $V_{CCA} + 0.5$ V
All B port (see Note 1)	−0.5 V to $V_{CCB} + 0.5$ V
Except I/O ports (see Note 2)	−0.5 V to $V_{CCA} + 0.5$ V
Output voltage range, V_O (see Note 1): All A port	−0.5 V to $V_{CCA} + 0.5$ V
All B port	−0.5 V to $V_{CCB} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	−50 mA
Output clamp current, I_{OK} ($V_O < 0$)	−50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CCA} , V_{CCB} , or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	104°C/W
DW package	81°C/W
PW package	120°C/W
Storage temperature range, T_{Stg}	−65°C to 150°C

NOTES:

1. This value is limited to 6 V maximum.
2. This value is limited to 4.6 V maximum.
3. The package thermal impedance is calculated in accordance with JEDEC 51.

SN74LVCC3245A

OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

SCAS585F – NOVEMBER 1996 – REVISED AUGUST 1998

recommended operating conditions (see Note 4)

		V _{CCA}	V _{CCB}	MIN	NOM	MAX	UNIT
V _{CCA}	Supply voltage			2.3	3.3	3.6	V
V _{CCB}	Supply voltage			3	5	5.5	V
V _{IHA}	High-level input voltage	V _{OB} ≤ 0.1 V, V _{OB} ≥ V _{CCB} – 0.1 V	2.3 V	3 V	1.7		V
			2.7 V	3 V	2		
			3 V	3.6 V	2		
			3.6 V	5.5 V	2		
V _{IHB}	High-level input voltage	V _{OA} ≤ 0.1 V, V _{OA} ≥ V _{CCA} – 0.1 V	2.3 V	3 V	2		V
			2.7 V	3 V	2		
			3 V	3.6 V	2		
			3.6 V	5.5 V	3.85		
V _{ILA}	Low-level input voltage	V _{OB} ≤ 0.1 V, V _{OB} ≥ V _{CCB} – 0.1 V	2.3 V	3 V		0.7	V
			2.7 V	3 V		0.8	
			3 V	3.6 V		0.8	
			3.6 V	5.5 V		0.8	
V _{ILB}	Low-level input voltage	V _{OA} ≤ 0.1 V, V _{OA} ≥ V _{CCA} – 0.1 V	2.3 V	3 V		0.8	V
			2.7 V	3 V		0.8	
			3 V	3.6 V		0.8	
			3.6 V	5.5 V		1.65	
V _{IA}	Input voltage			0		V _{CCA}	V
V _{IB}	Input voltage			0		V _{CCB}	V
V _{OA}	Output voltage			0		V _{CCA}	V
V _{OB}	Output voltage			0		V _{CCB}	V
I _{OHA}	High-level output current		2.3 V	3 V		–8	mA
			2.7 V	3 V		–12	
			3.3 V	3 V		–24	
I _{OHB}	High-level output current		2.3 V	3.3 V		–12	mA
			2.7 V	3.3 V		–12	
			3.3 V	3 V		–24	
I _{OLA}	Low-level output current		2.3 V	3 V		8	mA
			2.7 V	3 V		12	
			3.3 V	3 V		24	
I _{OLB}	Low-level output current		2.3 V	3.3 V		12	mA
			2.7 V	3.3 V		12	
			3.3 V	3 V		24	
Δt/Δv	Input transition rise or fall rate			0		10	ns/V
T _A	Operating free-air temperature			–40		85	°C

NOTE 4: All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74LVCC3245A
**OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE
AND 3-STATE OUTPUTS**

SCAS585F – NOVEMBER 1996 – REVISED AUGUST 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CCA}	V _{CCB}	MIN	TYP	MAX	UNIT
V _{OHA}		I _{OH} = –100 µA	3 V	3 V	2.9	3		V
		I _{OH} = –8 mA	2.3 V	3 V	2			
		I _{OH} = –12 mA	2.7 V	3 V	2.2	2.5		
			3 V	3 V	2.4	2.8		
		I _{OH} = –24 mA	3 V	3 V	2.2	2.6		
			2.7 V	4.5 V	2	2.3		
V _{OHB}		I _{OH} = –100 µA	3 V	3 V	2.9	3		V
		I _{OH} = –12 mA	2.3 V	3 V	2.4			
			2.7 V	3 V	2.4	2.8		
		I _{OH} = –24 mA	3 V	3 V	2.2	2.6		
			2.7 V	4.5 V	3.2	4.2		
V _{OLA}		I _{OL} = 100 µA	3 V	3 V			0.1	V
		I _{OL} = 8 mA	2.3 V	3 V			0.6	
		I _{OL} = 12 mA	2.7 V	3 V		0.1	0.5	
		I _{OL} = 24 mA	3 V	3 V		0.2	0.5	
			2.7 V	4.5 V		0.2	0.5	
V _{OLB}		I _{OL} = 100 µA	3 V	3 V			0.1	V
		I _{OL} = 12 mA	2.3 V	3 V			0.4	
		I _{OL} = 24 mA	3 V	3 V		0.2	0.5	
				4.5 V		0.2	0.5	
I _I	Control inputs	V _I = V _{CCA} or GND	3.6 V	3.6 V	±0.1	±1		µA
				5.5 V	±0.1	±1		
I _{OZ} [†]	A or B ports	V _O = V _{CCA/B} or GND, V _I = V _{IL} or V _{IH}	3.6 V	3.6 V	±0.5	±5		µA
I _{CCA}	B to A	A port = V _{CCA} or GND, I _O = 0	3.6 V	Open		5	50	µA
		B port = V _{CCB} or GND, I _O = 0	3.6 V	3.6 V		5	50	
				5.5 V		5	50	
I _{CCB}	A to B	A port = V _{CCA} or GND, I _O = 0	3.6 V	3.6 V		5	50	µA
				5.5 V		8	80	
ΔI _{CCA} [‡]	A port	V _I = V _{CCA} – 0.6 V, Other inputs at V _{CCA} or GND, OE at GND and DIR at V _{CCA}	3.6 V	3.6 V		0.35	0.5	mA
	$\overline{\text{OE}}$	V _I = V _{CCA} – 0.6 V, Other inputs at V _{CCA} or GND, DIR at V _{CCA}	3.6 V	3.6 V		0.35	0.5	
	DIR	V _I = V _{CCA} – 0.6 V, Other inputs at V _{CCA} or GND, OE at GND	3.6 V	3.6 V		0.35	0.5	
ΔI _{CCB} [‡]	B port	V _I = V _{CCB} – 2.1 V, Other inputs at V _{CCB} or GND, OE at GND and DIR at GND	3.6 V	5.5 V		1	1.5	mA
C _i	Control inputs	V _I = V _{CCA} or GND	Open	Open		4		pF
C _{io}	A or B ports	V _O = V _{CCA/B} or GND	3.3 V	5 V		18.5		pF
C _{pd}	A to B	Outputs enabled	3.3 V	5 V		38		pF
	B to A	Outputs enabled	3.3 V	5 V		36.5		

[†] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[‡] This is the increase in supply current for each input that is at one of the specified voltage levels rather than 0 V or the associated V_{CC}.

SN74LVCC3245A

OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

SCAS585F – NOVEMBER 1996 – REVISED AUGUST 1998

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$, $V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}$, $V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}$, $V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHL}	A	B	1	9.4	1	6	1	7.1	ns
t_{PLH}			1	9.1	1	5.3	1	7.2	
t_{PHL}	B	A	1	11.2	1	5.8	1	6.4	ns
t_{PLH}			1	9.9	1	7	1	7.6	
t_{PZL}	$\overline{OE}$	A	1	14.5	1	9.2	1	9.7	ns
t_{PZH}			1	12.9	1	9.5	1	9.5	
t_{PZL}	$\overline{OE}$	B	1	13	1	8.1	1	9.2	ns
t_{PZH}			1	12.8	1	8.4	1	9.9	
t_{PLZ}	$\overline{OE}$	A	1	7.1	1	5.5	1	6.6	ns
t_{PHZ}			1	6.9	1	7.8	1	6.9	
t_{PLZ}	$\overline{OE}$	B	1	8.8	1	7.3	1	7.5	ns
t_{PHZ}			1	8.9	1	7	1	7.9	

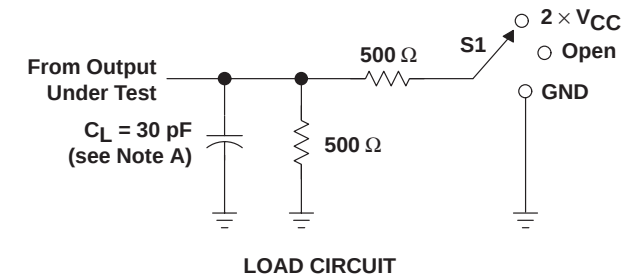
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OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

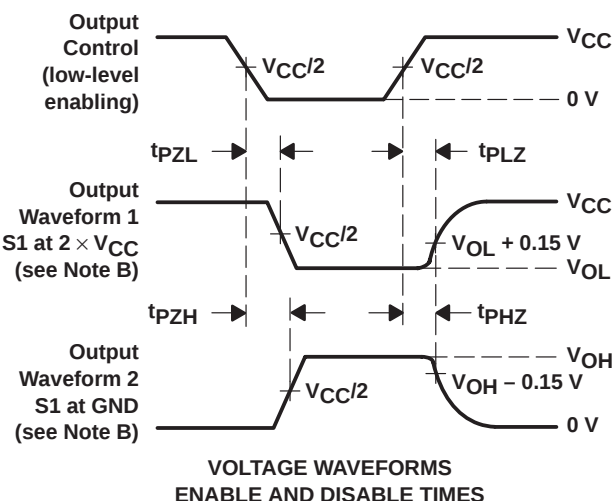
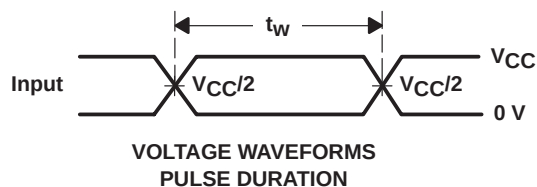
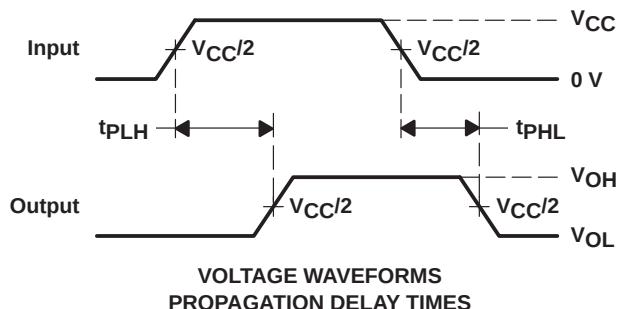
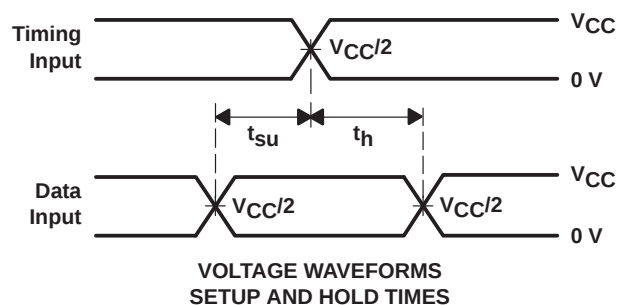
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PARAMETER MEASUREMENT INFORMATION FOR A PORT

$$V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V AND } V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PHZ}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

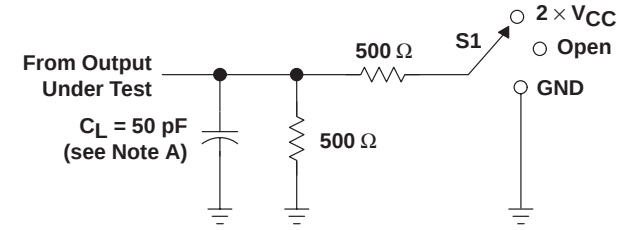
SN74LVCC3245A

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SCAS585F – NOVEMBER 1996 – REVISED AUGUST 1998

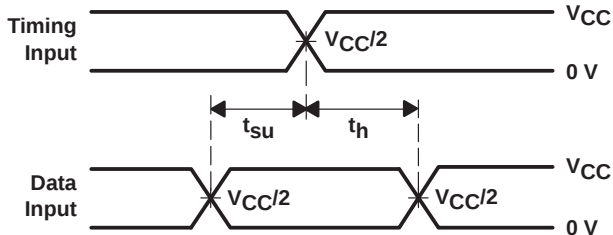
PARAMETER MEASUREMENT INFORMATION FOR B PORT

$$V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V AND } V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$$

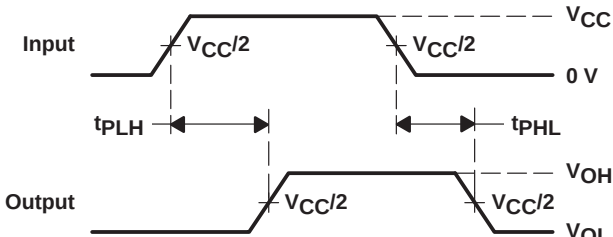


LOAD CIRCUIT

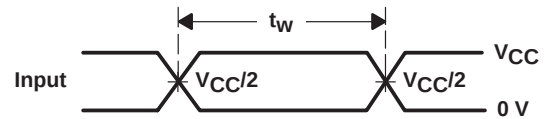
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PHZ}	GND



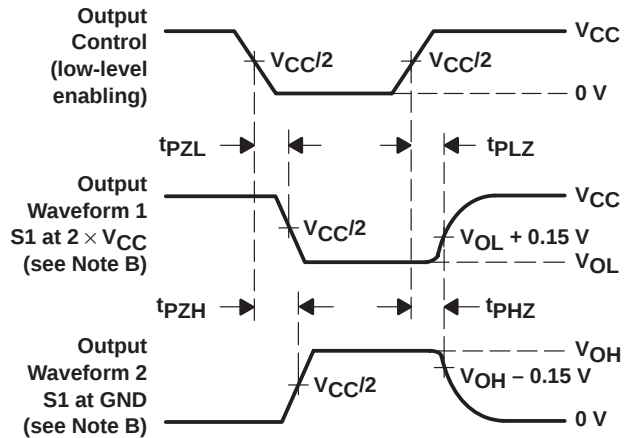
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

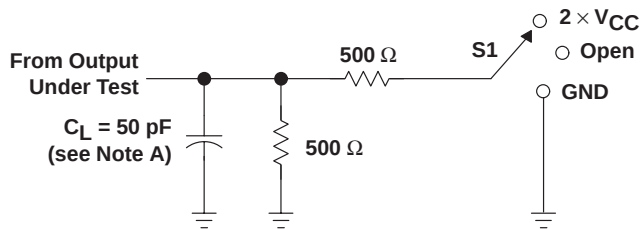
SN74LVCC3245A

OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

SCAS585F – NOVEMBER 1996 – REVISED AUGUST 1998

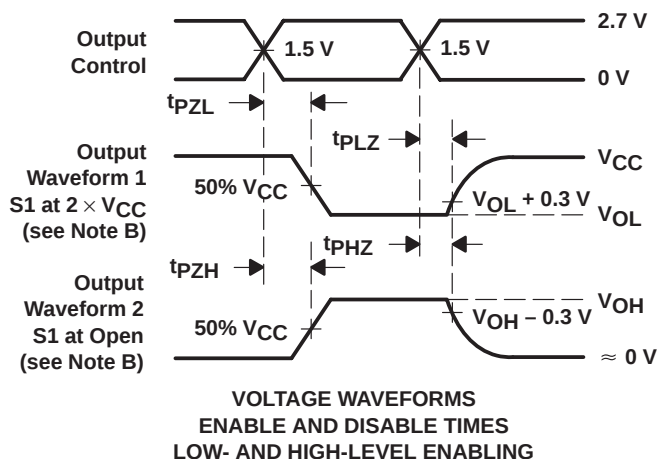
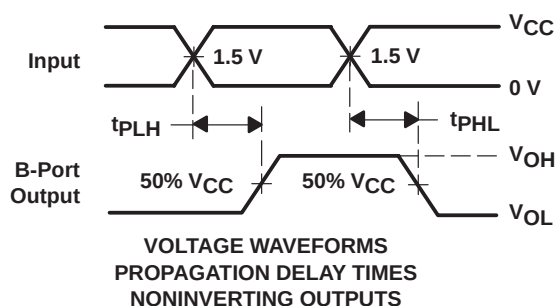
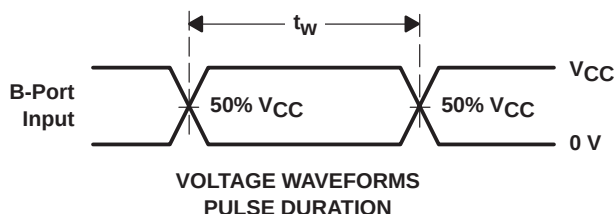
PARAMETER MEASUREMENT INFORMATION FOR B PORT

$V_{CCA} = 3.6 \text{ V}$ AND $V_{CCB} = 5.5 \text{ V}$



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

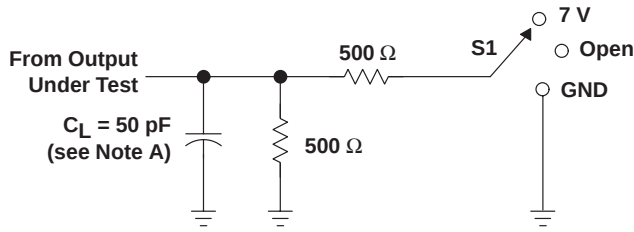
Figure 3. Load Circuit and Voltage Waveforms

SN74LVCC3245A

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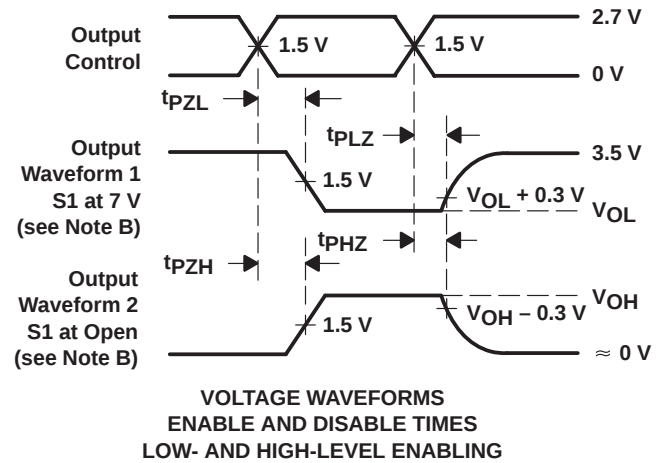
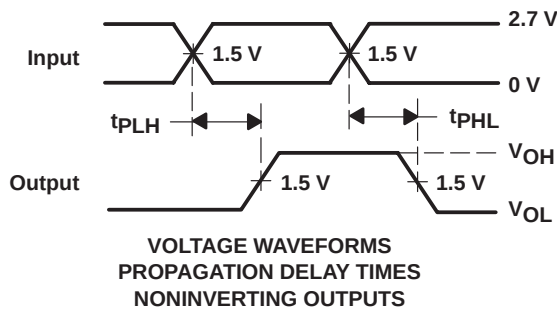
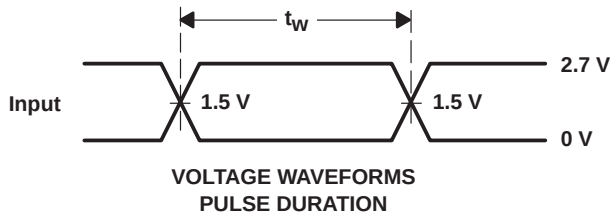
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PARAMETER MEASUREMENT INFORMATION FOR A AND B PORT V_{CCA} AND $V_{CCB} = 3.6\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 4. Load Circuit and Voltage Waveforms

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