



CYPRESS **PRELIMINARY**

CYNSE20512

CYNSE20256

Ayama™ 20000 Network Search Engine Family Data Sheet

Features

- Fast search rates
 - Up to 266 million searches per second (MSPS) in 72/144-bit configuration using MultiSearch™
 - Up to 133 MSPS in 32/288-bit configuration
 - Up to 66.5 MSPS in 576-bit configuration
- High packet processor transfer efficiency on the LA-1 Interface
 - 32-bit searches
 - Searches that reuse previous search keys using Key Capture™
 - Interrupt-driven Result Available signal saves polling cycles for result retrieval
- Mini-Key™ feature reduces power consumption by enabling only relevant blocks during a search
- Associated Data Management enables efficient SRAM management
- Ability to search two tables in a single clock cycle using MultiSearch
- Learn command simplifies data plane updates
- Ease of table management
 - Soft Priority™, assignable per sub-block
 - Mini-Key assignable per block
 - Cynapse™ APIs facilitate table management
- Aging of up to 256k entries using AgeAssist™
 - Age up to four independent tables
 - Single or double-buffered tables
- Atomic Command enables uninterrupted execution for a sequence of commands
- Error Management
 - Parity per interface
 - Core parity for data and mask arrays
 - Maskable error interrupt signal to the packet processor
- Cascadable for storage expansion with external NSEs using FastLink Interface
 - Logically expandable to store up to 25 million entries
 - Supports Ayama™ 10000 and/or Sahasra™ 50000 NSEs
- NPF-compatible Look-Aside (LA-1) Interface
 - One or two LA-1 ports
 - Support for 128 contexts per LA-1 port
- QDR-II up to 250 MHz, Burst-of-2 and Burst-of-4
- Convenient “Clamshellable” pinout for ease of board design
- No Bus Latency™ (NoBL™) SRAM Interface
 - 1.5V HSTL or 1.8V/2.5V LVCMOS I/Os support up to 200 MHz
- FastLink Interface
 - 1.5V HSTL I/Os support up to 266 MHz
 - 1.8V/2.5V LVCMOS I/Os support up to 200 MHz
- Configurable internal NSE table sizes
 - 512k entries in 36-bit configuration
 - 256k entries in 72-bit configuration
 - 128k entries in 144-bit configuration
 - 64k entries in 288-bit configuration
 - 32k entries in 576-bit configuration
- IEEE 1149.1 JTAG test access port
- 1.2V Core supply
- 1152-ball 35mm x 35mm FBGA package

Functional Description

The high-speed Ayama 20000 family of NSEs can be deployed in a variety of networking and communications applications. The performance and features of this family make it attractive in applications such as enterprise LAN switches, routing equipment, and security applications. The Ayama 20000 family of high-speed search engines are capable of supporting network data rates in excess of 10 Gbps.

The Ayama 20000 network search engine (NSE) provides a seamless connection to commercial packet processors via the industry-standard Look Aside (LA-1) Interface. The Ayama 20000 consists of control logic, which processes the commands, and a full Ternary Content-Addressable Memory (TCAM) array, which stores the databases searched by the control logic. *Figure 1* shows a block diagram of the Ayama 20000. The Ayama 20000 family includes densities of 18-Mbit (512k entries) and 9-Mbit (256k entries).

Using its two LA-1 ports, the Ayama 20000 NSE can interface with one or two packet processors. The processor issues commands and the Ayama 20000 returns the results of execution via this interface. One port may be connected to an ingress packet processor and the other to an egress packet processor. Both packet processors can perform searches on the same databases, eliminating the need for redundant memories or NSEs.

This family is designed to be scalable to support large databases. Through the FastLink Interface, the Ayama 20000 can access both the Ayama 10000 and the Sahasra 50000 NSEs.

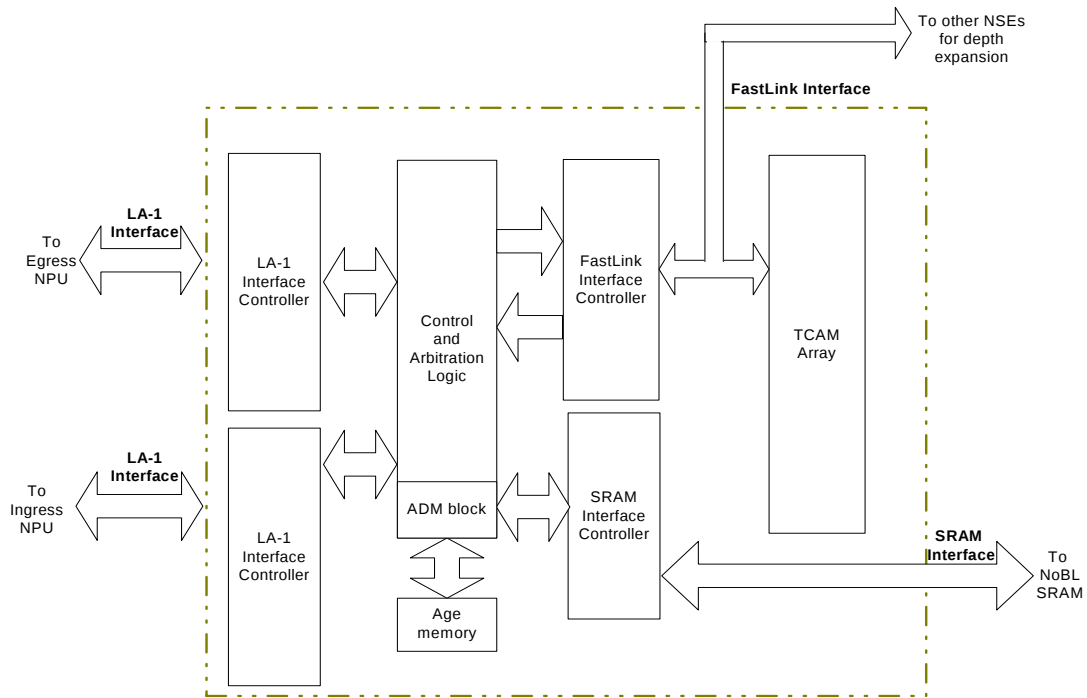


Figure 1. Ayama 20000 Block Diagram

The Ayama 20000 can optionally perform associated data lookups for the packet processor by accessing directly attached external SRAM. The Ayama 20000 contains logic which enables efficient packing of entries in the associated SRAM(s).

Figure 2 shows the use of Ayama 20000 in a typical search subsystem.

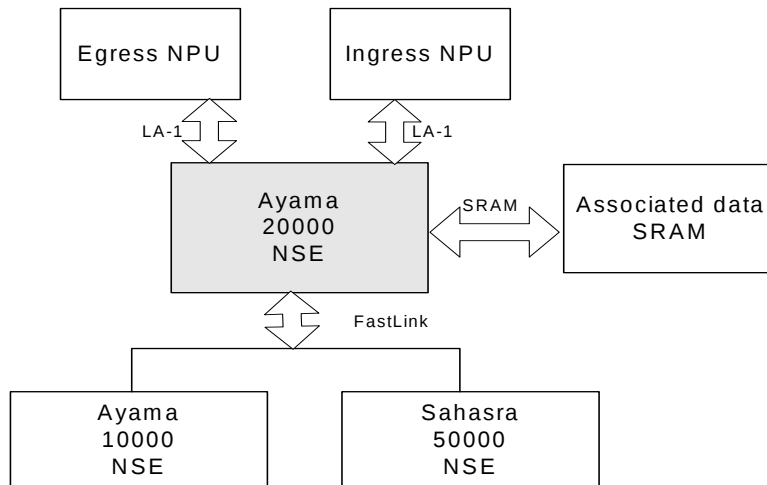


Figure 2. Ayama 20000 Linecard Application

Signal Descriptions

Table 1. Ayama 20000 Signal Descriptions

Signal Name	I/O Type, supply ^[1]	Signal Type ^[2]	Description
Clocks and Reset			
CLK	I, VDDQ_A	LVC MOS or HSTL	Master Clock. Master clock is used to generate device system clock. It is used to capture and present data on the FastLink interface relative to its rising edge when configured for single data rate (SDR) clocking, or both rising and falling edges when configured for double data rate (DDR) clocking.
CLK_MODE	I, VDDQ_A	LVC MOS or HSTL	Clock Mode. CLK_MODE selects if the master clock presented to the CLK input is an SDR or DDR clock. When LOW, SDR mode is selected and the maximum clock input frequency is 266 MHz. When HIGH, DDR mode is selected, and the maximum clock input frequency is 133 MHz.
PHS_OUT_L	O, VDDQ_A	LVC MOS or HSTL I/II	Phase Output. PHS_OUT_L outputs a signal used to set the phase relationship for cascaded devices (this signal connects to the PHS_L input of Ayama 10000 and Sahasra 50000). When operating with cascaded devices and SDR clocking, this output is used to identify the active phase of the transfer cycle. When operated in DDR clocking, this signal is constant LOW.
RST_L	I, VDDQ_A	LVC MOS or HSTL	Reset. Asserting RST_L LOW initializes the device to the default state. Refer to Reset and Power-on Sequence Requirements on page 15 for more details.
EINTR	O	LVC MOS or HSTL I/II	Error Interrupt. When EINTR is asserted HIGH, one or more errors have occurred. Possible errors include LA-1, FastLink, and SRAM interface parity errors as well as TCAM core parity errors and context processing errors.
LA-1 Interface			
K0, K1	I, VDDQ_Q	HSTL	K Clocks. K clocks of LA-1 ports 0 and 1, respectively. The rising edge of each K clock is used to latch address, data, and control inputs. The frequency of each LA-1 port is independently controlled and the K0 and K1 clocks do not need to run at the same frequency.
K0#, K1#	I, VDDQ_Q	HSTL	Complement K Clocks. K# clocks of LA-1 ports 0 and 1, respectively. The rising edge of each complement K clock is used to latch input data. It is nominally 180 degrees out of phase with its associated K clock.
C0, C1	I, VDDQ_Q	HSTL	C Clocks. C clocks of LA-1 ports 0 and 1, respectively. The rising edge of each C clock is used as the timing reference for the most significant output bits [31:16]. C and C# clocks must be provided; these pins must not be tied HIGH.
C0#, C1#	I, VDDQ_Q	HSTL	Complement C Clocks. C# of LA-1 ports 0 and 1, respectively. The rising edge of each complement C clock is used as the timing reference for the least significant output bits [15:0]. It should be nominally 180 degrees out of phase with its associated C-clock. C and C# clocks must be provided; these pins must not be tied HIGH.
CQ0, CQ1	O, VDDQ_Q	HSTL I/II	Echo Clocks. These are designed to track changes in output driver delays due to variance in die temperature and supply voltage. Echo clocks CQn track Cn. These clocks are active even if one or both LA-1 ports are deselected.
CQ0#, CQ1#	O, VDDQ_Q	HSTL I/II	Complement Echo C Clocks. These are designed to track changes in output driver delays due to variance in die temperature and supply voltage. The echo clocks are designed to transition with the data output drivers. The echo clock CQn# tracks Cn#. These clocks are active even if one or both LA-1 ports are deselected.
R0#, R1#	I, VDDQ_Q	HSTL	Read Select. Active LOW, initiate read cycles.
W0#, W1#	I, VDDQ_Q	HSTL	Write Select. Active LOW, initiate write cycles.
A0[21:0], A1[21:0]	I, VDDQ_Q	HSTL	Address Buses. Address buses for LA-1 ports 0 and 1, respectively. The Ayama 20000 defines a 32-bit word address bus. Care must be taken when connecting the address bus as the LA-1 specification and some packet processors define A[21:2], where A[2] is the LSB word address input corresponding to Ayama 2000's A[0] input. Note: A[19:0] must be driven while A[21:20] are reserved for future expansion.

Notes:

1. I = input only, O = output only, I/O = input or output, T = three-state output
2. Signaling type is selected by (a) NSESEL for clocks, reset, and FastLink Interface; (b) SRAMSEL for SRAM Interface

Table 1. Ayama 20000 Signal Descriptions (continued)

Signal Name	I/O Type, supply ^[1]	Signal Type ^[2]	Description
E0[1:0], E1[1:0]	I, VDDQ_Q	HSTL	Port Enable. Port enable signals for LA-1 ports 0 and 1, respectively. When En[1:0] of an LA-1 port match the values of EPn[1:0] for that LA-1 port, it is activated and participates in any associated data transfers.
EP0[1:0], EP1[1:0]	I, VDDQ_Q	HSTL	Port Enable Programming. Port enable programming signals for LA-1 ports 0 and 1, respectively. En[1:0] must match EPn[1:0] in order for a particular LA-1 port to be activated.
BW0#[1:0], BW1#[1:0]	I, VDDQ_Q	HSTL	Byte Write Enable. Byte write enable for LA-1 ports 0 and 1, respectively. The Ayama 20000 does not support individual byte writes, and in Burst-of-2 mode, both byte-write inputs should be driven LOW. In Burst-of-4 mode, these signals define whether the first, second, or both words are written. In this mode, the byte writes must both be LOW for a cycle to allow the word to be written on that cycle, or they must both be HIGH for a cycle to prevent a write occurring on that cycle. Other combinations are not valid.
D0[15:0], D1[15:0]	I, VDDQ_Q	HSTL	Data Input Buses. Synchronous data inputs from LA-1 ports 0 and 1, respectively. These buses carry the data for all write accesses.
DP0[1:0], DP1[1:0]	I, VDDQ_Q	HSTL	Data Parity Inputs. Synchronous even-parity inputs from LA-1 ports 0 and 1, respectively. DPn[0] is the XOR of Dn[7:0], and DPn[1] is the XOR of Dn[15:8]. Care must be taken when connecting the Dn and DPn signals as for some processors the parity bits appear on Dn[8] and Dn[17].
Q0[15:0], Q1[15:0]	O, VDDQ_Q	HSTL I/II	Data Output Buses. Synchronous data outputs to LA-1 ports 0 and 1, respectively. These buses carry the data for packet processor read accesses. The CQ and CQ# clocks are aligned with this data output.
QP0[1:0], QP1[1:0]	O, VDDQ_Q	HSTL I/II	Data Parity Outputs. Synchronous even-parity outputs to LA-1 ports 0 and 1, respectively. QPn[0] is the XOR of Qn[7:0], and QPn[1] is the XOR of Qn[15:8]. Care must be taken when connecting the Qn and QPn signals as for some processors the parity bits are expected on Qn[8] and Qn[17].
DOFF0_L, DOFF1_L	I, VDDQ_Q	HSTL	DLL Off. These inputs are used to control the internal DLL on LA-1 ports 0 and 1, respectively. These should be HIGH for normal operation to enable the DLL.
RA0, RA1	O, VDDQ_Q	HSTL I/II	Result Available Interrupts. These outputs indicate that context results are ready to be read back from the result FIFOs.
QDR0REF0 QDR0REF1 QDR1REF0 QDR1REF1	I	Analog input	LA-1 Reference Voltages. Must be externally driven within the allowed reference voltage range for HSTL I/II (nominally $V_{DDQ_Q}/2$). The bias point can be adjusted to improve system noise margin.
IFC0[1:0], IFC1[1:0]	I, VDDQ_Q	HSTL	LA-1 Interface Configurations. These inputs configure the associated LA-1 Interface for Burst-of-2 or Burst-of-4.
FastLink Interface			
DQ and Command Bus			
DQ[71:0]	I/O, VDDQ_A	LVC MOS or HSTL I/II	Address/Data Bus. DQ[71:0] carry the read and write address and data during register, data, and mask-array operations. It carries the search key during search operations.
PAR[1:0]	I/O, VDDQ_A	LVC MOS or HSTL I/II	DQ Parity. PAR[1:0] carry the even-parity information for the bidirectional DQ Bus. These signals are driven on the FastLink Interface when the DQ and Command Bus are written, and read from the FastLink Interface on all NSE read operations. PAR[0] carries parity information for all even numbered DQ bits (i.e., 70, 68,...,0). PAR[1] carries parity information for all odd numbered DQ bits (i.e., 71, 69,...,1).
CMD[10:0]	O, VDDQ_A	LVC MOS or HSTL I/II	Command Bus. This carries the command and associated parameters to cascaded Type-1 and Type-2 devices.
CMDV	O, VDDQ_A	LVC MOS or HSTL I/II	Command Valid. When HIGH, CMDV indicates to any Type-1 cascaded devices that a valid command is present on the command bus.

Table 1. Ayama 20000 Signal Descriptions (continued)

Signal Name	I/O Type, supply ^[1]	Signal Type ^[2]	Description
SCMDV	O, VDDQ_A	LVC MOS or HSTL I/II	Secondary Command Valid. When HIGH, SCMDV indicates to any Type-2 cascaded devices that a valid command is present on the command bus.
ACK ^[3]	I/O, VDDQ_A	LVC MOS or HSTL I/II	Read Acknowledge. When HIGH, ACK indicates that valid data is available on the DQ Bus during NSE register, data, and mask-array read operations.
PARERR_L ^[4]	I/O Open Drain, VDDQ_A	LVC MOS or HSTL I/II	Parity Error. PARERR_L is asserted LOW by a Type-1 NSE when there is a core parity error or bus parity error detected by a device on the NSE Primary Result Bus.
SPARERR_L ^[4]	I Open Drain, VDDQ_A	LVC MOS or HSTL	Secondary Parity Error. SPARERR_L is asserted LOW by a Type-2 NSE when there is a core parity error or bus parity error detected by a device on the NSE Secondary Result Bus.
NSESEL	I, VDDQ_A	LVC MOS	NSE I/O Select. When NSESEL is set to V _{DDQ_A} , all FastLink signals comply to LVC MOS signalling standards. When set to V _{SS} , these signals comply to HSTL signalling standards.
NSEREF0 NSEREF1 NSEREF2 NSEREF3 NSEREF4	I	Analog Input	NSE Reference Voltages. When NSESEL is set to V _{SS} , these signals, must be externally driven within the reference voltage range for HSTL, nominally V _{DDQ_A} /2. If NSESEL is configured for LVC MOS operation they may be left floating, or connected to any voltage between V _{SS} and V _{DDQ_A} .
HS_PWRSAVE	O, VDDQ_A	LVC MOS or HSTL I/II	High Speed Power Save. Leave floating for operation below 200 MHz. For operation above 200 MHz this pin can be left floating or, for power savings this can be tied to HIGH_SPEEDI_L through an inverter.
HIGH_SPEEDI_L	I, VDDQ_A	LVC MOS or HSTL	High Speed Enable Input. For operation at or below 200 MHz, this pin should be tied HIGH. For operation above 200 MHz this pin can be tied LOW, or for additional power savings can be tied to HS_PWRSAVE through an inverter.
<i>NSE Primary Result Bus</i>			
SSF	I/O, VDDQ_A	LVC MOS or HSTL I/II	Search Successful Flag. When HIGH, SSF indicates that a Type-1 device is the global winner in a Search operation. SSF is valid whenever SSV is HIGH.
SSV ^[3]	I/O, VDDQ_A	LVC MOS or HSTL I/II	Search Successful Flag Valid. When HIGH, SSV indicates a valid SSF and FULL_OUT value.
FULL_IN	I, VDDQ_A	LVC MOS or HSTL	Full Flag Input. This signal tells the Ayama 20000 device that there are no free entries within the TCAM array. When cascaded with Type-1 devices, the FULL output of the last device in the cascade must be connected to FULL_IN of the Ayama 20000. If the Ayama 20000 is the last device or stand-alone, FULL_OUT of the Ayama 20000 should be connected to FULL_IN.
FULL_OUT	O, VDDQ_A	LVC MOS or HSTL I/II	Full Flag Output. When HIGH, FULL_OUT indicates that there are no free entries in the internal TCAM array (for the blocks selected by Mini-Key). FULL_OUT is valid whenever SSV is HIGH.
INDEX[23:0]	I/O, VDDQ_A	LVC MOS or HSTL	Search Index Bus. This bus carries the successful search index of the winning Type-1 device on the FastLink interface.
<i>NSE Secondary Result Bus</i>			
SSSF	I, VDDQ_A	LVC MOS or HSTL	Secondary Search Successful Flag. When HIGH, SSSF indicates that a Type-2 NSE is the global winner in a search operation.
SSSV ^[3]	I, VDDQ_A	LVC MOS or HSTL	Secondary Search Successful Flag Valid. When HIGH, SSSV indicates a valid SSSF value.

Notes:

- Requires a weak external bias LOW. A 70Ω pull-down and 165Ω pull-up resistor combination is recommended.
- This signal is open drain and requires a weak external bias HIGH. A 70Ω pull-up and 165Ω pull-down resistor combination is recommended.

Table 1. Ayama 20000 Signal Descriptions (continued)

Signal Name	I/O Type, supply ^[1]	Signal Type ^[2]	Description
SINDEX[23:0]	I, VDDQ_A	LVC MOS or HSTL	Secondary Search Index Bus. This bus carries the search index of the winning Type-2 device on the cascade bus.
<i>Cascade Bus (Type-1 devices only)</i>			
LHI[6:0]	I, VDDQ_A	LVC MOS or HSTL	Local Hit In/Local Hit In Bank 0. These inputs indicate whether there is a hit in the upstream devices within the same block. When MultiSearch is enabled, the LHI[6:0] signals indicate a local hit in bank 0. When there are no cascaded Type-1 devices, these inputs should all be tied LOW. Refer to the Ayama 20000 Device Manual for further details regarding cascading.
LHO[1:0]	O, VDDQ_A	LVC MOS or HSTL I/II	Local Hit Out/ Local Hit Out Bank 0. LHO[0] and LHO[1] are logically the same signal. They can each be used to drive up to four devices. These signals are connected to the LHI inputs on downstream cascaded devices. When MultiSearch is enabled, LHO[1:0] indicate a local hit in bank 0.
BHI[2:0]	I, VDDQ_A	LVC MOS or HSTL	Block Hit In. These signals indicate if there is a hit in the upstream/previous logical blocks in a cascade. When there are no cascaded Type-1 devices, these inputs must all be tied LOW. Refer to the Ayama 20000 Device Manual for further details regarding cascading.
BHO[2:0]	O, VDDQ_A	LVC MOS or HSTL I/II	Block Hit Out. All BHO signals perform the same logical function. BHO signals are connected to the BHI inputs of downstream cascaded Type-1 blocks.
FULI[6:0]	I, VDDQ_A	LVC MOS or HSTL	Full In/Local Hit In Bank 1. During a search operation, these inputs indicate whether an upstream device has a free entry (within the blocks selected by the Mini-Key). When MultiSearch is activated, the FULI[6:0] signals replicate the function of LHI[6:0] for bank 1. When there are no cascaded Type-1 devices, these inputs must all be tied HIGH. Refer to the Ayama 20000 Device Manual for further details regarding cascading.
FULO[1:0]	O, VDDQ_A	LVC MOS or HSTL I/II	Full Out/Local Hit Out Bank 1. FULO[0] and FULO[1] are logically the same signal. FULO[1:0] connect to the FULI inputs on downstream cascaded devices. When MultiSearch is activated, the FULO[1:0] signals replicate the function of LHO[1:0] for bank 1.
SRAM Interface			
AD_SADR[23:0]	O, VDDQ_S	LVC MOS or HSTL I/II	SRAM Address Bus. AD_SADR[23:0] is the address bus for the off-chip associated data SRAMs.
AD_SDATA[31:0]	I/O, VDDQ_S	LVC MOS or HSTL I/II	SRAM Data Bus. AD_SDATA [31:0] is the data bus to the off-chip associated data SRAMs.
AD_SDATAP[3:0]	I/O, VDDQ_S	LVC MOS or HSTL I/II	SRAM Data Parity Bus. AD_SDATAP[3:0] carry even parity information per data byte transferred between the device and associated SRAMs. AD_SDATAP[3] carries parity information for the most significant byte and AD_SDATAP[0] carries parity information for the least significant byte.
AD_CE_L	O, VDDQ_S	LVC MOS or HSTL I/II	SRAM Chip Enable. Active LOW. AD_CE_L is the chip enable signal for associated SRAMs.
AD_WE_L	O, VDDQ_S	LVC MOS or HSTL I/II	SRAM Write Enable. Active LOW. AD_WE_L is the write enable signal for associated SRAMs.
SRAMSEL	I, VDDQ_S	LVC MOS	SRAM I/O Select. When SRAMSEL is driven to V _{DDQ_S} , all SRAM interface signals comply to LVC MOS signalling standards. When driven to V _{SS} , these signals comply to HSTL signalling standards.
SRAMREF	I	Analog input	SRAM Reference Voltages. When SRAMSEL is set to V _{SS} , this signal must be externally driven within the reference voltage range for HSTL (nominally V _{DDQ_S} /2). Otherwise, it may be left floating, or connected to any voltage between V _{SS} and V _{DDQ_S} .

Table 1. Ayama 20000 Signal Descriptions (continued)

Signal Name	I/O Type, supply ^[1]	Signal Type ^[2]	Description
Configuration			
ID[4:0]	I, VDDQ_A	LVC MOS and HSTL	Device Identification. Used to select devices configured for cascaded operations. This feature is only supported for cascaded Type-1 devices. The binary-encoded device identification for a depth-cascaded system starts at "00000" and goes up to "11110." The number "11111" is reserved as the broadcast address which selects all NSEs attached to a cascaded bus.
Reserved Signals			
RSVD	NC	NC	Reserved signal. For internal use only. Do not connect any signal/trace to these signals.
TERM	I/O, VDDQ_A	LVC MOS or HSTL I/II	Terminated signal. For internal use only. If NSESEL is V _{ss} , this signal must be terminated per the HSTL standard. If NSESEL is V _{DDQ_A} , this signal should be left floating.
TEST_PB	I, VDDQ_A	LVC MOS and HSTL	TEST. This pin must be LOW for normal operation. This pin must be driven HIGH during JTAG testing.
JTAG Test Access Port			
TDI	I, VDDQ_J	LVC MOS	Test Data Input. JTAG access port test data in. Weak pull-up.
TCK	I, VDDQ_J	LVC MOS	Test Clock. JTAG access port test clock.
TDO	T, VDDQ_J	LVC MOS	Test Data Output. JTAG access port test data out.
TMS	I, VDDQ_J	LVC MOS	Test Mode Select. JTAG access port test mode select. Weak pull-up.
TRST*	I, VDDQ_J	LVC MOS	Test Reset. JTAG access port reset. Weak pull-up.
Power Domains			
V _{SS}		Ground	Common ground for all signals and power domains except PLL supply.
V _{SS_PLL}		Ground	Ground for PLL Supply
V _{DD}		Power	1.2V Core power
V _{DD_PLL}		Power	1.2V PLL Supply
V _{DDQ_Q}		Power	1.5V (HSTL) for LA-1 Interfaces and related signals
V _{DDQ_A}		Power	1.5V (HSTL), 1.8V (LVC MOS), or 2.5V (LVC MOS) power for NSE and FastLink Interface and related signals
V _{DDQ_S}		Power	1.5V (HSTL), 1.8V (LVC MOS), or 2.5V (LVC MOS) power for SRAM Interface and related signals
V _{DDQ_J}		Power	1.8 or 2.5V (LVC MOS) power. This domain provides power to the JTAG I/O. Signals affected are TDO, TDI, TCK, TRST*, and TMS.

Ayama 20000 Interfaces

The Ayama 20000 has three interfaces:

- LA-1
- FastLink
- SRAM

LA-1 Interface

The Ayama 20000 connects directly to commercial packet processors via the Network Processing Forum (NPF) compatible LA-1 interfaces. LA-1 interfaces support

- Concurrent read and write operations

- Unidirectional read and write interfaces
- Single address bus
- 32-bit data transfers, plus four bits of even-byte parity per read or write
- Burst-of-2 and Burst-of-4 transactions

The LA-1 ports can run at different frequencies, as set by their respective K clocks.

LA-1 Physical Interface

Each LA-1 port includes

- Six clock pins (K, K#, C, C#, CQ, CQ#)

- 20-bit address bus (A[19:0])
- 16-bit data bus (D[15:0]) and 2-bit parity bus (DP[1:0]) for write operations (input to the Ayama 20000 NSE)
- 16-bit data bus (Q[15:0]) and 2-bit parity bus (QP[1:0]) for read operations (output from the Ayama 20000 NSE)
- Active-LOW read and write control signals, R# and W#
- Port Enables E[1:0] and EP[1:0]
- Byte-write enable BW#[1:0]

These are shown in *Figure 3*.

In addition to the transactions and speeds documented in the LA-1 implementation agreement, the Ayama 20000 supports QDR-II with Burst-of-2 or Burst-of-4 up to 250 MHz

The LA-1 interface uses HSTL I/O signalling.

LA-1 Logical Interface.

The Ayama 20000 supports up to 128 contexts on each of its two LA-1 ports. Each LA-1 port is independently controlled and can operate at different frequencies. A context is accessed by encoding its number on a subset of the LA-1 port's address bus. Each context has a data FIFO, a command FIFO, and a result FIFO. The user encodes the command in the address and places related data on the data bus. Results of execution are read from the result FIFO. *Figure 4* contains a logical view of an LA-1 context.

The Ayama 20000 supports queuing of instructions using the command and data FIFOs within each context. Because different commands require different numbers of data quadlets, the total number of outstanding commands that can be stored on the transmit side is limited by the smaller of the number of commands (16 or less) or the number of data quadlets associated with the commands (32 or less). Similarly,

the number of results that can be stored in the result FIFO is limited by the number of quadlets returned per command.

When a context receives a complete atomic command sequence, that context is lined up for execution. Context scheduling occurs per the following rules:

- Round-robin between alternate LA-1 ports
- Order of arrival within the same LA-1 port.

The packet processor reads results from the result FIFO, which can store 16 quadlets per context. The number of results this corresponds to depends on whether the device is programmed to return the index and/or associated data.

Should an empty FIFO be read, an Empty FIFO Indicator (EFI) is returned.

Result Available Notification

A Result Available signal (RA), four Result Available Vectors (RAV), and a Result Available Vector Aggregate (RAVA) are available for each LA-1 interface. The RA signal indicates that a result is available from one of the 128 contexts. The four 32-bit Result Available Vectors may be read to determine which context has a result. The RAVA indicates which of the four RAVs to read.

FastLink Interface

The purpose of the FastLink Interface is to connect multiple NSEs to the Ayama 20000. In addition to providing extra storage and searching capabilities, the connection of external NSEs allows packet processors to perform searches on larger tables via the same LA-1 Interface. The Ayama 20000 can support various table widths across cascaded devices of the same type.

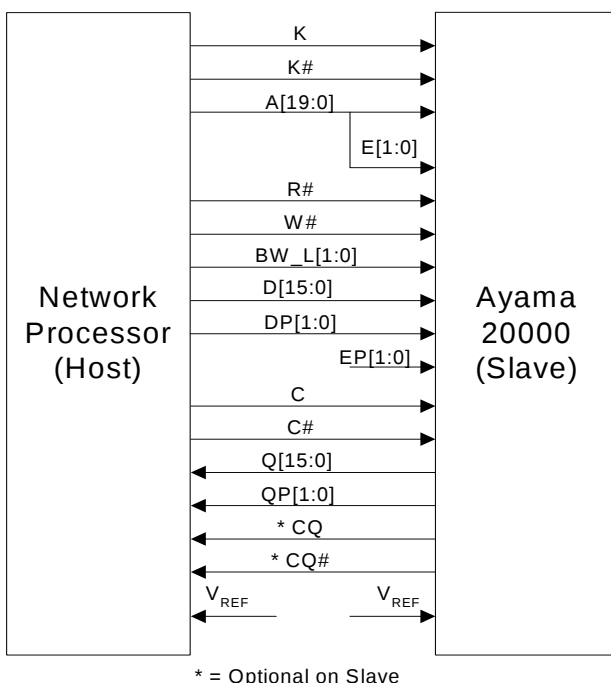


Figure 3. LA-1 Interface Signals

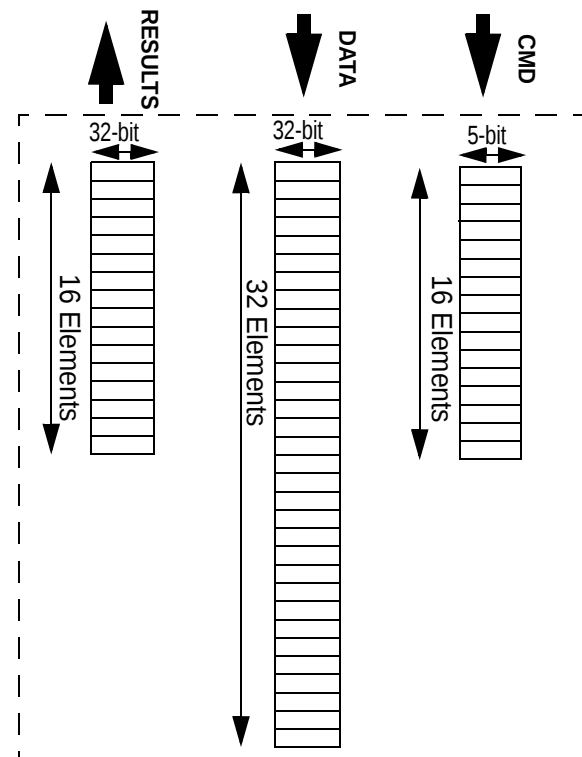


Figure 4. Logical View of a Context

FastLink Physical Interface

The FastLink Interface includes

- DQ and CMD buses
- INDEX and SINDEX buses

The DQ and CMD busses carry the data and the encoded instruction to all cascaded NSEs. Two result buses are provided to prevent contention due to the different latencies in Type-1 and Type-2 devices. The INDEX bus carries the result generated by Type-1 devices, as well as the SSV, SSF, FULL_IN, and FULL_OUT signals. Similarly, the SINDEX bus carries the result generated by Type-2 devices, as well as the SSSV and SSSF signals.

The FastLink Interface supports LVCMOS and HSTL I/O standards, with programmable drive strength. LVCMOS allows the I/O signals to run at up to 200 MHz for SDR clocking, and up to 100 MHz for DDR clocking. With HSTL, the I/O signals run up to 266-MHz SDR and 133-MHz DDR standalone.

FastLink Logical Interface

Commands are dispatched from the packet processor to the Ayama 20000 NSE via the LA-1 interface. The Associated Data Manager (ADM) is referenced to determine the target device. The operation is presented on the DQ and CMD buses, and if the command is targeted to a cascaded device, the CMDV and SCMDV signals direct the operation to the Type-1 or Type-2 cascade respectively. *Figure 5* shows the cascading of devices using the FastLink interface.

SRAM Interface

The Ayama 20000 device communicates with external NoBL memory via the SRAM Interface. Successful searches in the internal and cascaded NSEs return indices pointing to the location of the hit. The Ayama 20000 NSE has an internal SRAM memory controller that uses these indices to determine the offset for the associated data. The Ayama 20000 offloads

SRAM lookup overhead from the packet processors by automatically performing these associated-data lookups.

SRAM Physical Interface

The SRAM interface includes the following:

- Address bus
- Data and associated parity bus
- Chip and write enable

The Ayama 20000 SRAM Interface is compliant with NoBL SRAMs in the pipelined mode but does not support flow-through modes. The Ayama 20000 supports HSTL and LVCMOS SRAM at speeds up to 200 MHz.

The SRAM interface is also register configurable to run either at the same rate or half the rate of the SDR core clock. This half-rate support enables SRAM lookups when the core runs over 200 MHz. For example, to run the core at 266 MHz, the SRAM interface must be in half-rate mode and thus runs at 133 MHz.

SRAM Logical Interface

When a successful search returns an index, the Associated Data Manager (ADM) is referenced to determine the width of the table and the width of the associated SRAM entry. The ADM uses this information, together with the user-programmed offset for the table, to generate a pointer to the equivalent SRAM entry.

The Ayama 20000 manages the SRAM entries for the internal array and of any cascaded devices.

Table Widths, Data Array, and Mask Array

The Ayama 20000 contains a 9/18-Mbit TCAM core. The core consists of a data array, and a mask array.

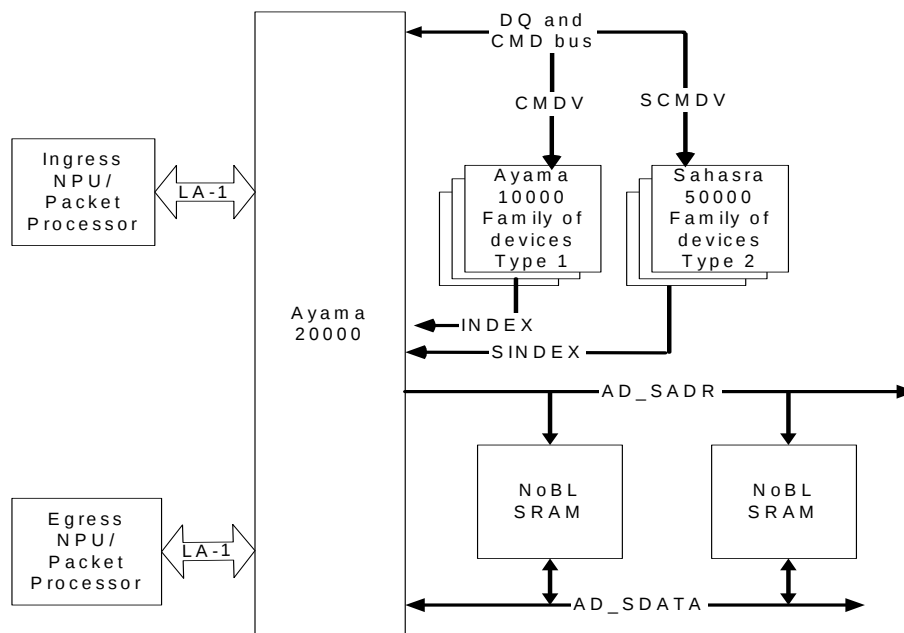


Figure 5. Cascading Devices Off the Fastlink Interface

The data array consists of 256k 72-bit TCAM words for an 18-Mbit device and 128k 72-bit TCAM words for a 9-Mbit device. Each TCAM word having a native size of 72 bits. Entries are logically grouped into blocks of 2k x 72-bit TCAM words, where the number of entries per block depend on entry width. For example, a 144-bit entry would occupy two 72-bit TCAM words and hence each block can only contain 1k 144-bit entries. These blocks are the building blocks of storage tables, which can be of various dimensions and are shown in *Figure 6*.

To facilitate selective search across entries within the same logical table, the Ayama 20000 NSE has a local mask entry corresponding to each data entry in the lookup table. Local masks identify the bits of a TCAM word that are considered in a search.

Besides local masks, the Ayama 20000 NSE provides a global mask facility to the packet processor. A global mask is selected by the packet processor for each search, and this global mask is overlaid on the local mask for all entries activated by the search.

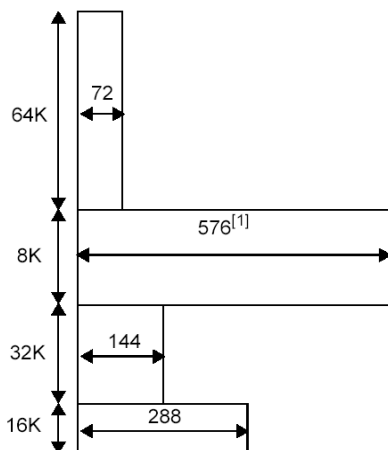


Figure 6. Multi-width Table Configuration

Basic Operations

The Ayama 20000 NSE has the following basic operations.

- Search
- Learn
- Read
- Write

For details, or for more information on advanced operations for specific features, see the Ayama 20000 Device Manual.

Search

To perform lookups on the database, the Ayama 20000 provides search commands in widths of x32, x72, x144, x288 and x576. Single and MultiSearch capabilities are offered to search one or two tables in a single cycle. A search operation takes in the following parameters:

- Global mask register (GMR). This selects one of sixteen user-programmed global masks to be applied to the search. This choice also selects the Mini-Key and a priority value. The Mini-Key allows the user to select which blocks are enabled for the search. The priority value allows the user to return a result that is equal to, or equal to or less than, the given priority.

- Associated Data Manager (ADM). Sixteen ADM registers store search profiles. The profile includes information on the associated data and key widths for efficient SRAM management, and instructions for whether the search returns an index and/or the results of the associated data lookup for that index.
- Search successful register (SSR). This register stores the search result in one of eight SSRs.
- Comparand register (CMPR). This register stores the search key, which can later be used for a learn, in one of sixteen CMPR registers. The CMPR is one-to-one mapped with a search result register (SRR), which stores the location of the next free entry within the blocks selected by the search.

Depending on the ADM configuration, a search returns an index and/or the associated data corresponding to that index. When configured for single search, a single key is provided and a single result is returned. When configured for MultiSearch, two searches are performed, one on each half of the array. If MultiSearch is enabled for 72-bit search keys, two independent search keys and GMRs can be provided, one for each half of the array. For larger key sizes, a single key is provided with independent GMRs for each side of the array.

Learn

In case of a search miss, or control plane updates, the NSE is able to add new entries to the data array using Learn. The Learn command writes data into the next free location within the table, and can be configured to learn user-provided data, or to learn from a previously-supplied search key. The next free location is stored in one of sixteen SRR registers.

The Learn with implicit Data command takes the following inputs:

- Width of the key to be learned
- Indication of whether the key is to be learned to the data or mask array, and to a single-search or MultiSearch enabled table
- Comparand register index. This register stores the data to be learned. Sixteen CMPRs are available to store search keys.

The Learn with Data commands are available in x72, x144, x288 and x576 widths, and takes the following inputs:

- Data to be learned
- Indication of whether the key is to be learned to the data or mask array.

Learn commands return the index where the information was stored and an indicator of whether there are more free entries remaining for future learns.

Read and Write

The Ayama 20000 provides read and write commands, for three target device categories:

- TCAM word or register values in the Ayama 20000 (or cascaded Type-1 devices)
- Data or register location in cascaded Type-2 devices
- Associated data SRAM.

Features

Atomic Command Sequences

Atomic Command sequences allow the packet processor to bind a set of instructions so that they are not interrupted during execution. This maintains coherence when tables are being updated while preventing intervening searches. Atomic Command sequences also reduce processor overhead by updating the result available notification only when all results from the Atomic Command sequence are available. This reduces the polling/interrupt overhead.

The Ayama 20000 reports results in the result FIFO only after the result for the last available command is available. Until then, an Empty FIFO indicator (EFI) value is returned. Once the result for the last command is available, the Result Available signal is asserted and the results may be read from the Result FIFO in the order they were received.

Key Capture™

Sequential searches often occur where keys differ only in port information or table identifier. The Key Capture feature improves LA-1 bandwidth utilization by allowing the reuse of the search key. Two bytes of each search key can be changed and the rest of the search key can be used, by passing a SameWDR command along with the bits that need to be changed in a single quadlet. This feature saves LA-1 cycles for the packet processor and increases headroom. Multiple SameWDR commands can be issued by re-using the previously stored search key. This feature can be used on search types of 72-bits or greater.

Clamshelling QDR™ SRAMs

Ayama 20000 NSEs support clamshelling of up to two QDR™ SRAMs. Clamshelling is the placement of devices directly opposite each other on both sides of a PCB. The footprint of each LA-1 port on an Ayama 20000 device is pin-compatible with a QDR SRAM. This allows up to two QDR SRAMs to be clamshelled to the opposite side of the circuit board where the Ayama 20000 is mounted. Each QDR SRAM is attached to a separate LA-1 port (see Figure 7).

When a QDR SRAM is clamshelled to an LA-1 port on an Ayama 20000 device, the QDR SRAM and the particular LA-1 port are separately enabled using the En[1:0] or the NPU's Read Port Select (RPS0 and RPS1) and Write Port Select (WPS0 and WPS1) respectively.

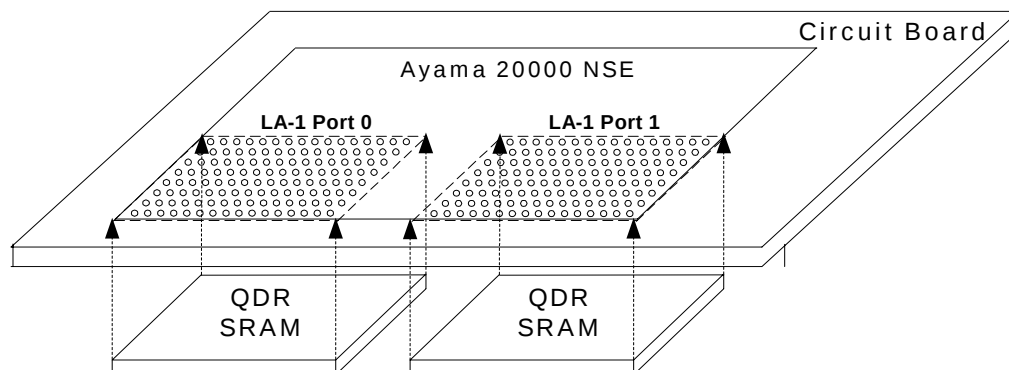


Figure 7. Clamshelling QDR SRAMs on the Ayama 20000

Clamshelling QDR SRAMs to the Ayama 20000 NSE reduces PCB board routing complexity. In some situations, clamshelling the QDR SRAMs may also eliminate line termination problems.

Mini-Key™

The Mini-Key feature reduces the power consumption by allowing the user to select which blocks are enabled for a search. Disabling remaining blocks considerably reduces power consumption. This feature simplifies table management by assigning up to four Mini-Key values per block, allowing each block to be a member of up to four logical tables. This is shown in Figure 8.

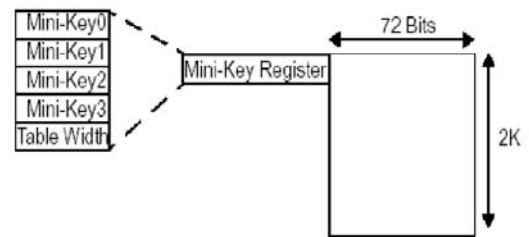


Figure 8. Mini-Key Block Association

When a search command is issued, it sends with it the Mini-Key value of the blocks it wants to search. A block is enabled when any one of four block Mini-Keys matches the Mini-Key issued by the search command. The remaining blocks are disabled on a cycle-by-cycle basis and do not take part in the search. Mini-Keys are supported by both the Ayama 20000 and any cascaded Ayama 10000 NSEs.

Full-speed 32-bit Searches

The full-speed 32-bit search feature enables full-speed searching of two 32-bit entries packed into a single TCAM word. Without this feature, either speed or density are sacrificed.

The native size of a TCAM word is 72 bits. However, if entries are 32 bits, the user would either populate each 72-bit TCAM word with only 32 bits of data and perform searches at full speed, or the user can populate each 72-bit field with two 32-bit entries, but perform two searches on the same table, each masking half of the array.

Full-speed 32-bit searches remove this trade-off by allowing 32-bit searches to operate at full speed while packing two 32-bit entries into each TCAM word. This feature requires that the APM feature be enabled.

MultiSearch™

The MultiSearch feature enables the Ayama 20000 to simultaneously search two different tables. This is done by dividing the core into two equal arrays. Each array consists of 64 or 32 blocks (corresponding to an 18-Mbit or 9-Mbit core respectively). Both tables are searched concurrently and a result is returned from each search.

For MultiSearch on tables up to 72 bits wide, each array can be searched using a different GMR and search key. *Figure 9(a)* shows a logical view of MultiSearch performed on 72-bit wide tables on both halves of the device.

For MultiSearch on keys larger than 72-bits, two searches can be performed from the same key, minimizing the number of cycles required to transfer a key and increasing the search rate. The first search uses the full key on one array. At the same time, the second search uses either the full key or a subset of the key to search on a table in the other array. The second table's width must be smaller or equal to the width of the search key.

For example, a 288-bit key can be provided for a search in a 288-bit table in Array 0. Simultaneously, a 144-bit subset of this key can be used with a different GMR to search a 144-bit table in Array 1, as shown in *Figure 9(b)*.

Cascaded Type-2 devices can only support MultiSearch for tables up to 72 bits wide.

AgeAssist™

Network lookup tables typically contain hundreds of thousands of entries. With heavy traffic, the topology of a network can change dramatically due to link failures, and the addition or removal of network devices. The AgeAssist feature of the Ayama 20000 helps increase switch performance by purging stale entries and making memory resources available for new entries.

The Age Memory Block can be used to keep track of the usage of each database entry. If a database entry has not been used for a certain amount of time, the entry is marked in the Age Memory Block. The information stored in this block may be used to consider which database entries to replace or filter out.

Hardware support is provided for reporting aging on up to 256k entries and up to four tables (if multiple tables are used, the total number of entries must be less than or equal to 256k). Two modes are supported, and are global to all age tables: single-buffered and double-buffered.

In the single-buffered case, time is divided into aging and read-out periods. The age table is cleared during device initialization. After the aging period (sampling interval), the table is read. While reading, software has the option of leaving the table enabled or disabling the table so that no additional updates are made. *Figure 10* shows the table structure of a single-buffered age table.

In the double-buffered case, a bit in the Age Information Register controls which of the two tables are available for reading, and which is used to flag accesses. In this way, one table is always being aged, and the other is in a position for reading, thereby enabling continuous aging. The drawback to the double-buffered solution is that the effective number of entries is halved. *Figure 11* shows the table structure of a double-buffered age table.

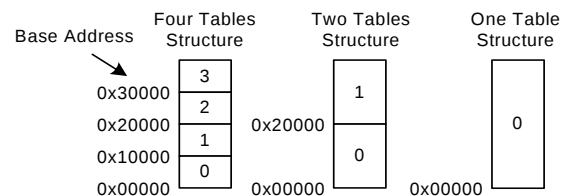


Figure 10. Single-Buffered Age Table Structure

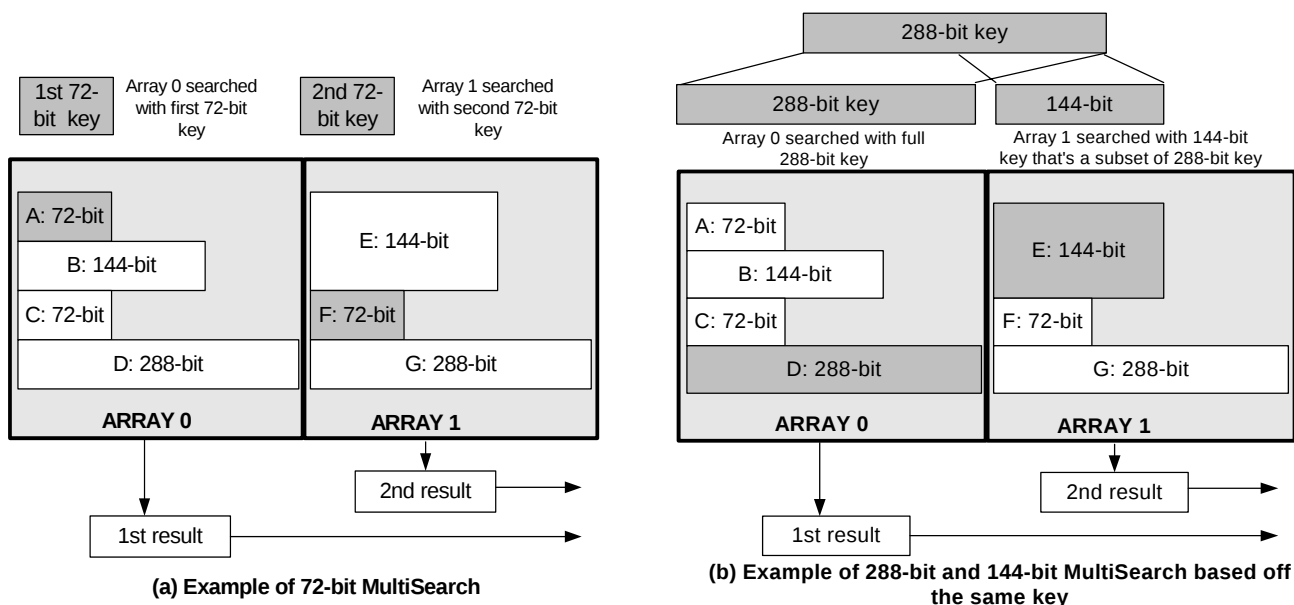


Figure 9. MultiSearch Operation

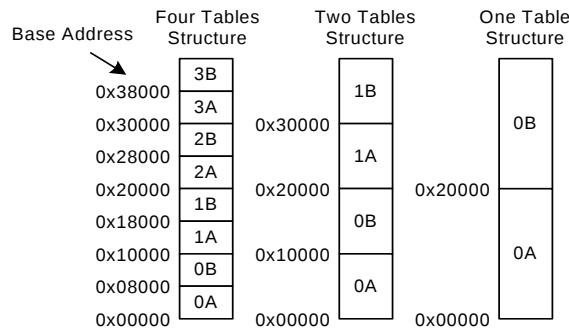


Figure 11. Double-Buffered Age Table Structure

Soft Priority™

The purpose of this feature is to resolve multiple hits and simplify table management.

To use this feature, blocks of data must be subdivided so that a priority value can be assigned to each one. Each block should be divided into four subblocks (shown in *Figure 12*) each of which is assigned a 6-bit Soft Priority value. To resolve multiple hits within a table, the sub-block with the highest priority is declared the winner. To resolve multiple hits among entries with the same Soft Priority value, the entry with the lowest address is the winner.

In an NSE where priority is determined solely by hit address, adding entries to a Longest Prefix Match Table could require multiple reshuffles or pre-assigned empty entries for future expansion. Soft priority removes this constraint by allowing the user to set priority on a sub-block basis, independent of the hit address.

The user can also provide a Soft Priority value on a search. The table can be configured to return a hit with either equal or equal-or-lower priority.

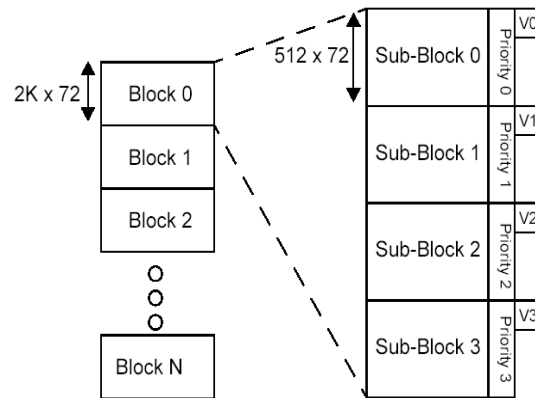


Figure 12. Soft Priority Sub-blocks

Associated Data Manager

The Associated Data Manager (ADM) enables flexible and efficient associated SRAM data management.

In TCAMs, the indices of the NSE table entries are one-to-one mapped to addresses on the external SRAM.

For NSE entries wider than 72-bits, memory gaps form on the external SRAM. *Figure 13* illustrates how these memory holes are created. For example, each 144-bit entry consists of two consecutive 72-bit TCAM words. However, only one SRAM address is needed for storing the corresponding associated data, and thus, without the ADM, one out of two SRAM address remains unused. In the case of 576-bit entries, each entry uses eight 72-bit TCAM words, thus seven SRAM memory locations are wasted.

When associated data is wider than the 32-bit native SRAM width, the SRAMs need to be width cascaded, potentially wasting board space.

The ADM solves this problem of inefficient SRAM space usage by removing the constraint of one-to-one mapping of 72-bit TCAM words to SRAM addresses. The ADM allows users to customize the ratio of the mapping for each table. Each table has a user-programmable SRAM offset to allow efficient packing of multiple tables of different NSE and SRAM entry widths.

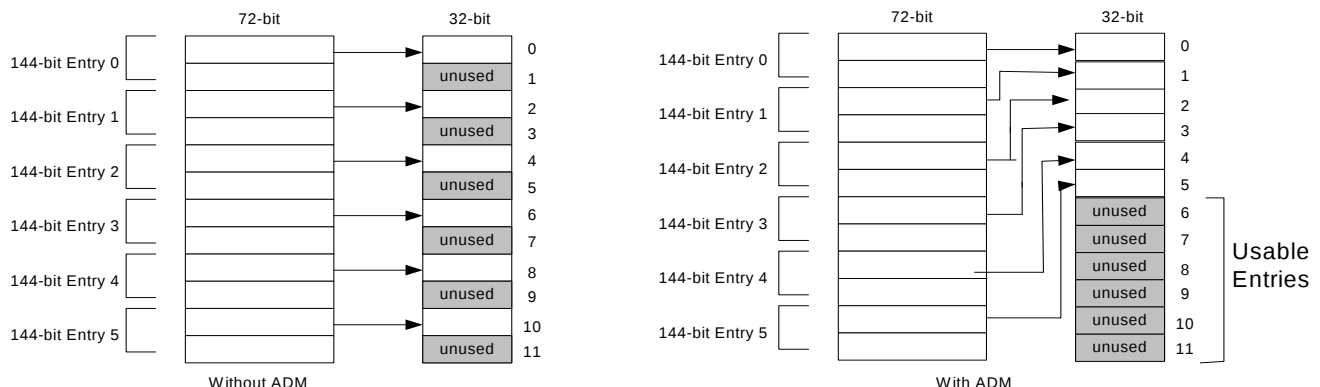


Figure 13. SRAM Memory Use With and Without ADM

Cascading for Storage

Additional NSEs can be cascaded to increase storage and search capabilities. The FastLink interface facilitates cascading and supports two types of devices:

- Type-1 devices must have command structures and latencies that match the Ayama 10000 family of devices.
- Type-2 devices must have command structures and latencies that match those of the Sahasra 50000 family of devices.

Although all devices share the same DQ and CMD buses, each type of device has its own result index bus (INDEX for Type-1 devices and SINDEX for Type-2 devices). When multiple hits occur across the different devices within the same type of device, the devices themselves perform the necessary arbitration to decide which device drives the result bus.

A maximum of 30 Type-1 devices can be cascaded using the FastLink Interface, while a maximum of seven Type-2 devices can be cascaded. Table 2 lists different features and their availability in cascaded Type-1 devices.

Table 2. Operation and Features for Cascaded Type-1 Devices

	MSE = 0 MultiSearch Disabled		MSE = 1 MultiSearch Enabled	
	1–7	8–30	1–7	8–30
# of Devices	1–7	8–30	1–7	8–30
MultiSearch Command	N/A	N/A	Yes	No
Learn Command	Yes	No	No	No
Mini-Key	Yes	Yes	Yes	Yes
Soft Priority	No	No	No	No
Full indicator	Yes	No	No	No
Associated Data Management	Yes	Yes	Yes	Yes

Parity

The Ayama 20000 checks and reports both core and interface parity errors on the LA-1, FastLink, and SRAM interfaces. An interrupt signal, PARERR_L, informs the packet processor of the error, while registers store the nature of the error.

Ayama 20000 features a core parity scan, which enables background scrubbing of the core. Every core parity read operation checks the parity on four adjacent 72-bit TCAM words on all 64/32 even or odd blocks in parallel. This parallel read minimizes the overhead associated with the core parity check.

Core parity errors are not fatal; instead the packet processor should overwrite the erroneous TCAM word with valid data to remove the error.

Interface parity is generated and checked on the LA-1, FastLink, and SRAM interfaces. The signals PARERR_L and SPARERR_L, inform the Ayama 20000 of parity errors in cascaded devices. Interface parity errors are fatal and a soft reset of the device must be performed to clear the error.

Errors

The Ayama 20000 reports command processing and parity errors. Command processing errors occur due to context FIFO overflow conditions and invalid commands. Parity checking is described in the previous section.

The signal EINTR asserts if an unmasked error is present, to alert the packet processor of the error condition. Error reporting registers identify the source of the error. Each error's source and type can be masked to prevent an associated error from asserting EINTR.

A context reset exists to clear a command error, allowing processing to complete before a software reset.

Clocking

Multiple clock domains are present on the Ayama 20000: one per LA-1 port and one for core. Each LA-1 clock domain extends to the direct access registers, the write ports of the data and command FIFOs, and the read ports of the result FIFOs. The FIFOs synchronize the data to the core clock. Beyond the FIFOs, the Ayama 20000 processes all data using the core clock. See Figure 15 for the clock domain diagram.

LA-1 Interface Clocking

Each LA-1 port has its own clock, and is treated independently from all other interfaces.

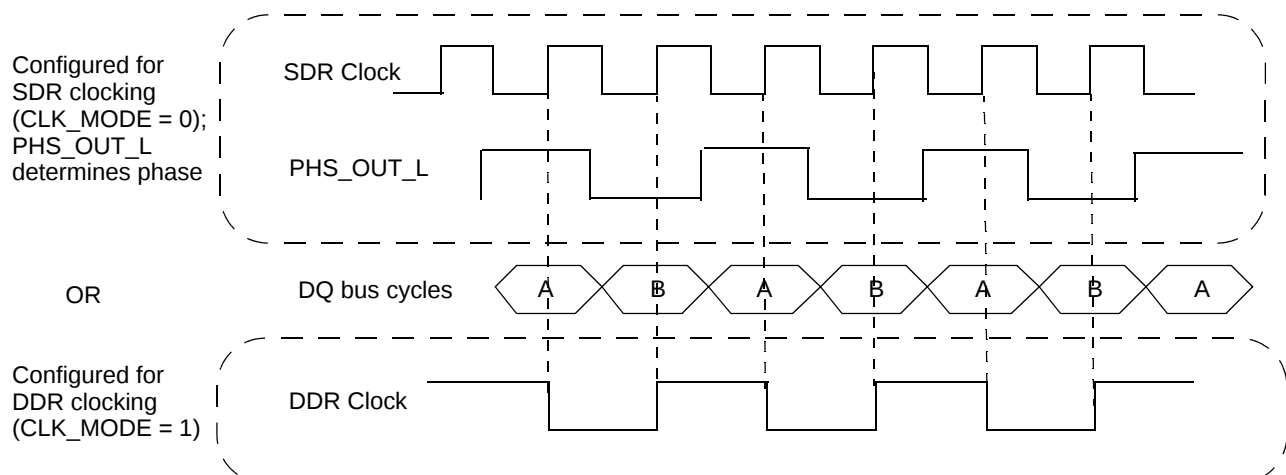


Figure 14. Ayama 20000 Clocks

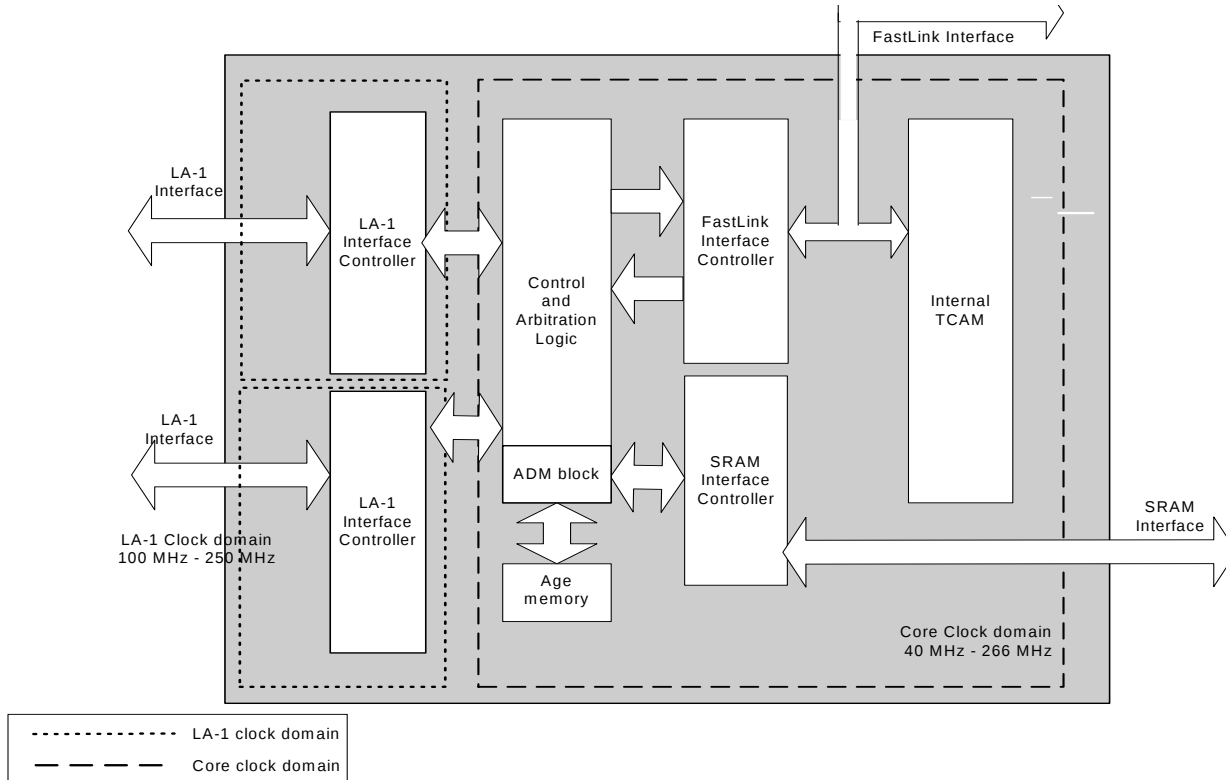


Figure 15. Clock Domain Diagram

Core Clocking

Once data is stored in the interface registers or context FIFOs, all processing moves to the core clock domain. This clock domain includes all state machines that interpret information flow, and is the clock domain for the outputs to the FastLink and the SRAM Interfaces. This clock domain operates from the CLK input with CLK_MODE selecting SDR or DDR clocking.

When configured for DDR clocking, commands are sent to cascaded devices from both rising and falling edges of the clock. In DDR clocking mode, cycle A occurs on the rising edge and cycle B on the falling edge. In SDR clocking mode, commands are sent to cascaded devices relative to the rising edge of the clock. PHS_OUT_L is a phase alignment signal used to distinguish between the cycles. Cycle A occurs when PHS_OUT_L is HIGH; cycle B occurs when PHS_OUT_L is LOW. See Figure 14 for details. When an Ayama 20000 device is configured for DDR clocking, PHS_OUT_L may be left unconnected.

The maximum core clock frequency is 266 MHz. Both the core and the FastLink interface are clocked relative to CLK. When devices are cascaded off the FastLink bus, the CLK frequency is limited by the interface timing, with a maximum of approximately 220 MHz.

The SRAM bus is similarly limited to 200 MHz. However, the Ayama 20000 is register configurable to run the SRAM interface at half the core frequency. As such, when a single Ayama 20000 has associated SRAMs attached, the following options are available:

- Run core and SRAM at the same frequency, up to 200 MHz.

- Run the SRAM interface at half speed. This enables core operation above 200 MHz with associated SRAM lookups. For example, the core can run at 266 MHz, with the SRAM interface at 133 MHz.

Reset and Power-on Sequence Requirements

System reset is initiated by asserting RST_L LOW. The master clock (CLK) must be running before and during the assertion of RST_L. RST_L assertion is recognized after a HIGH to LOW transition; i.e., RST_L cannot start LOW and then toggle HIGH. RST_L must be held LOW for t_{RESET} in order to reset the device. After RST_L is deasserted, the packet processor must wait for at least $t_{\text{RST_DELAY}}$ before accessing the device.

For each LA-1 port, if both K and C clocks are active, they must be running during reset. In addition, the rise time for RST_L must not exceed t_{RISE} .

Table 3. Reset Timing

Parameter	Minimum Duration
t_{RESET}	100 μs
$t_{\text{RST_DELAY}}$	1024 LA-1 clock cycles (slowest LA-1 port)
t_{RISE}	5 ns

The Ayama 20000 NSE contains two software resets—control logic reset and NSE array reset—allowing the device to be reset in two stages. The control logic must be reset first, followed by the TCAM Array. These resets are both initiated by setting a software reset register bit, which the Ayama 20000 then clears when the reset is complete. There is no wait period ($t_{\text{RST_DELAY}}$) after a soft reset.

The power-on sequence requires that the Core power (V_{DD}) be applied before the I/O power (V_{DDQ_Q} , V_{DDQ_A} , V_{DDQ_S}) to guarantee that the I/Os are in a known state when power is applied to the I/O signals. See *Tables 4 through 7* for the values during reset. For further information on the power-up sequence, please refer to the Ayama 20000 Device Manual.

Table 4. FastLink Interface Output/Bidirectional Signal Behavior During Hard/Soft Reset

Signal Name	Reset Value
CMD[10:0]	0
CMDV	0
SCMDV	0
DQ[71:0]	HIGH-Z
PAR[1:0]	HIGH-Z
ACK	1
PARERR_L	1
SPARERR_L	1
RESERVED	0
PHS_OUT_L	for CLK_MODE=1:0 for CLK_MODE=0:CLK/2

Table 5. LA-1 Interface Output/Bidirectional Signal Behavior During Hard Reset

Signal Name	Reset Value
Q0[15:0]	HIGH-Z
Q1[15:0]	HIGH-Z
CQ0	0
CQ1	0
CQ0_L	0
CQ1_L	0

Table 8. Supported Operations

Instruction	Type	Description
SAMPLE/PRELOAD	Mandatory	Sample/Preload. This operation loads the values of signals going to and from I/O signals into the boundary scan shift register to provide a snapshot of the normal operation.
EXTTEST	Mandatory	External Test. This operation uses boundary scan values shifted in from the TAP to test connectivity external to the device.
BYPASS	Mandatory	Bypass. This operation bypasses the device in a JTAG chain by loading a single bit shift register between TDI and TDO and provides a minimum-length serial path when no test operation is required.
IDCODE	Optional	Device JTAG ID Code. This operation selects the JTAG Identification register and outputs the IDCODE field serially through TDO.
CLAMP	Optional	Output Clamp. This operation drives preset values onto the outputs of the device.
HIGHZ	Optional	HIGH-Z Output. This operation sets the device output signals in high impedance state.

Table 6. Other Output Signal Behavior During Hard/Soft Reset

Signal Name	Reset Value
EINTR	0
RA0	0
RA1	0

Table 7. SRAM Interface Output/Bidirectional Signal Behavior During Hard/Soft Reset

Signal Name	Reset Value
AD_SADR[23:0]	0
AD_SDATA[31:0]	HIGH-Z
AD_SDATAP[3:0]	HIGH-Z
AD_CE_L	1
AD_WE_L	1

JTAG (IEEE 1149.1)

The Ayama 20000 device supports the Test Access Port (TAP) and Boundary Scan Architecture specified in IEEE JTAG Standard Number 1149.1. The JTAG interface to the chip consists of five signals with the standard functions: TCK, TMS, TDI, TDO, and TRST*. *Table 8* describes the operations that the TAP controller supports.

Electrical Specs and Operating Conditions

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature, condition B:..... -65°C to +150°C

Maximum Junction Temperature: 125°C

Static Discharge Voltage

(Human Body Model,

JEDEC EIA./JESD22-A114B,

MIL-STD-883E-3015): >2000V

ESD CDM Model (EIA/JESD22-C101C): >500V

Latch-up Current (EIA/JESD17): > ± 300mA

Table 9. Operating Conditions for Ayama 20000

Parameter	Description	Min.	Typical	Max.	Unit
V _{DDQ_x} = 2.5V	Operating voltage for I/O (2.5V LVCMOS)	2.3	2.5	2.7	V
V _{DDQ_x} = 1.8V	Operating voltage for I/O (1.8V LVCMOS)	1.65	1.8	1.95	V
V _{DDQ_x} = 1.5V	Operating voltage for I/O (1.5V HSTLI/II)	1.4	1.5	1.6	V
V _{REF}	Reference voltage for QDR and FastLink I/O (1.5V HSTLI/II)	V _{DDQ} /2	V _{DDQ} /2	V _{DDQ} /2	V
V _{DD}	Operating supply voltage	1.14	1.2	1.26	V
T _{A_C}	Ambient operating temperature	0		70	°C
T _J	Junction temperature	0		110	°C

Capacitance

Table 10. Capacitance Characteristics

Parameter	Description	Max.	Unit
C _{IN_LA1}	Input capacitance on LA-1 interface	5	pF ^[5]
C _{IN_SRAM}	Input capacitance on SRAM interface	10	pF ^[5]
C _{IN_FL}	Input capacitance on FastLink interface	18	pF ^[5]

DC Electrical Characteristics

This section describes the DC electrical specifications for the Ayama 20000 device.

Table 11 and Table 12 contain the electrical characteristics for the LA-1 Interface, as well as the FastLink and the SRAM Interfaces.

Table 11. LA-1 Interface DC Electrical Characteristics

Parameter	Description	Conditions	Min.	Max.	Unit	Notes
V _{IH}	Input HIGH (logic 1) voltage		V _{REF} + 0.1	V _{DDQ_Q} + 0.3	V	6
V _{IL}	Input LOW (logic 0) voltage		-0.3	V _{REF} - 0.1	V	7
V _{OH_DC}	Output HIGH voltage	I _{OH} ≤ 0.1 mA	V _{DDQ_Q} - 0.2	V _{DDQ_Q}	V	
V _{OL_DC}	Output LOW voltage	I _{OL} ≤ 0.1 mA	V _{SS}	0.2	V	
V _{OH_AC}	Output HIGH voltage	I _{OH} ≥ 8 mA, class I; I _{OH} ≥ 16 mA, class II	V _{DDQ_Q} - 0.5	V _{DDQ_Q}	V	
V _{OL_AC}	Output LOW voltage	I _{OL} ≥ 8 mA, class I; I _{OL} ≥ 16 mA, class II	V _{SS}	V _{SS} + 0.5	V	
V _{DDQ_Q}	Output buffer supply voltage	V _{DDQ_Q} = 1.5V nominal	1.4	1.6	V	
V _{REF}	Input reference voltage	V _{REF} = V _{DDQ_Q} /2 nominal	0.7	0.8	V	
I _{LI}	Input leakage current		-10	10	μA	
I _{LO}	Output leakage current		-10	10	μA	

Notes:

5. f = 1 MHz, V_{IN} = 0 V. Tested initially and after any design or process change that may affect these parameters.

6. Maximum allowable applies to overshoot only.

7. Minimum allowable applies to undershoot only.

Table 12. FastLink Interface and SRAM Interface DC Electrical Characteristics ^[8]

Parameter	Description	Conditions	Min.	Max.	Unit	Notes
I_{LI}	Input leakage current	$V_{DDQ} = V_{DDQ} \text{ Max.}, V_{IN} = 0 \text{ to } V_{DDQ} \text{ Max.}$	-10	10	μA	
I_{LO}	Output leakage current	$V_{DDQ} = V_{DDQ} \text{ Max.}, V_{IN} = 0 \text{ to } V_{DDQ} \text{ Max.}$	-10	10	μA	
V_{IL1}	Input LOW voltage (1.8V)		-0.3	$0.35 V_{DDQ}$	V	7
V_{IH1}	Input HIGH voltage (1.8V)		$0.65 V_{DDQ}$	$V_{DDQ} + 0.3$	V	6
V_{OL1}	Output LOW voltage (1.8V)	$V_{DDQ} = V_{DDQ} \text{ Min.}, I_{OL} = 2 \text{ mA}$		0.45	V	
V_{OH1}	Output HIGH voltage (1.8V)	$V_{DDQ} = V_{DDQ} \text{ Min.}, I_{OH} = 2 \text{ mA}$	$V_{DDQ} - 0.45$		V	
V_{IL2}	Input LOW voltage (2.5V)		-0.3	0.7	V	7
V_{IH2}	Input HIGH voltage (2.5V)		1.7	$V_{DDQ} + 0.3$	V	6
V_{OL2}	Output LOW voltage (2.5V)	$V_{DDQ} = V_{DDQ} \text{ Min.}, I_{OL} = 2 \text{ mA}$		0.7	V	
V_{OH2}	Output HIGH voltage (2.5V)	$V_{DDQ} = V_{DDQ} \text{ Min.}, I_{OH} = 2 \text{ mA}$	1.7		V	
V_{IL3}	Input LOW voltage (1.5V)		-0.3	$V_{REF} - 0.1$	V	7
V_{IH3}	Input HIGH voltage (1.5V)		$V_{REF} + 0.1$	$V_{DDQ} + 0.3$	V	6
V_{REF}	Input reference voltage		0.7	0.9	V	
V_{OL3_DC}	Output LOW voltage (1.5V)	$V_{DDQ} = V_{DDQ} \text{ Min.}, I_{OL} = 0.1 \text{ mA}$	V_{SS}	0.2	V	
V_{OH3_DC}	Output HIGH voltage (1.5V)	$V_{DDQ} = V_{DDQ} \text{ Min.}, I_{OH} = 0.1 \text{ mA}$	$V_{DDQ} - 0.2$	V_{DDQ}	V	

AC Timing Parameters, Waveforms, and Test Conditions

The following shows I/O standards supported on each interface of the device for three different core frequencies.

Table 13. Speed Grade Mapping to Various Interface Frequencies

Interface	CYNSE20XXX-266 ^[10]		CYNSE20XXX-200 ^[10]		CYNSE20XXX-166 ^[10]	
	HSTL	LVC MOS	HSTL	LVC MOS	HSTL	LVC MOS
FastLink/Core	266 MHz ^[9]	200 MHz	200 MHz	200 MHz	166 MHz	166 MHz
QDR-II	250 MHz	NA	235 MHz	NA	200 MHz	NA
SRAM	200 MHz	200 MHz	200 MHz	200 MHz	166 MHz	166 MHz

LA-1 QDR-II AC Timing Parameters and Waveforms

Table 14. LA-1 QDR-II AC Timing Parameters

Parameter	Description	200 MHz ^[13]		235/250 MHz ^[13]		Unit	Notes
		Min.	Max.	Min.	Max.		
Clock Timing							
KC var	Clock phase jitter		0.2		0.2	ns	10
t _{KHKH}	Clock cycle time	5.0	6.0	4.7/4.0	6.0	ns	12
t _{KHKL}	Clock HIGH time	2		1.75		ns	
t _{KLKH}	Clock LOW time	2		1.75		ns	
t _{KHK#H}	K, C to K#, C#	2.3		1.8		ns	
t _{K#HKH}	K#, C# to K, C	2.3		1.8		ns	
t _{KHCH}	K to C clock skew	0	2.3	0.45	1.8	ns	
Input Set-up Timing							
t _{AVKH}	Address input valid to clock HIGH	0.6		0.3		ns	
t _{DVKH}	Data input valid to clock HIGH	0.6		0.3		ns	

Notes:

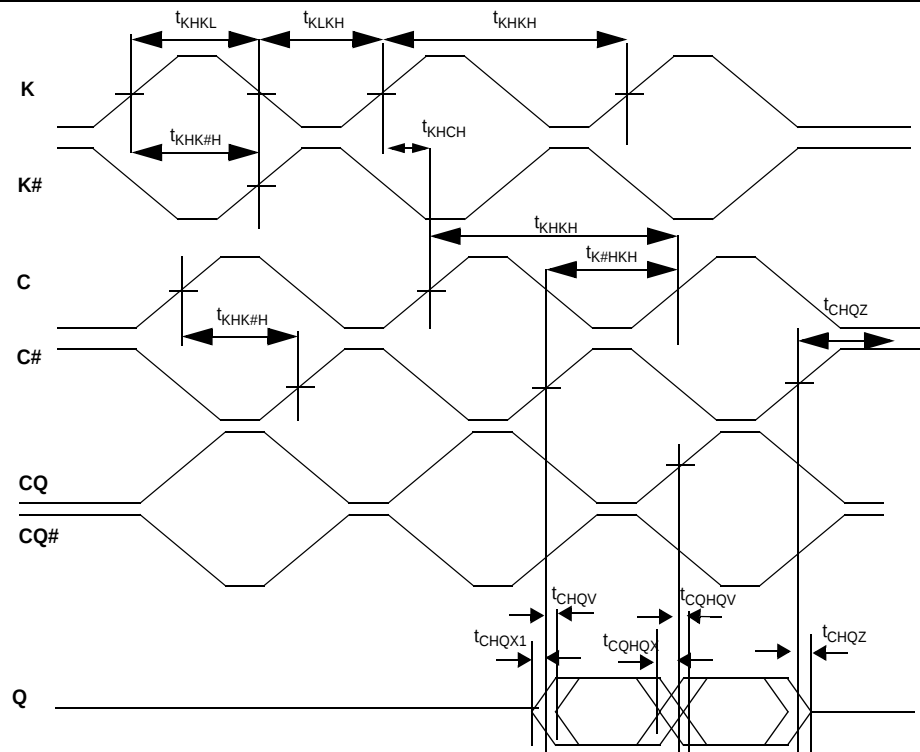
8. All references to V_{DDQ} in the above table applies to both V_{DDQ_A} and V_{DDQ_S} .
9. See Core Clocking section for restrictions on the core clock operating due to interface timing with cascaded devices.
10. Part number extension refers to maximum FastLink bus and core clock speed.
11. Tested initially and after any design or process changes that may affect these parameters, but not production tested.
12. For CYNSE20XXX-266, min cycle time is 4 ns as QDR-II fmax is 250 MHz. For CYNSE20XXX-200 MHz, min cycle time is 4.7 ns as QDR-II fmax is 235 MHz.
13. Frequencies apply to LA-1 operating frequency, not speed bin. See Table 14 for the maximum LA-1 operating frequency corresponding to each speed bin.

Table 14. LA-1 QDR-II AC Timing Parameters (continued)

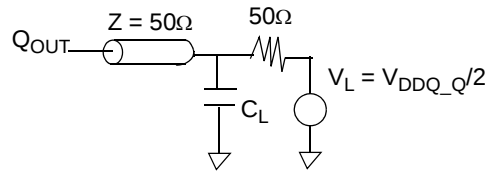
Parameter	Description	200 MHz ^[13]		235/250 MHz ^[13]		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{IVKH}	Control input valid to clock HIGH	0.6		0.4		ns	15, 14
Input Hold Timing							
t_{KHAX}	Clock HIGH to address hold	0.65		0.55		ns	
t_{KHDX}	Clock HIGH to data input hold	0.65		0.55		ns	
t_{KHIX}	Clock HIGH to control input hold	0.65		0.6		ns	15, 14
Output Timing							
t_{CHQV}	C, C# HIGH to data output valid		0.75		0.7	ns	17, 18
t_{CHQX}	C, C# HIGH to data output hold	-0.4		-0.3		ns	17, 18
t_{CHCQV}	C, C# HIGH to echo clock valid		0.55		0.5	ns	18
t_{CHCQX}	C, C# HIGH to echo clock hold	-0.4		-0.35		ns	18
t_{CQHqV}	CQ, CQ# HIGH to data output valid		0.5		0.47	ns	18
t_{CQHqX}	CQ, CQ# HIGH to data output hold	-0.55		-0.45		ns	18
t_{CHQZ}	C, C# HIGH to output HIGH-Z		0.75		0.7	ns	16, 10
t_{CHQX1}	C, C# HIGH to output LOW-Z	-0.4		-0.3		ns	16, 10

Table 15. Other LA-1 Interface Signal Timing, all speed bins

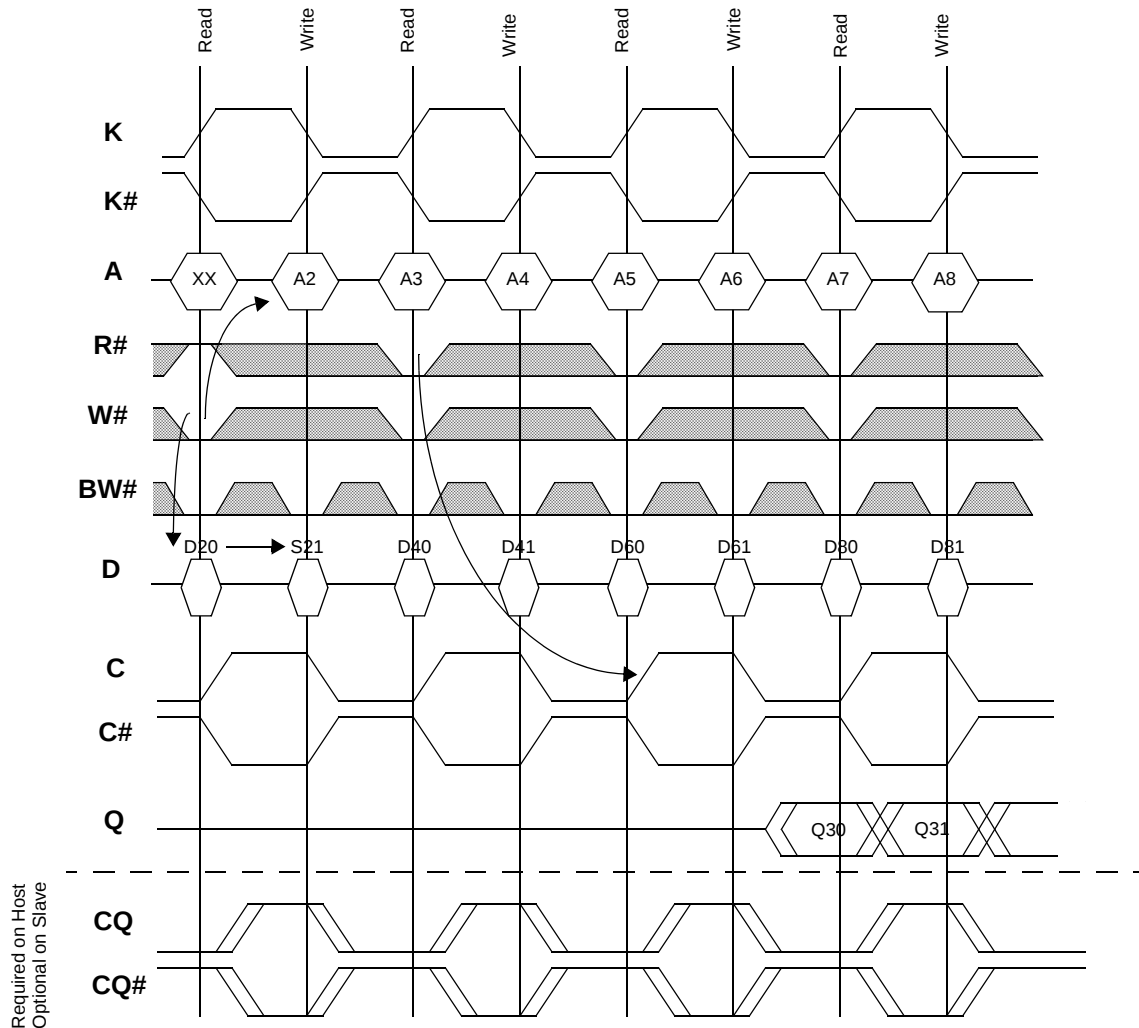
Parameter	Description	Min.	Max.	Unit
t_{RADV}	K HIGH to RA valid		3.0	ns
t_{RADH}	K HIGH to RA hold	1.2		ns


Figure 16. Illustration of QDR-II LA-1 Output Timing Parameters
Notes:

14. Applies to R#, W#, BW# and E[1:0].
15. Control input signals may not be operated with pulse widths less than t_{KHKL} (Min).
16. Transition is measured ± 100 mV from steady state voltage.
17. These parameters take precedence for slave ports implemented without echo clocks.
18. Test load shown in Figure 27; 16-mA drive strength.

LA-1 Test Conditions and Output Load


Input pulse levels	0.25V to 1.25V
Input rise and fall times	0.3ns
Input timing reference levels	0.75V
Output reference levels	$V_{DDQ_Q}/2$
C_L	5pF

Figure 17. HSTL I/O Output Load
LA-1 Timing Waveforms

Figure 18. Simplified Timing Diagram for LA-1 Port Operation

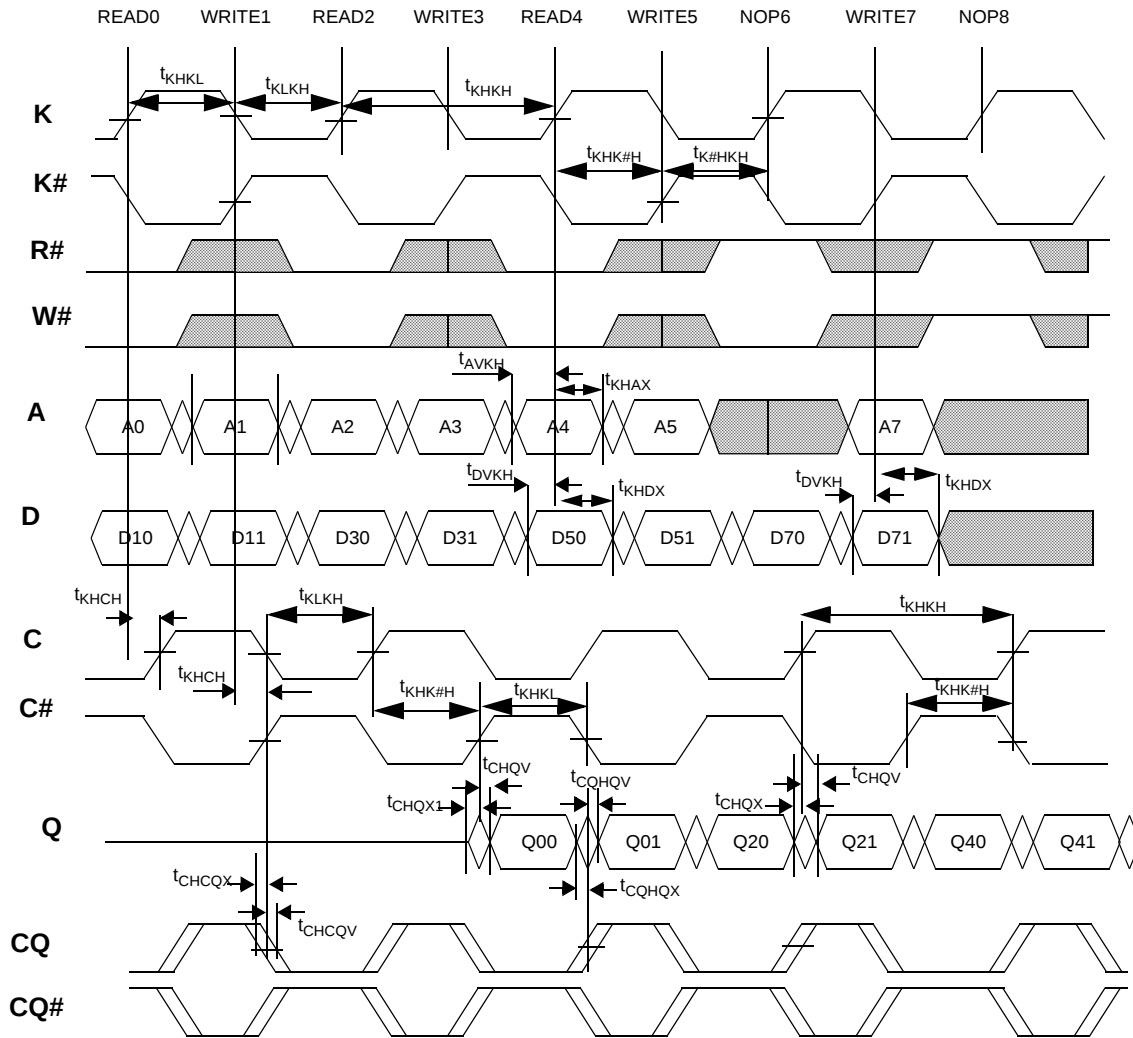


Figure 19. LA-1 Port Burst-of-2 Read and Write Timing Diagram

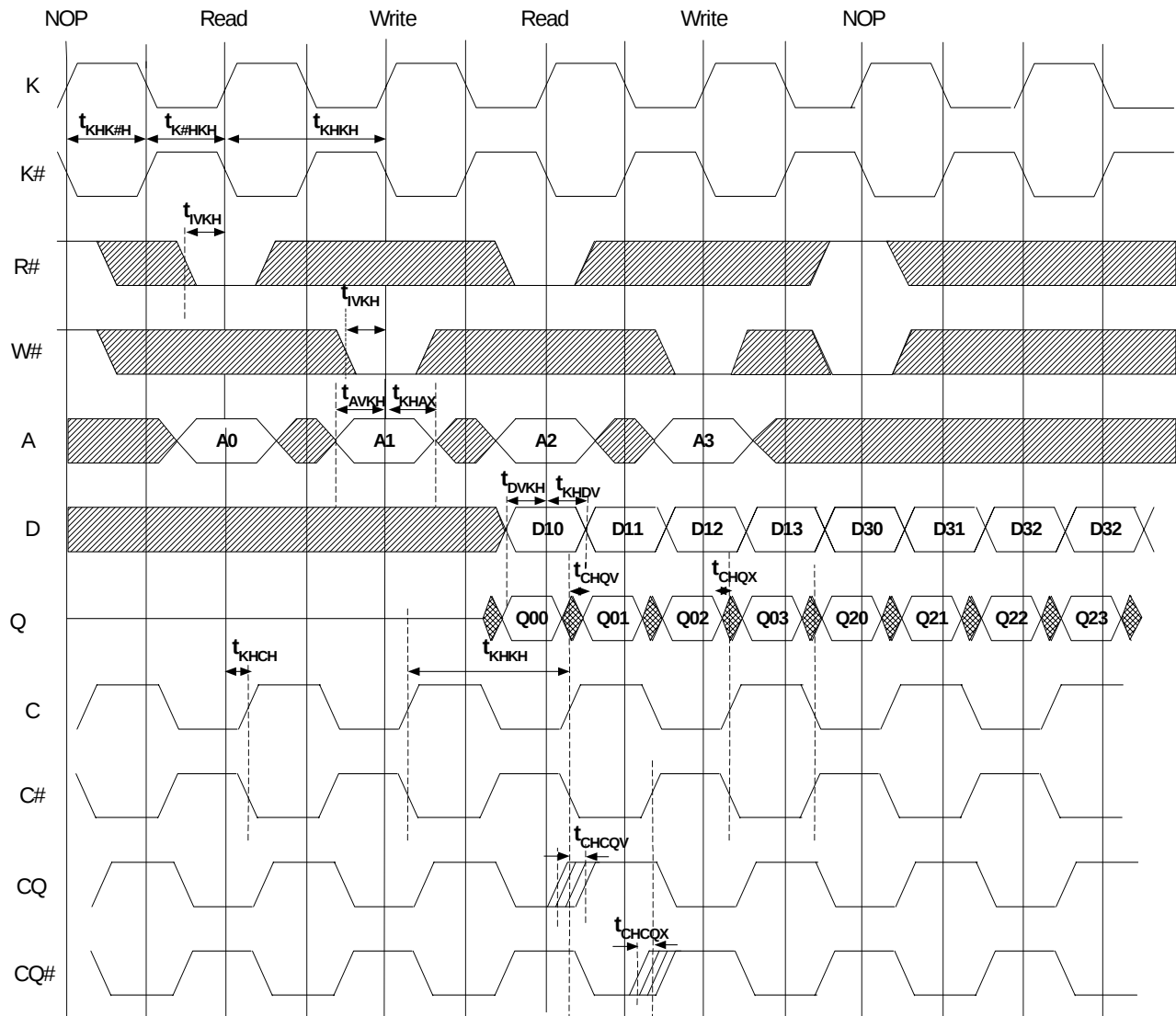


Figure 20. LA-1 port Burst-of-4 Read and Write Timing Diagram

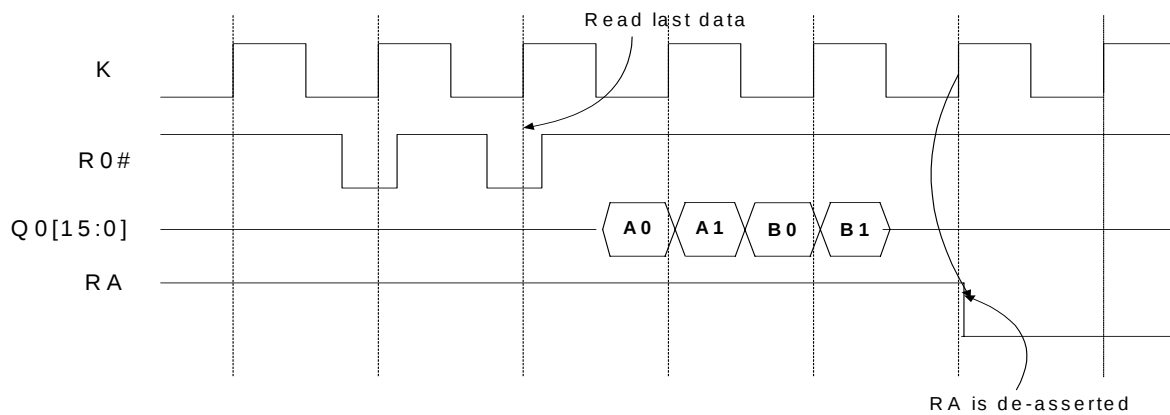


Figure 21. RA Timing Waveform

CLK Timing Parameters

Table 16. CLK Timing Parameters

Parameter	Description	166 MHz HSTL/LVCMOS FastLink/Core		200 MHz LVCMOS/HSTL FastLink/Core		266 MHz HSTL FastLink/Core		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{CLK_SDR}	SDR core clock frequency	100	166	100	200	100	266	MHz
f_{CLK_DDR}	DDR core clock frequency	50	83	50	100	50	133	MHz
DC_CLK	CLK duty cycle	40	60	40	60	40	60	%

FastLink AC Timing

Table 17. FastLink AC Timing Parameters^[19, 20]

Parameter	Description	166 MHz HSTL/LVCMOS FastLink/Core		200 MHz LVCMOS/HSTL FastLink/Core		266 MHz HSTL FastLink/Core		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{ISCH_DQ}	DQ, PAR input set-up time to CLK rising edge	0		0		0		ns	21
t_{ISCH}	xPARERR_L, ACK set-up time to CLK rising edge	0.9		0.75		0.65		ns	
t_{IHCH_DQ}	DQ input hold time after CLK rising edge	0.7		0.6		0.55		ns	
t_{IHCH}	xPARERR_L, ACK, FULL_IN hold after CLK rising edge	0.85		0.75		0.7		ns	
t_{ISIND}	Index set-up time to CLK rising edge	1.0		0.95		0.85		ns	
t_{IHIND}	Index hold time after CLK rising edge	0.9		0.8		0.7		ns	
t_{IS_HIT}	Input set-up time to LHI and BHI	4.5		4.0		3.5		ns	
t_{IS_FUL}	Input set-up time to FULI	1.8		1.8		1.8		ns	
t_{IH_HIT}	LHI, BHI hold time after CLK rising edge	0		0		0		ns	
t_{IH_FUL}	FULI hold time after CLK rising edge	0.8		0.7		0.5		ns	
t_{CKHOH_HSTL}	DQ bus hold time after CLK rising edge, HSTL	0.7		0.8		0.95		ns	23
t_{CKHOH_CMOS}	DQ bus hold time after CLK rising edge, LVCMOS	0.4		0.5				ns	23
t_{CKHOH_CMD}	CMD bus hold time after CLK rising edge	0.3		0.4		0.6		ns	22
t_{CKHOH_PHS}	PHS_OUT_L hold after CLK rising edge	0.8		0.9		1.1		ns	22
t_{CKHOH_HIT}	LHO, BHO hold time after CLK rising edge	0.5		0.5		0.7		ns	22
t_{CKHOH_FUL}	FULO hold time after CLK rising edge	1.0		1.1		1.2		ns	22
t_{CKHOH_F}	FULL_OUT hold time after CLK rising edge	0.5		0.5		0.7		ns	22
t_{CKHOH_E}	EINTR hold time after CLK rising edge	0.3		0.4		0.5		ns	22
t_{CKHDV_HSTL}	Rising edge of CLK to DQ valid, HSTL mode		3.3		3.1		3.0	ns	23
t_{CKHDV_CMOS}	Rising edge of CLK to DQ valid, LVCMOS mode		2.9		2.75			ns	22
t_{CKHDV_CMD}	Rising edge of CLK to CMD valid		2.6		2.4		2.3	ns	22
t_{CKHDV_PHS}	Rising edge of CLK to PHS_OUT_L valid		3.1		2.9		2.8	ns	22
t_{CKHDV_HIT}	Rising edge of CLK to LHO, BHO valid		4.3		3.4		3.4	ns	22
t_{CKHDV_FUL}	Rising edge of CLK to FULO valid		7.4		6.5		6.2	ns	22
t_{CKHDV_F}	Rising edge of CLK to FULL_OUT valid		3.6		3.4		3.0	ns	22
t_{CKHDV_E}	Rising edge of CLK to EINTR valid		2.6		2.4		2.2	ns	22

Notes:

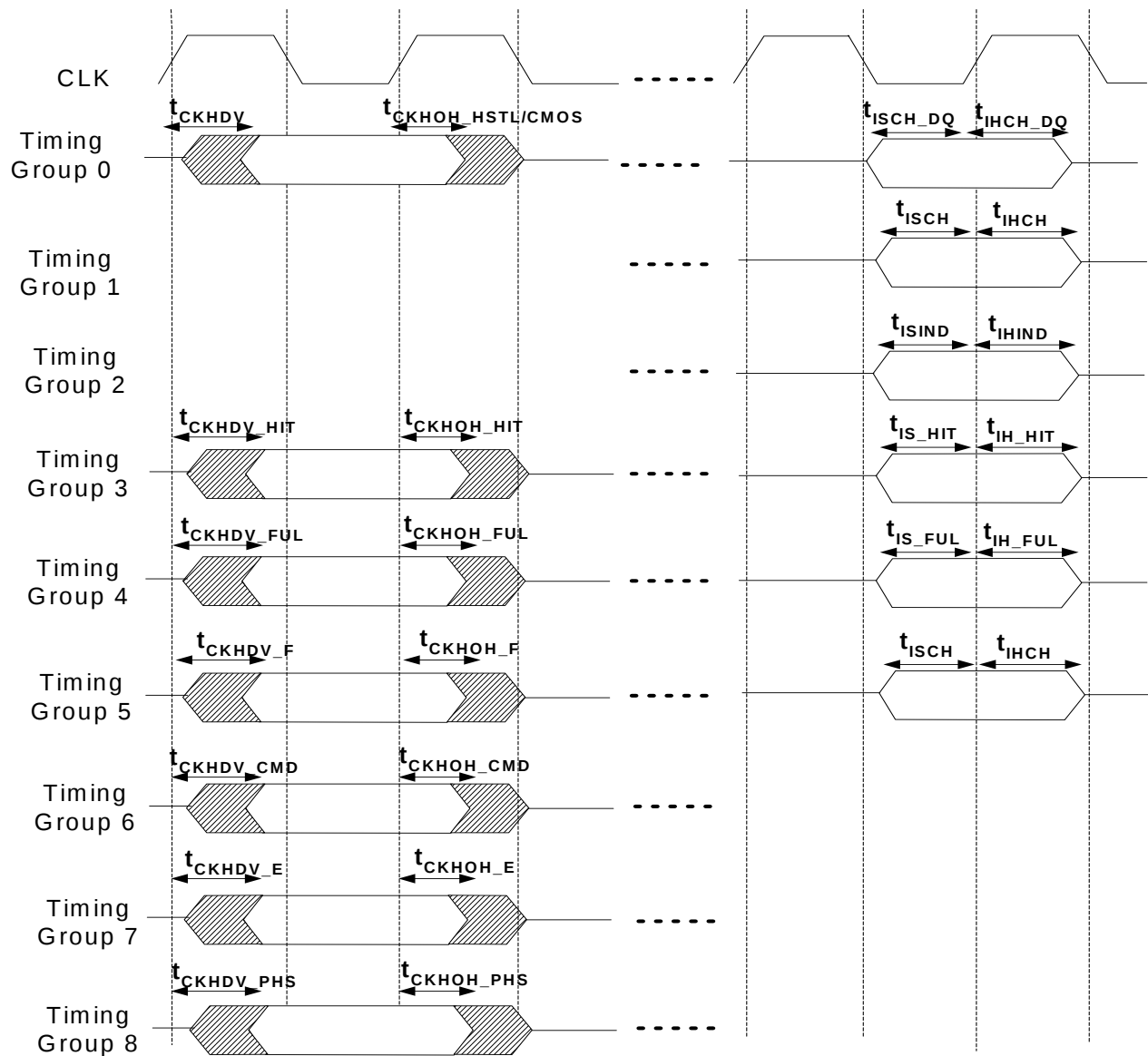
19. Description below and testing done for SDR clocking mode. For DDR clocking mode, the same timing numbers apply to either the rising or falling edges, by design.

20. Values are based on 50% signal levels unless otherwise stated.

21. Guaranteed by design.

22. Test load shown in Figure 27; HSTL 16-mA drive strength. LVCMOS 16-mA drive strength.

23. Test load shown in Figure 28; HSTL 16-mA drive strength. LVCMOS 16-mA drive strength.



Timing Group 0: DQ, PAR
Timing Group 1: ACK, PARERR_L, SPARERR_L
Timing Group 2: SINDEX, SSSV, SSSF, SSV, SSF, INDEX
Timing Group 3: LHI, LHO, BHI, BHO
Timing Group 4: FULL, FULO
Timing Group 5: FULL_OUT, FULL_IN
Timing Group 6: CMD, CMDV, SCMDV
Timing Group 7: EINTR
Timing Group 8: PHS_OUT_L

Figure 22. Fastlink Timing

SRAM AC Timing Parameters and Waveforms

Table 18. SRAM AC Timing Parameters^[20]

Parameter	Description	166 MHz LVCMOS/HSTL SRAM		200MHz LVCMOS SRAM		200 MHz HSTL SRAM		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{IS_AD}	Input setup time to CLK rising edge	0.95		0.6		0.6		ns	
t_{IH_AD}	Input hold time to CLK rising edge	1.0		0.85		0.85		ns	
t_{CKHDV_AD}	Rising edge of CLK to data valid		2.7		2.0		2.4	ns	24
t_{OH_AD}	Output hold time after the rising edge of CLK	0.3		0.45		0.65		ns	24
t_{CKHZD_AD}	Rising edge of CLK to data LOW-Z	0.3		0.45		0.65		ns	10, 25

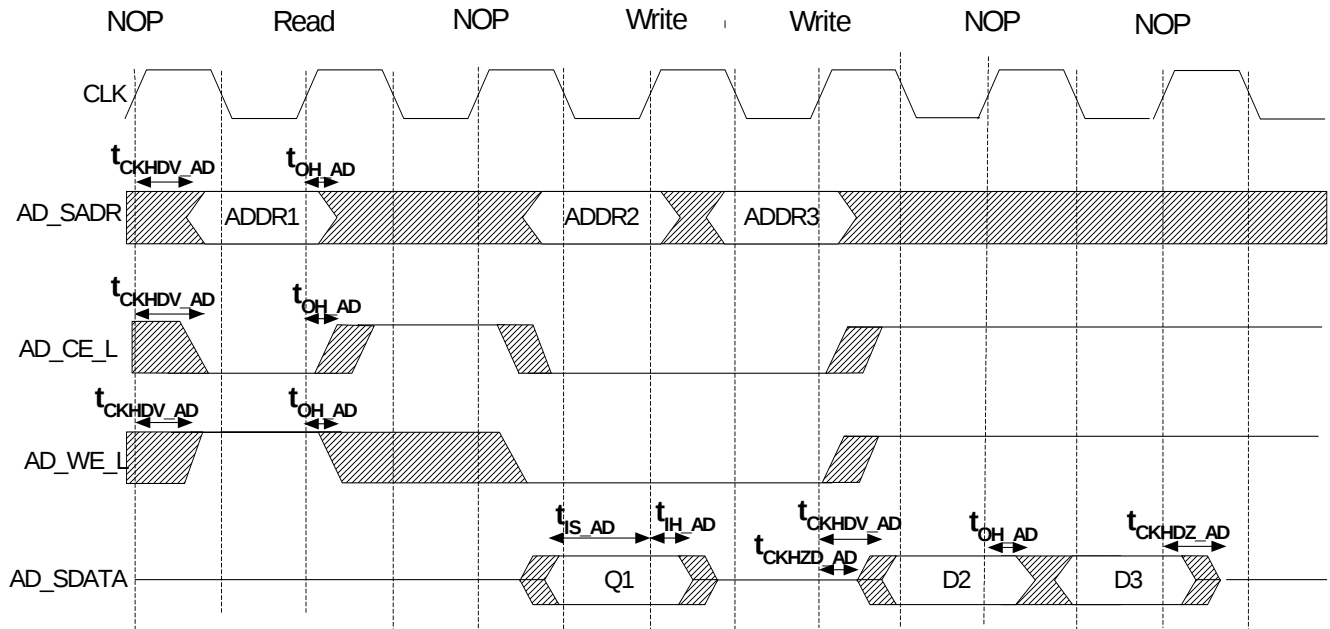


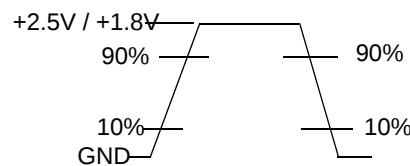
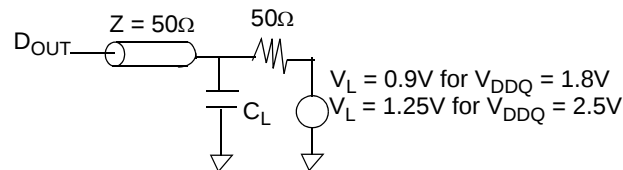
Figure 23. SRAM Timing

Notes:

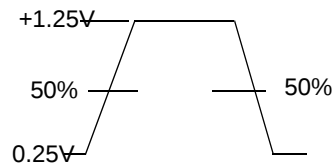
24. Test load shown in Figure 27; HSTL 16-mA drive strength, LVCMOS 8-mA and 16-mA drive strength.
25. Transition is measured ± 100 mV from steady state voltage.

**FastLink and SRAM Interface AC Test
Conditions and Output Loads**
Table 19. LVCMOS AC Test Conditions and Output Loads

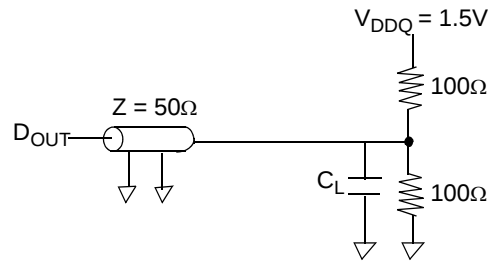
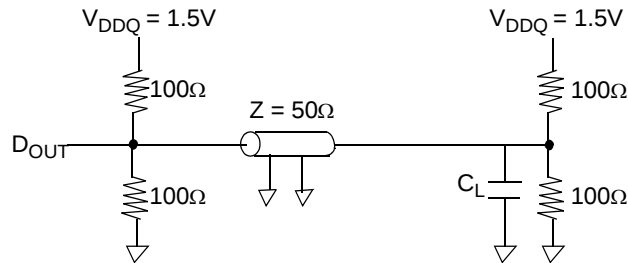
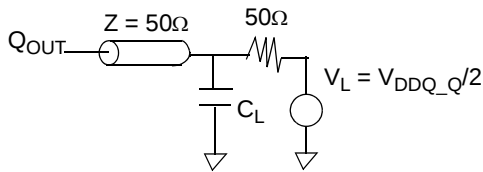
Conditions	Results
Input pulse levels	GND to 2.5V / 1.8V
Input rise and fall times measured for 2.5V LVCMOS at 0.25V and 2.25V	$\leq 1.2 \text{ ns}^{[26]}$
Input rise and fall times measured for 1.8V LVCMOS at 0.18V and 1.98V	$\leq 1.2 \text{ ns}^{[26]}$
Input timing reference levels (2.5V/1.8V)	1.25V/0.9V
Output reference levels (2.5V/1.8V)	1.25V/0.9V
Output load (C_L)	6 pF
Junction Temperature (T_j)	110°C


Figure 24. LVCMOS I/O Input Waveform

Figure 25. LVCMOS I/O Output Load
Table 20. HSTL I/II AC Test Conditions and Output Loads

Conditions	Results
Input pulse levels	0.25V to 1.25V
Input rise and fall times measured at 20% and 80% of input pulse	Faster than $1\text{V/ns}^{[26]}$
Input timing reference levels	0.75V
Output reference levels	0.75V
Output load (C_L)	6 pF
Junction Temperature (T_j)	110°C


Figure 26. HSTL I/II I/O Input Waveform
Note:

26. Tested initially and after any design or process change that may affect this parameter.


Figure 27. HSTL I I/O Output Load

Figure 28. HSTL II I/O Output Load
LA-1 Test Conditions and Output Load


Input pulse levels	0.25 V to 1.25 V
Input rise and fall times	0.3 ns
Input timing reference levels	0.75 V
Output reference levels	$V_{DDQ_Q}/2$
CL	6 pF

Figure 29. LVC MOS I/O Output Load
JTAG Timing
Table 21. JTAG Timing Parameters

Parameter	Description	All bins		Unit
		Min.	Max.	
f_{JTAG}	Maximum JTAG TAP Controller Frequency		10	MHz
t_{TCYC}	TCK Clock Cycle Time	100		ns
DC_{JTAG}	TCK Clock Duty Cycle	40	60	%
t_{TMSS}	TMS Set-up to TCK Clock Rise	10		ns
t_{TMSH}	TMS Hold After TCK Clock Rise	10		ns
t_{TDIS}	TDI Set-up to TCK Clock Rise	10		ns
t_{TDIH}	TDI Hold After TCK Clock Rise	10		ns
t_{TDOV}	TCK Clock LOW to TDO Valid		10	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0		ns



PRELIMINARY

CYNSE20512
CYNSE20556

Signal Assignments and Pinout Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	
A	no ball	NC	NC	NC	NC	NC	NC	DOF0_L	NC	NC	NC	NC	NC	NC	CQ0_L	E0[0]	CLK	VSS	E0[0]	CQ1	Q0[8]	Q1[8]	D1[7]	Q0[6]	Q0[5]	D1[5]	NC	D1[4]	Q0[3]	Q0[2]	D1[2]	D1[1]	RSVD	no ball	
B	IC0[1]	NC	DP0[1]	NC	Q0[15]	NC	NC	Q0R0R EF1	D0[13]	Q0[12]	NC	D0[11]	NC	Q0[9]	NC/A0 [24]	E0[1]	CLK_M ODE	RST_L	E1[0]	NC/A1 [20]	NC	Q0[7]	NC	D1[6]	NC	NC	Q0R1R EF0	Q1[4]	D1[3]	NC	Q1[1]	NC	VSS	VSS	
C	A0[6]	Q0[0]	Q0[0]	DP0[0]	D0[15]	Q0[14]	D0[14]	VDDQ_Q	Q0[13]	D0[12]	Q0[11]	Q0[10]	D0[10]	D0[9]	A0[19]	EP0[0]	RA0	RA1	EP1[0]	A1[5]	NC	NC	NC	NC	NC	NC	Q0R1R EF0	NC	NC	NC	NC	NC	VSS		
D	A0[8]	A0[10]	VSS_PL L	VSS	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VSS	VSS	A0[4]	W0_L	EP0[1]	NC	NC	EP1[1]	R1_L	A1[3]	VSS	VSS	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VSS	VSS	VSS	VSS	
E	A0[18]	A0[18]	A0[14]	VSS	VSS	VDD_PL L	VDD	VDD	VDD	VDD	VSS	VSS	A0[2]	NC	BW0_L [1]	RSVD	NC	NC	RSVD	NC	BW1_L [0]	A1[1]	VSS	VSS	VDD	VDD	VDD	VDD	VDD	VSS	VSS	A1[13]	VSS	VSS	
F	C0_L	C0	A0[12]	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	A0[0]	K0	K0_L	TEST_PB	NC	RSVD	RSVD	K1_L	K1	A1[0]	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	A1[12]	VSS	VSS	
G	A0[17]	A0[15]	A0[13]	VSS	VSS	VDD	VDD	VDD	VDD	VDD	VSS	VSS	A0[1]	NC	BW0_L [0]	NC	RSVD	NC	NC	RSVD	BW1_L [1]	NC	A1[2]	VSS	VSS	VDD	VDD	VDD	VDD	VDD	VSS	VSS	A1[14]	VSS	VSS
H	A0[9]	A0[11]	VSS	VSS	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VSS	VSS	A0[3]	R0_L	NC	NC	NC	NC	W1_L	A1[4]	VSS	VSS	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VSS	VSS	VSS	VSS	
J	A0[7]	NC	NC	NC	NC	NC	NC	VDDQ_Q	NC	NC	NC	NC	NC	NC	A0[5]	NC	NC	NC	NC	A1[19]	D1[9]	D1[10]	Q1[10]	Q1[11]	D1[12]	Q1[13]	VDDQ_Q	D1[14]	Q1[14]	D1[15]	DP1[0]	QP1[0]	RSVD	VSS	
K	IC0[0]	D0[0]	NC	Q0[1]	NC	D0[3]	Q0[4]	Q0R0R EF0	NC	NC	D0[6]	NC	Q0[7]	NC	NC/A0 [20]	NC	NC	NC	NC	NC/A1 [24]	Q0[9]	NC	D1[11]	NC	Q1[12]	D1[13]	Q0R1R EF1	NC	NC	Q1[15]	NC	DP1[1]	NC	VSS	
L	NC	Q0[0]	D0[1]	D0[2]	Q0[2]	Q0[3]	D0[4]	NC	D0[5]	Q0[5]	Q0[6]	D0[7]	D0[8]	Q0[8]	CQ0	NC	NC	NC	NC	CQ1_L	NC	NC	NC	NC	NC	NC	DOF1_L	NC	NC	NC	NC	NC	NC	NC	
M	EINTR	RSVD	RSVD	RSVD	NSERE F1	NSERE F2	NC	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	HIGH_S PEEDI_L	VSS	VDDQ_Q	VDDQ_Q	VDDQ_Q	SRAMR EF	NC	NC	NC	NC	
N	SSV	SSF	SSSV	SSSF	VDDQ_Q	VDDQ_Q	NC	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	INT_VD D	NC	NC	VDDQ_Q	VDDQ_Q	AD_SD ATA[7]	AD_SD ATA[6]	AD_SD ATA[15]	AD_SD ATA[14]	
P	RSVD	RSVD	NC	NC	VDDQ_Q	VDDQ_Q	NC	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	NC	NC	VDDQ_Q	VDDQ_Q	AD_SD ATA[5]	AD_SD ATA[4]	AD_SD ATA[13]	AD_SD ATA[12]	
R	INDEX[22]	INDEX[23]	SINDE X[23]	SINDE X[22]	VSS	VSS	INT_VD D	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	NC	INT_VD D	VSS	VSS	AD_SD ATA[3]	AD_SD ATA[2]	AD_SD ATA[11]	AD_SD ATA[10]	
T	INDEX[21]	INDEX[20]	SINDE X[21]	SINDE X[20]	VSS	VSS	INT_VD D	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	NC	INT_VD D	VSS	VSS	AD_SD ATA[1]	AD_SD ATA[0]	AD_SD ATA[9]	AD_SD ATA[8]	
U	INDEX[19]	INDEX[18]	SINDE X[19]	SINDE X[18]	VDDQ_Q	VDDQ_Q	NC	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	INT_VD D	NC	NC	VDDQ_Q	VDDQ_Q	AD_SD ATA[1]	AD_SD ATA[0]	AD_SD ATA[23]	AD_SD ATA[22]	
V	INDEX[17]	INDEX[16]	SINDE X[17]	SINDE X[16]	VDDQ_Q	VDDQ_Q	NC	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	INT_VD D	NC	NC	VDDQ_Q	VDDQ_Q	AD_SA DR[15]	AD_SA DR[14]	AD_SA DR[19]	AD_SA DR[18]	
W	INDEX[15]	INDEX[14]	SINDE X[15]	SINDE X[14]	VSS	VSS	INT_VD D	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	NC	INT_VD D	VSS	VSS	AD_SA DR[7]	AD_SA DR[6]	AD_SA DR[13]	AD_SA DR[12]	
Y	INDEX[13]	INDEX[12]	SINDE X[13]	SINDE X[12]	VSS	VSS	INT_VD D	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	INT_VD D	NC	INT_VD D	VSS	VSS	AD_SA DR[3]	AD_SA DR[2]	AD_SA DR[5]	AD_SA DR[4]	
AA	INDEX[11]	INDEX[10]	SINDE X[11]	SINDE X[10]	VDDQ_Q	VDDQ_Q	NC	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	NC	NC	VDDQ_Q	VDDQ_Q	AD_SA DR[1]	AD_SA DR[0]	NC	NC	
AB	INDEX[9]	INDEX[8]	SINDE X[9]	SINDE X[8]	VSS	VSS	INT_VD D	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	INT_VD D	NC	NC	VDDQ_Q	VDDQ_Q	AD_SA DR[2]	AD_SA DR[1]	NC	NC	
AC	INDEX[7]	INDEX[6]	SINDE X[7]	SINDE X[6]	VSS	VSS	INT_VD D	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	INT_VD D	NC	INT_VD D	VSS	VSS	AD_SA DR[6]	AD_SA DR[5]	AD_SA DR[10]	AD_SA DR[9]	
AD	INDEX[5]	INDEX[4]	SINDE X[5]	SINDE X[4]	VSS	VSS	INT_VD D	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	INT_VD D	NC	INT_VD D	VSS	VSS	AD_SA DR[14]	AD_SA DR[13]	AD_SA DR[18]	AD_SA DR[17]	
AE	INDEX[3]	INDEX[2]	SINDE X[3]	SINDE X[2]	VDDQ_Q	VDDQ_Q	NC	NC	NC	NC	NC	NC	NC	NC	INT_VS S	INT_VS S	INT_VS S	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	VDDQ_Q	VDDQ_Q	AD_SD ATAP[3]	AD_SD ATAP[2]	NC	AD_SD ATAP[1]	
AF	INDEX[1]	INDEX[0]	SINDE X[1]	SINDE X[0]	VDDQ_Q	VDDQ_Q	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	VDDQ_Q	VDDQ_Q	AD_SD ATAP[1]	AD_SD ATAP[0]	AD_SD ATAP[16]	AD_SD ATAP[15]	
AG	VDDQ_Q	CM0[1]	VDDQ_Q	NC	VSS	VSS	INT_VD D	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	INT_VD D	VSS	VSS	AD_SD ATAP[1]	AD_SD ATAP[0]	AD_SD ATAP[17]	AD_SD ATAP[16]
AH	CM0[9]	CM0[8]	SCMD0V	NC	VSS	VSS	INT_VD D	NC	NC	NC	INT_VD D	INT_VD D	NC	NC	INT_VD D	INT_VD D	NC	NC	INT_VD D	INT_VD D	NC	NC	INT_VD D	INT_VD D	NC	NC	NC	NC	INT_VD D	VSS	VSS	AD_SD ATAP[1]	AD_SD ATAP[0]	AD_SD ATAP[18]	AD_SD ATAP[17]
AJ	CM0[7]	CM0[6]	RSVD	VDDQ_Q	VSS	VSS	VSS	VSS	VDDQ_Q	VDDQ_Q	VSS	VSS	VDDQ_Q	VDDQ_Q	VSS	VSS	VDDQ_Q	VDDQ_Q	VSS	VSS	VDDQ_Q	VDDQ_Q	VSS	VSS	VDDQ_Q	VDDQ_Q	VSS	VSS	VSS	VSS	VSS	VSS	NSERE F3	AD_SD ATAP[1]	AD_SD ATAP[0]
AK	CM0[5]	CM0[4]	RSVD	VDDQ_Q	VSS	VSS	VSS	VSS	VDDQ_Q	VDDQ_Q	VSS	VSS	VDDQ_Q	VDDQ_Q	VSS	VSS	VDDQ_Q	VDDQ_Q	VSS	VSS	VDDQ_Q	VDDQ_Q	VSS	VSS	VDDQ_Q	VDDQ_Q	VSS	VSS	VSS	VSS	VSS	VSS	SRAMS EL	AD_SD ATAP[1]	AD_SD ATAP[0]
AL	CM0[3]	CM0[2]	HS_PW RSARE	VDDQ_Q	VDDQ_Q	VSS	VSS	DQ[3]	DQ[7]	DQ[11]	DQ[15]	DQ[19]	DQ[23]	DQ[27]	DQ[31]	DQ[35]	DQ[39]	DQ[43]	DQ[47]	DQ[51]	DQ[55]	DQ[59]	DQ[63]	DQ[67]	DQ[71]	DQ[75]	DQ[79]	DQ[83]	DQ[87]	DQ[91]	DQ[95]	DQ[99]	NSERE F4	AD_SD ATAP[1]	AD_SD ATAP[0]
AM	CM0[1]	CM0[0]	VDDQ_Q	RULL_N	NC	PAR[1]	DQ[1]	DQ[5]	DQ[9]	DQ[13]	DQ[17]	DQ[21]	DQ[25]	DQ[29]	DQ[33]	DQ[37]	DQ[41]	DQ[45]	DQ[49]	DQ[53]	DQ[57]	DQ[61]	DQ[65]	DQ[69]	TDI	TMS	TCK	TRST*	TDO	BH[2]	BH[3]	BH[4]	RULL[1]	RULL[0]	
AN	CM0V	VDDQ_Q	SPARE RR_L	PHS_O UT_L	VDDQ_Q	PARER R_L	DQ[2]	DQ[6]	DQ[10]	DQ[14]	DQ[18]	DQ[22]	DQ[26]	DQ[30]	DQ[34]	DQ[38]	DQ[42]	DQ[46]	DQ[50]	DQ[54]	DQ[58]	DQ[62]	DQ[66]	DQ[70]	LH[0]	LH[1]	LH[2]	LH[3]	LH[4]	LH[5]	LH[6]	LH[7]	BH[5]	BH[6]	RULL[2]
AP	no ball	TERM	RULL_O UT	ACK	RSVD	PAR[0]	DQ[0]	DQ[4]	DQ[8]	DQ[12]	DQ[16]	DQ[20]	DQ[24]	DQ[28]	DQ[32]	DQ[36]	DQ[40]	DQ[44]	DQ[48]	DQ[52]	DQ[56]	DQ[60]	DQ[64]	DQ[68]	RSVD	LH[1]	LH[2]	LH[3]	LH[4]	LH[5]	LH[6]	LH[7]	BH[8]	BH[9]	no ball

Figure 30. CYNSE20512 Dual LA-1 Port Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	
A	n o ba ll	NC	NC	NC	NC	NC	NC	DORF L	NC	NC	NC	NC	NC	NC	CQ0_L	E0[0]	CLK	VSS	VSS	RSVD	RSVD	VSS	VSS	RSVD	RSVD	VSS	NC	VSS	RSVD	RSVD	VSS	VSS	RSVD	n o ba ll	
B	IFC0[1]	NC	DP0[1]	NC	Q0[15]	NC	NC	QORR EFL	D0[13]	Q0[12]	NC	D0[11]	NC	Q0[9]	NC/A0 [21]	E0[1]	CLK_M ODE	RST_L	VSS	NC	NC	RSVD	NC	VSS	NC	NC	QORR ER0	RSVD	VSS	NC	RSVD	NC	VSS	VSS	
C	A0[6]	Q0[1]	Q0[0]	DP0[0]	D0[15]	Q0[14]	D0[14]	VDDQ Q	Q0[13]	D0[12]	Q0[11]	Q0[10]	D0[10]	D0[9]	A0[19]	EP0[0]	RA0	RSVD	VDDQ Q	VSS	NC	NC	NC	NC	NC	NC	VDDQ Q	NC	NC	NC	NC	NC	VSS		
D	A0[8]	A0[10]	VSS_PL L	VSS	VDDQ Q	VDDQ Q	VDDQ Q	VDDQ Q	VDDQ Q	VDDQ Q	VDDQ Q	VSS	VSS	A0[4]	W0_L	EP0[1]	NC	NC	VDDQ Q	VDDQ Q	VSS	VSS	VSS	VDDQ Q	VDDQ Q	VDDQ Q	VDDQ Q	VDDQ Q	VDDQ Q	VDDQ Q	VSS	VSS	VSS	VSS	
E	A0[18]	A0[16]	A0[14]	VSS	VSS	VDD_PL L	VDD	VDD	VDD	VDD	VSS	A0[2]	NC	BW0_L [1]	RSVD	NC	NC	RSVD	NC	VDDQ Q	VSS	VSS	VSS	VSS	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS		
F	C0_L	C0	A0[12]	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	A0[0]	K0	K0_L	TEST_ PB	NC	RSVD	RSVD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS		
G	A0[17]	A0[15]	A0[13]	VSS	VSS	VDD	VDD	VDD	VDD	VDD	VSS	VSS	A0[1]	BW0_L [0]	NC	RSVD	NC	NC	RSVD	VDDQ Q	NC	VSS	VSS	VSS	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS		
H	A0[9]	A0[11]	VSS	VSS	VDDQ Q	VDDQ Q	VDDQ Q	VDDQ Q	VDDQ Q	VDDQ Q	VSS	VSS	A0[3]	R0_L	NC	NC	NC	NC	NC	VDDQ Q	VSS	VSS	VSS	VDDQ Q	VDDQ Q	VDDQ Q	VDDQ Q	VDDQ Q	VDDQ Q	VDDQ Q	VSS	VSS	VSS	VSS	
J	A0[7]	NC	NC	NC	NC	NC	NC	VDDQ Q	NC	NC	NC	NC	NC	A0[5]	NC	NC	NC	NC	VSS	VSS	VSS	RSVD	RSVD	VSS	RSVD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	RSVD	RSVD	
K	IFC0[0]	D0[0]	NC	Q0[1]	NC	D0[3]	Q0[4]	QORR ER0	NC	NC	D0[6]	NC	Q0[7]	NC	NC/A0 [20]	NC	NC	NC	NC	NC	RSVD	NC	VSS	NC	RSVD	VSS	QORR ER1	NC	NC	RSVD	VSS	VSS	NC	VSS	
L	NC	Q0[0]	D0[1]	D0[2]	Q0[2]	Q0[3]	D0[4]	NC	D0[5]	Q0[5]	Q0[6]	D0[7]	D0[8]	Q0[8]	CQ0	NC	NC	NC	NC	RSVD	NC	NC	NC	NC	NC	NC	VSS	NC	NC	NC	NC	NC	NC		
M	EINTR	RSVD	RSVD	RSVD	NSERE F1	NSERE F2	NC	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	HIGH_S PEEDI_	VSS	VDDQ_J	VSS	VDDQ_J	SRAMR EF	NC	NC	NC	NC
N	SSV	SSF	SSSV	SSSF	VDDQ A	VDDQ A	NC	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	INT_VD D	NC	NC	VDDQ S	VDDQ S	AD_SA ATA[7]	AD_SA ATA[6]	AD_SA ATA[15]	AD_SA ATA[14]	
P	RSVD	RSVD	NC	NC	VDDQ A	VDDQ A	NC	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	NC	NC	VDDQ S	VDDQ S	AD_SA ATA[5]	AD_SA ATA[4]	AD_SA ATA[13]	AD_SA ATA[12]	
R	INDEX[23]	INDEX[22]	SINDE X[23]	SINDE X[22]	VSS	VSS	INT_VD D	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	NC	INT_VD D	VSS	VSS	AD_SA ATA[3]	AD_SA ATA[2]	AD_SA ATA[11]	AD_SA ATA[10]	
T	INDEX[21]	INDEX[20]	SINDE X[21]	SINDE X[20]	VSS	VSS	INT_VD D	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	NC	INT_VD D	VSS	VSS	AD_SA ATA[1]	AD_SA ATA[0]	AD_SA ATA[9]	AD_SA ATA[8]	
U	INDEX[19]	INDEX[18]	SINDE X[19]	SINDE X[18]	VDDQ A	VDDQ A	NC	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	INT_VD D	NC	NC	VDDQ S	VDDQ S	AD_SA ATA[P]	AD_SA ATA[P]	AD_SA ATA[23]	AD_SA ATA[21]	
V	INDEX[17]	INDEX[16]	SINDE X[17]	SINDE X[16]	VDDQ A	VDDQ A	NC	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	INT_VD D	NC	NC	VDDQ S	VDDQ S	AD_SA ATA[15]	AD_SA ATA[14]	AD_SA ATA[13]	AD_SA ATA[12]	
W	INDEX[15]	INDEX[14]	SINDE X[15]	SINDE X[14]	VSS	VSS	INT_VD D	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	NC	INT_VD D	VSS	VSS	AD_SA ATA[15]	AD_SA ATA[14]	AD_SA ATA[13]	AD_SA ATA[12]	
Y	INDEX[13]	INDEX[12]	SINDE X[13]	SINDE X[12]	VSS	VSS	INT_VD D	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	INT_VD D	NC	NC	INT_VD D	VSS	VSS	AD_SA ATA[15]	AD_SA ATA[14]	AD_SA ATA[13]	AD_SA ATA[12]
AA	INDEX[11]	INDEX[10]	SINDE X[11]	SINDE X[10]	NSERE R0	VDDQ A	NC	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	NC	NC	VDDQ S	VDDQ S	AD_SA ATA[15]	AD_SA ATA[14]	AD_SA ATA[13]	AD_SA ATA[12]	
AB	INDEX[9]	INDEX[8]	SINDE X[9]	SINDE X[8]	NSERE F4	VDDQ A	NC	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	INT_VD D	NC	NC	VDDQ S	VDDQ S	AD_SA ATA[15]	AD_SA ATA[14]	AD_SA ATA[13]	AD_SA ATA[12]	
AC	INDEX[7]	INDEX[6]	SINDE X[7]	SINDE X[6]	VSS	VSS	INT_VD D	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	INT_VD D	NC	NC	INT_VD D	VSS	VSS	AD_SA ATA[15]	AD_SA ATA[14]	AD_SA ATA[13]	AD_SA ATA[12]
AD	INDEX[5]	INDEX[4]	SINDE X[5]	SINDE X[4]	VSS	VSS	INT_VD D	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	INT_VD D	NC	NC	INT_VD D	VSS	VSS	AD_SA ATA[15]	AD_SA ATA[14]	AD_SA ATA[13]	AD_SA ATA[12]
AE	INDEX[3]	INDEX[2]	SINDE X[3]	SINDE X[2]	VDDQ A	VDDQ A	NC	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	INT_VD D	NC	NC	VDDQ S	VDDQ S	AD_SA ATA[15]	AD_SA ATA[14]	AD_SA ATA[13]	AD_SA ATA[12]	
AF	VDDQ_ A	CMQ[1 0]	VDDQ_ A	NC	VSS	VSS	INT_VD D	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	VDDQ S	VDDQ S	AD_SA ATA[15]	AD_SA ATA[14]	AD_SA ATA[13]	AD_SA ATA[12]	
AG	CMQ[8 0]	VDDQ_ A	NC	VSS	VSS	INT_VD D	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	VDDQ S	VDDQ S	AD_SA ATA[15]	AD_SA ATA[14]	AD_SA ATA[13]	AD_SA ATA[12]	
AH	CMQ[9 1]	CMQ[8 0]	NC	VSS	VSS	INT_VD D	NC	NC	NC	INT_VD D	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	VDDQ S	VDDQ S	AD_SA ATA[15]	AD_SA ATA[14]	AD_SA ATA[13]	AD_SA ATA[12]
AJ	CMQ[7 1]	CMQ[6 0]	RSVD	VDDQ_ A	VSS	VSS	VSS	VSS	VDDQ_ A	VDDQ_ A	VSS	VSS	VDDQ_ A	VDDQ_ A	VSS	VSS	VDDQ_ A	VDDQ_ A	VSS	VSS	VDDQ_ A	VDDQ_ A	VSS	VSS	VDDQ_ A	VDDQ_ A	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	
AK	CMQ[5 1]	CMQ[4 0]	RSVD	VDDQ_ A	VDDQ_ A	VSS	VSS	VSS	VDDQ_ A	VDDQ_ A	VSS	VSS	VDDQ_ A	VDDQ_ A	VSS	VSS	VDDQ_ A	VDDQ_ A	VSS	VSS	VDDQ_ A	VDDQ_ A	VSS	VSS	VDDQ_ A	VDDQ_ A	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	
AL	CMQ[3 1]	CMQ[2 0]	HS_PW RSAVE	VDDQ_ A	VDDQ_ A	VDDQ_ A	DQ[3]	DQ[7]	DQ[11]	DQ[15]	DQ[19]	DQ[23]	DQ[27]	DQ[31]	DQ[35]	DQ[39]	DQ[43]	DQ[47]	DQ[51]	DQ[55]	DQ[59]	DQ[63]	DQ[67]	DQ[71]	DQ[75]	DQ[79]	DQ[83]	DQ[87]	DQ[91]	DQ[95]	DQ[99]	DQ[103]	DQ[107]		
AM	CMQ[1 1]	CMQ[0 0]	VDDQ_ A	RULL_N	NC	PAR[1]	DQ[4]	DQ[8]	DQ[12]	DQ[16]	DQ[20]	DQ[24]	DQ[28]	DQ[32]	DQ[36]	DQ[40]	DQ[44]	DQ[48]	DQ[52]	DQ[56]	DQ[60]	DQ[64]	DQ[68]	DQ[72]	DQ[76]	DQ[80]	DQ[84]	DQ[88]	DQ[92]	DQ[96]	DQ[100]	DQ[104]	DQ[108]		
AN	CMQ[0 1]	CMQ[0 0]	SIPARE RR_L	VDDQ_ A	VDDQ_ A	VDDQ_ A	DQ[2]	DQ[6]	DQ[10]	DQ[14]	DQ[18]	DQ[22]	DQ[26]	DQ[30]	DQ[34]	DQ[38]	DQ[42]	DQ[46]	DQ[50]	DQ[54]	DQ[58]	DQ[62]	DQ[66]	DQ[70]	DQ[74]	DQ[78]	DQ[82]	DQ[86]	DQ[90]	DQ[94]	DQ[98]	DQ[102]	DQ[106]		
AP	n o ba ll	TERM	ACK	RSVD	PAR[0]	DQ[0]	DQ[4]	DQ[8]	DQ[12]	DQ[16]	DQ[20]	DQ[24]	DQ[28]	DQ[32]	DQ[36]	DQ[40]	DQ[44]	DQ[48]	DQ[52]	DQ[56]	DQ[60]	DQ[64]	DQ[68]	DQ[72]	DQ[76]	DQ[80]	DQ[84]	DQ[88]	DQ[92]	DQ[96]	DQ[100]	DQ[104]	DQ[108]		

Figure 31. CYNSE20512 Single LA-1 Port Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
A	no bal (NC)	NC	NC	NC	NC	NC	NC	DOFRL	NC	NC	NC	NC	NC	NC	CQ0_L	E0[0]	CLK	VSS	E[0]	CQ1	Q[8]	D[8]	D[7]	Q[6]	Q[5]	D[5]	NC	D[4]	Q[3]	Q[2]	D[2]	D[1]	Q[0]	no bal (NC)
B	IFC[0]	1	NC	DP0[1]	NC	Q0[15]	NC	Q0R0R EFL	D0[13]	Q0[12]	NC	D0[11]	NC	Q0[9]	NC/ A0 [2]	E0[1]	CLK_M ODE	RST_L	E[1]	NC/ A[1 20]	NC	Q[7]	NC	D[6]	NC	NC	Q0R1R EFL	Q[4]	D[3]	NC	Q[4]	NC	D[0]	IFC[0]
C	A0[6]	Q0[1]	Q0[0]	DP0[0]	D0[15]	Q0[14]	D0[14]	VDDQ_Q	Q0[13]	D0[12]	Q0[11]	Q0[10]	D0[10]	D0[9]	A0[19]	EP0[0]	RA0	RA1	EP[0]	A[5]	NC	NC	NC	NC	NC	NC	VDDQ_Q	NC	NC	NC	NC	NC	A[7]	
D	A0[8]	A0[10]	VSS_PL L	VSS	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VSS	VSS	A0[4]	W0_L	EP0[1]	NC	NC	EP[1]	R1_L	A[3]	VSS	VSS	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VSS	VSS	A[1]	A[9]
E	A0[18]	A0[16]	A0[14]	VSS	VSS	VDD_PL L	VDD	VDD	VDD	VDD	VSS	VSS	A0[2]	NC	BW0_L [1]	RSVD	NC	NC	RSVD	NC	BW1_L [2]	A[1]	VSS	VSS	VDD	VDD	VDD	VDD	VDD	VSS	VSS	A[13]	A[15]	A[17]
F	C0_L	C0	A0[12]	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	A0[0]	K0	K0_L	TEST_PB	NC	RSVD	RSVD	K1_L	K1	A[0]	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	A[12]	C1	C1_L
G	A0[17]	A0[15]	A0[13]	VSS	VSS	VDD	VDD	VDD	VDD	VDD	VSS	VSS	A0[1]	BW0_L [0]	NC	RSVD	NC	NC	RSVD	BW1_L [1]	NC	A[2]	VSS	VSS	VDD	VDD	VDD	VDD	VDD	VSS	VSS	A[14]	A[16]	A[18]
H	A0[9]	A0[11]	VSS	VSS	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VSS	VSS	A0[3]	R0_L	NC	NC	NC	NC	W1_L	A[4]	VSS	VSS	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VSS	VSS	A[10]	A[8]
J	A0[7]	NC	NC	NC	NC	NC	NC	VDDQ_Q	NC	NC	NC	NC	NC	NC	A0[5]	NC	NC	NC	NC	A[19]	D[9]	D[10]	Q[10]	Q[11]	D[12]	Q[13]	VDDQ_Q	D[14]	Q[14]	D[15]	DP[0]	QP[0]	QP[1]	A[6]
K	IFC[0]	1	D0[0]	NC	Q0[1]	NC	D0[3]	Q0[4]	Q0R0R EFL	NC	NC	D0[6]	NC	Q0[7]	NC	NC/ A0 [20]	NC	NC	NC	NC/ A[1 21]	Q[9]	NC	D[11]	NC	Q[12]	D[13]	Q0R1R EFL	NC	NC	Q[15]	NC	DP[1]	NC	IFC[1]
L	NC	Q0[0]	D0[1]	D0[2]	Q0[2]	Q0[3]	D0[4]	NC	D0[5]	Q0[5]	Q0[6]	D0[7]	D0[8]	Q0[9]	CQ0	NC	NC	NC	NC	CQ1_L	NC	NC	NC	NC	NC	NC	DOFRL	NC	NC	NC	NC	NC	NC	
M	EINTR	RSVD	RSVD	RSVD	NSERE F1	NSERE F2	NC	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	HIGH_S PEED	VDDQ_Q	VSS	VDDQ_Q	VDDQ_Q	SRAMR EF	NC	NC	NC	NC
N	SSV	SSF	SSSV	SSSF	VDDQ_A	VDDQ_A	NC	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	INT_VD D	NC	NC	VDDQ_S	VDDQ_S	AD_SD ATA[7]	AD_SD ATA[6]	AD_SD ATA[15]	AD_SD ATA[14]
P	RSVD	RSVD	NC	NC	VDDQ_A	VDDQ_A	NC	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	NC	NC	VDDQ_S	VDDQ_S	AD_SD ATA[5]	AD_SD ATA[4]	AD_SD ATA[13]	AD_SD ATA[12]
R	INDEX[23]	INDEX[22]	SINDE X[23]	SINDE X[22]	VSS	VSS	INT_VD D	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	NC	INT_VD D	VSS	VSS	AD_SD ATA[3]	AD_SD ATA[2]	AD_SD ATA[11]	AD_SD ATA[10]
T	INDEX[21]	INDEX[20]	SINDE X[21]	SINDE X[20]	VSS	VSS	INT_VD D	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	NC	INT_VD D	VSS	VSS	AD_SD ATA[1]	AD_SD ATA[0]	AD_SD ATA[9]	AD_SD ATA[8]	
U	INDEX[19]	INDEX[18]	SINDE X[19]	SINDE X[18]	VDDQ_A	VDDQ_A	NC	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	INT_VD D	NC	NC	VDDQ_S	VDDQ_S	AD_SD AD_SA DR[3]	NC	AD_SD AD_SA DR[2]	
V	INDEX[17]	INDEX[16]	SINDE X[17]	SINDE X[16]	VDDQ_A	VDDQ_A	NC	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	INT_VD D	NC	NC	VDDQ_S	VDDQ_S	AD_SA DR[15]	AD_SA DR[17]	AD_SA DR[19]	AD_SA DR[21]
W	INDEX[15]	INDEX[14]	SINDE X[15]	SINDE X[14]	VSS	VSS	INT_VD D	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	NC	INT_VD D	VSS	VSS	AD_SA DR[7]	AD_SA DR[9]	AD_SA DR[11]	AD_SA DR[13]	
Y	INDEX[13]	INDEX[12]	SINDE X[13]	SINDE X[12]	VSS	VSS	INT_VD D	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	INT_VD D	NC	INT_VD D	VSS	VSS	AD_SA DR[3]	AD_SA DR[5]	AD_SA DR[7]	AD_SA DR[9]	
AA	INDEX[11]	INDEX[10]	SINDE X[11]	SINDE X[10]	NSERE R0	VDDQ_A	NC	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	NC	NC	VDDQ_S	VDDQ_S	AD_SA DR[1]	AD_SA DR[3]	NC	NC	
AB	INDEX[9]	INDEX[8]	SINDE X[9]	SINDE X[8]	NSERE F4	VDDQ_A	NC	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	INT_VD D	NC	NC	VDDQ_S	VDDQ_S	AD_SA DR[2]	AD_SA DR[4]	NC	NC	
AC	INDEX[7]	INDEX[6]	SINDE X[7]	SINDE X[6]	VSS	VSS	INT_VD D	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	INT_VD D	NC	INT_VD D	VSS	VSS	AD_SA DR[6]	AD_SA DR[8]	AD_SA DR[10]	AD_SA DR[12]	
AD	INDEX[5]	INDEX[4]	SINDE X[5]	SINDE X[4]	VSS	VSS	INT_VD D	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	INT_VD D	NC	INT_VD D	VSS	VSS	AD_SA DR[14]	AD_SA DR[16]	AD_SA DR[18]	AD_SA DR[20]	
AE	INDEX[3]	INDEX[2]	SINDE X[3]	SINDE X[2]	VDDQ_A	VDDQ_A	NC	NC	NC	NC	NC	NC	NC	NC	INT_VS S	INT_VS S	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	VDDQ_S	VDDQ_S	AD_SD AD_SA DR[22]	NC	AD_SD AD_SA DR[21]		
AF	INDEX[1]	INDEX[0]	SINDE X[1]	SINDE X[0]	VDDQ_A	VDDQ_A	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	VDDQ_S	VDDQ_S	AD_SD AD_SA DR[2]	AD_SD AD_SA DR[1]	AD_SD AD_SA DR[0]		
AG	VDDQ_A	CM[0]	CM[1]	CM[2]	NC	VSS	VSS	INT_VD D	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	INT_VD D	VSS	VSS	AD_SD AD_SA DR[18]	AD_SD AD_SA DR[19]	AD_SD AD_SA DR[20]		
AH	CM[9]	CM[8]	SCMDV	NC	VSS	VSS	INT_VD D	NC	NC	NC	INT_VD D	INT_VD D	NC	NC	INT_VD D	INT_VD D	NC	NC	INT_VD D	INT_VD D	NC	NC	INT_VD D	INT_VD D	NC	NC	NC	INT_VD D	VSS	VSS	AD_SD AD_SA DR[21]	AD_SD AD_SA DR[22]	AD_SD AD_SA DR[23]	
AJ	CM[7]	CM[6]	RSVD	VDDQ_A	VSS	VSS	VSS	VSS	VDDQ_A	VDDQ_A	VSS	VSS	VDDQ_A	VDDQ_A	VSS	VSS	VDDQ_A	VDDQ_A	VSS	VSS	VDDQ_A	VDDQ_A	VSS	VSS	VDDQ_A	VDDQ_A	VSS	VSS	VSS	VSS	NSERE F3	AD_SD AD_SA DR[24]	AD_SD AD_SA DR[25]	
AK	CM[5]	CM[4]	RSVD	VDDQ_A	VDDQ_A	VSS	VSS	VSS	VDDQ_A	VDDQ_A	VSS	VSS	VDDQ_A	VDDQ_A	VSS	VSS	VDDQ_A	VDDQ_A	VSS	VSS	VDDQ_A	VDDQ_A	VSS	VSS	VDDQ_A	VDDQ_A	VSS	VSS	VDDQ_A	VDDQ_A	SRAMS L	AD_SA DR[26]	AD_SA DR[27]	
AL	CM[3]	CM[2]	HS_PW RSARE	VDDQ_A	VDDQ_A	VSS	VSS	VSS	VDDQ_A	VDDQ_A	VSS	VSS	VDDQ_A	VDDQ_A	VSS	VSS	VDDQ_A	VDDQ_A	VSS	VSS	VDDQ_A	VDDQ_A	VSS	VSS	VDDQ_A	VDDQ_A	VSS	VSS	VDDQ_A	VDDQ_A	NSESE L	AD_SA DR[28]	AD_SA DR[29]	
AM	CM[1]	CM[0]	RULL_N	NC	PAR[1]	DQ[1]	DQ[5]	DQ[9]	DQ[13]	DQ[17]	DQ[21]	DQ[25]	DQ[29]	DQ[33]	DQ[37]	DQ[41]	DQ[45]	DQ[49]	DQ[53]	DQ[57]	DQ[61]	DQ[65]	DQ[69]	T0I	TMS	TCK	TRST	TDO	B[16]	B[17]	B[18]	B[19]		
AN	CM[0]	VDDQ_A	SPARE RR_L	PHS_O UT_L	VDDQ_A	PARER_R_L	DQ[2]	DQ[6]	DQ[10]	DQ[14]	DQ[18]	DQ[22]	DQ[26]	DQ[30]	DQ[34]	DQ[38]	DQ[42]	DQ[46]	DQ[50]	DQ[54]	DQ[58]	DQ[62]	DQ[66]	DQ[70]	LH[0]	LH[1]	LH[2]	LH[3]	LH[4]	LH[5]	LH[6]	LH[7]		
AP	no bal (NC)	TERM	RULL_O UT	ACK	RSVD	PAR[0]	DQ[0]	DQ[4]	DQ[8]	DQ[12]	DQ[16]	DQ[20]	DQ[24]	DQ[28]	DQ[32]	DQ[36]	DQ[40]	DQ[44]	DQ[48]	DQ[52]	DQ[56]	DQ[60]	DQ[64]	DQ[68]	RSVD	LH[1]	LH[2]	LH[3]	LH[4]	LH[5]	LH[6]	LH[7]	no bal (NC)	

Figure 32. CYNSE2056 Dual LA-1 Port Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	
A	n o ball	NC	NC	NC	NC	NC	NC	DOH0_L QDRR EF1	NC	NC	NC	NC	NC	NC	CQ0_L E0[0]	CLK	VSS	VSS	RSVD	RSVD	VSS	VSS	RSVD	RSVD	VSS	NC	VSS	RSVD	RSVD	VSS	VSS	RSVD	RSVD	n o ball	
B	IFC0[1]	NC	DP0[1]	NC	Q0[15]	NC	NC	Q0[13]	Q0[12]	NC	D0[11]	NC	Q0[9]	NC/A0 [2]	E0[1]	CLK_M ODE	RST_L	VSS	NC	NC	RSVD	NC	VSS	NC	NC	QDRR EF0	RSVD	VSS	NC	RSVD	NC	VSS	VSS		
C	A0[6]	Q0[1]	Q0[0]	DP0[0]	D0[15]	Q0[14]	D0[14]	Q0[13]	D0[12]	Q0[11]	Q0[10]	D0[10]	D0[9]	A0[19]	EP0[0]	RA0	RSVD	VDDQ_Q	VSS	NC	NC	NC	NC	NC	NC	VDDQ_Q	NC	NC	NC	NC	NC	NC	VSS		
D	A0[8]	A0[10]	VSS_PL L	VSS	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VSS	VSS	A0[4]	W0_L	EP0[1]	NC	NC	VDDQ_Q	VDDQ_Q	VSS	VSS	VSS	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VSS	VSS	VSS	VSS		
E	A0[18]	A0[16]	A0[14]	VSS	VSS	VDD_PL L	VDD	VDD	VDD	VSS	VSS	A0[2]	NC	BW0_L [1]	RSVD	NC	NC	RSVD	NC	VSS	VSS	VSS	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS			
F	C0_L	C0	A0[12]	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	A0[0]	K0	K0_L	TEST_P B	NC	RSVD	RSVD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS		
G	A0[17]	A0[15]	A0[13]	VSS	VSS	VDD	VDD	VDD	VDD	VSS	VSS	A0[1]	BW0_L [8]	NC	RSVD	NC	NC	RSVD	VDDQ_Q	NC	VSS	VSS	VSS	VSS	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS		
H	A0[9]	A0[11]	VSS	VSS	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VSS	VSS	A0[3]	R0_L	NC	NC	NC	NC	VDDQ_Q	VSS	VSS	VSS	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VDDQ_Q	VSS	VSS	VSS	VSS		
J	A0[7]	NC	NC	NC	NC	NC	NC	VDDQ_Q	NC	NC	NC	NC	NC	A0[5]	NC	NC	NC	NC	VSS	VSS	VSS	RSVD	RSVD	VSS	RSVD	VSS	VSS	VSS	VSS	VSS	RSVD	RSVD	VSS		
K	IFC0[0]	D0[0]	NC	Q0[1]	NC	D0[3]	Q0[4]	QDRR EF0	NC	NC	D0[6]	NC	Q0[7]	NC	NC/A0 [20]	NC	NC	NC	NC	NC	RSVD	NC	VSS	NC	RSVD	VSS	QDRR EF1	NC	NC	RSVD	NC	VSS	NC	VSS	
L	NC	Q0[0]	D0[1]	D0[2]	Q0[2]	Q0[3]	D0[4]	NC	D0[5]	Q0[5]	Q0[6]	D0[7]	D0[8]	Q0[8]	CQ0	NC	NC	NC	NC	RSVD	NC	NC	NC	NC	NC	NC	VSS	NC	NC	NC	NC	NC	NC		
M	INTR	RSVD	RSVD	RSVD	NSERE F1	NSERE F2	NC	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	HIGH_S PEEDI_	VDDQ_J	VSS	VSS	VDDQ_J	SRAMR EF	NC	NC	NC	NC	
N	SSV	SSF	SSSV	SSSF	VDDQ_Q	VDDQ_Q	NC	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	INT_VD D	NC	NC	VDDQ_S	AD_SA ATA[7]	AD_SA ATA[6]	AD_SA ATA[15]	AD_SA ATA[14]		
P	RSVD	RSVD	NC	NC	VDDQ_Q	VDDQ_Q	NC	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	NC	NC	VDDQ_S	AD_SA ATA[5]	AD_SA ATA[4]	AD_SA ATA[13]	AD_SA ATA[12]		
R	INDEX[23]	INDEX[22]	SINDE X[23]	SINDE X[22]	VSS	VSS	INT_VD D	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	NC	INT_VD D	VSS	VSS	AD_SA ATA[3]	AD_SA ATA[2]	AD_SA ATA[11]	AD_SA ATA[10]	
T	INDEX[21]	INDEX[20]	SINDE X[21]	SINDE X[20]	VSS	VSS	INT_VD D	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	NC	INT_VD D	VSS	VSS	AD_SA ATA[1]	AD_SA ATA[0]	AD_SA ATA[9]	AD_SA ATA[8]	
U	INDEX[19]	INDEX[18]	SINDE X[19]	SINDE X[18]	VDDQ_Q	VDDQ_Q	NC	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	INT_VD D	NC	NC	VDDQ_S	VDDQ_S	AD_SA ATA[1]	AD_SA DR[23]	NC	AD_SA ATA[1]		
V	INDEX[17]	INDEX[16]	SINDE X[17]	SINDE X[16]	VDDQ_Q	VDDQ_Q	NC	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	INT_VD D	NC	NC	VDDQ_S	AD_SA DR[15]	AD_SA DR[17]	AD_SA DR[19]	AD_SA DR[21]		
W	INDEX[15]	INDEX[14]	SINDE X[15]	SINDE X[14]	VSS	VSS	INT_VD D	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	NC	INT_VD D	VSS	VSS	AD_SA DR[7]	AD_SA DR[9]	AD_SA DR[11]	AD_SA DR[13]	
Y	INDEX[13]	INDEX[12]	SINDE X[13]	SINDE X[12]	VSS	VSS	INT_VD D	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	INT_VD D	NC	NC	INT_VD D	VSS	VSS	AD_SA DR[3]	AD_SA DR[5]	AD_CE L	AD_WE L
AA	INDEX[11]	INDEX[10]	SINDE X[11]	SINDE X[10]	NSERE R0	VDDQ_Q	NC	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	NC	NC	NC	NC	AD_SA DR[1]	AD_SA DR[0]	NC	NC		
AB	INDEX[9]	INDEX[8]	SINDE X[9]	SINDE X[8]	NSERE F4	VDDQ_Q	NC	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	INT_VD D	NC	NC	INT_VD D	VSS	VSS	AD_SA DR[1]	AD_SA DR[2]	AD_SA DR[4]	NC	
AC	INDEX[7]	INDEX[6]	SINDE X[7]	SINDE X[6]	VSS	VSS	INT_VD D	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	INT_VD D	NC	NC	INT_VD D	VSS	VSS	AD_SA DR[6]	AD_SA DR[8]	AD_SA DR[10]	AD_SA DR[12]	
AD	INDEX[5]	INDEX[4]	SINDE X[5]	SINDE X[4]	VSS	VSS	INT_VD D	NC	NC	INT_VS S	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	INT_VD D	NC	NC	INT_VD D	VSS	VSS	AD_SA DR[14]	AD_SA DR[16]	AD_SA DR[18]	AD_SA DR[20]	
AE	INDEX[3]	INDEX[2]	SINDE X[3]	SINDE X[2]	VDDQ_Q	VDDQ_Q	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	AD_SA ATA[1]	AD_SA ATA[2]	NC	AD_SA ATA[3]		
AF	INDEX[1]	INDEX[0]	SINDE X[1]	SINDE X[0]	VDDQ_Q	VDDQ_Q	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	AD_SA ATA[17]	AD_SA ATA[16]	AD_SA ATA[2]	AD_SA ATA[2]		
AG	VDDQ_Q	CM0[1]	VDDQ_Q	CM0[0]	NC	VSS	VSS	INT_VD D	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	
AH	CM0[9]	CM0[8]	SCMDV	NC	VSS	VSS	INT_VD D	NC	NC	NC	INT_VD D	INT_VD D	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	
AJ	CM0[7]	CM0[6]	RSVD	VDDQ_Q	VSS	VSS	VSS	VSS	VDDQ_Q	VDDQ_Q	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS		
AK	CM0[5]	CM0[4]	RSVD	VDDQ_Q	VDDQ_Q	VSS	VSS	VSS	VDDQ_Q	VDDQ_Q	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS		
AL	CM0[3]	CM0[2]	HS_PW RSAVE	VDDQ_Q	VDDQ_Q	VDDQ_Q	DQ[3]	DQ[7]	DQ[11]	DQ[15]	DQ[19]	DQ[23]	DQ[27]	DQ[31]	DQ[35]	DQ[39]	DQ[43]	DQ[47]	DQ[51]	DQ[55]	DQ[59]	DQ[63]	DQ[67]	DQ[71]	DQ[75]	DQ[79]	DQ[83]	DQ[87]	DQ[91]	DQ[95]	DQ[99]	DQ[103]	DQ[107]		
AM	CM0[1]	CM0[0]	RULL_N	NC	PAR[1]	DQ[1]	DQ[5]	DQ[9]	DQ[13]	DQ[17]	DQ[21]	DQ[25]	DQ[29]	DQ[33]	DQ[37]	DQ[41]	DQ[45]	DQ[49]	DQ[53]	DQ[57]	DQ[61]	DQ[65]	DQ[69]	TDI	TMS	TCK	TRST*	TDO	BH[1]	BH[2]	BH[3]	BH[4]			
AN	CM0V	VDDQ_Q	SPARE RR_L	PHS_O UT_L	VDDQ_Q	PARER R_L	DQ[2]	DQ[6]	DQ[10]	DQ[14]	DQ[18]	DQ[22]	DQ[26]	DQ[30]	DQ[34]	DQ[38]	DQ[42]	DQ[46]	DQ[50]	DQ[54]	DQ[58]	DQ[62]	DQ[66]	DQ[70]	LH[0]	LH[1]	LH[2]	LH[3]	LH[4]	LH[5]	LH[6]	LH[7]			
AP	n o ball	TERM	ACK	RSVD	PAR[0]	DQ[0]	DQ[4]	DQ[8]	DQ[12]	DQ[16]	DQ[20]	DQ[24]	DQ[28]	DQ[32]	DQ[36]	DQ[40]	DQ[44]	DQ[48]	DQ[52]	DQ[56]	DQ[60]	DQ[64]	DQ[68]	RSVD	LH[1]	LH[2]	LH[3]	LH[4]	LH[5]	LH[6]	LH[7]	n o ball			

Figure 33. CYNSE20526 Single LA-1 Port Top View

Table 22. Signal Assignment

Package Ball Number	CYNSE20XXX-XXXXFGC		Package Ball Number	CYNSE20XXX-XXXXFGC		Package Ball Number	CYNSE20XXX-XXXXFGC	
	Signal Name	Signal Type		Signal Name	Signal Type		Signal Name	Signal Type
A1	No Ball [NC]	No Ball [NC]	AA24	VSS	GND	AB8	NC	NO CONNECT
A10	NC	NO CONNECT	AA25	VSS	GND	AB9	NC	NO CONNECT
A11	NC	NO CONNECT	AA26	NC	NO CONNECT	AC1	INDEX[7]	I/O
A12	NC	NO CONNECT	AA27	NC	NO CONNECT	AC10	NC/INT_VSS	NO CONNECT
A13	NC	NO CONNECT	AA28	NC	NO CONNECT	AC11	VDD	1.2V
A14	NC	NO CONNECT	AA29	VDDQ_S	1.5V/1.8V/2.5V	AC12	VDD	1.2V
A15	CQ0#	OUTPUT	AA3	SINDEX[11]	INPUT	AC13	VDD	1.2V
A16	E0[0]	INPUT	AA30	VDDQ_S	1.5V/1.8V/2.5V	AC14	VDD	1.2V
A17	CLK	INPUT	AA31	AD_SADR[1]	OUTPUT	AC15	VDD	1.2V
A18	VSS	GND	AA32	AD_SADR[0]	OUTPUT	AC16	VDD	1.2V
A19	see Table 23		AA33	NC	NO CONNECT	AC17	VDD	1.2V
A2	NC	NO CONNECT	AA34	NC	NO CONNECT	AC18	VSS	GND
A20	see Table 23		AA4	SINDEX[10]	INPUT	AC19	VSS	GND
A21	see Table 23		AA5	NSEREF0	INPUT	AC2	INDEX[6]	I/O
A22	see Table 23		AA6	VDDQ_A	1.5V/1.8V/2.5V	AC20	VSS	GND
A23	see Table 23		AA7	NC	NO CONNECT	AC21	VSS	GND
A24	see Table 23		AA8	NC	NO CONNECT	AC22	VSS	GND
A25	see Table 23		AA9	NC	NO CONNECT	AC23	VSS	GND
A26	see Table 23		AB1	INDEX[9]	I/O	AC24	VSS	GND
A27	NC	NO CONNECT	AB10	NC/INT_VSS	NO CONNECT	AC25	VSS	GND
A28	see Table 23		AB11	VDD	1.2V	AC26	NC/INT_VDD	NO CONNECT
A29	see Table 23		AB12	VDD	1.2V	AC27	NC	NO CONNECT
A3	NC	NO CONNECT	AB13	VDD	1.2V	AC28	NC/INT_VDD	NO CONNECT
A30	see Table 23		AB14	VDD	1.2V	AC29	VSS	GND
A31	see Table 23		AB15	VDD	1.2V	AC3	SINDEX[7]	INPUT
A32	see Table 23		AB16	VDD	1.2V	AC30	VSS	GND
A33	see Table 23		AB17	VDD	1.2V	AC31	AD_SADR[6]	OUTPUT
A34	No Ball [NC]	No Ball [NC]	AB18	VSS	GND	AC32	AD_SADR[8]	OUTPUT
A4	NC	NO CONNECT	AB19	VSS	GND	AC33	AD_SADR[10]	OUTPUT
A5	NC	NO CONNECT	AB2	INDEX[8]	I/O	AC34	AD_SADR[12]	OUTPUT
A6	NC	NO CONNECT	AB20	VSS	GND	AC4	SINDEX[6]	INPUT
A7	NC	NO CONNECT	AB21	VSS	GND	AC5	VSS	GND
A8	DOFF0_L	INPUT	AB22	VSS	GND	AC6	VSS	GND
A9	NC	NO CONNECT	AB23	VSS	GND	AC7	NC/INT_VDD	NO CONNECT
AA1	INDEX[11]	I/O	AB24	VSS	GND	AC8	NC	NO CONNECT
AA10	NC/INT_VSS ^[27]	NO CONNECT	AB25	VSS	GND	AC9	NC	NO CONNECT
AA11	VDD	1.2V	AB26	NC/INT_VDD ^[27]	NO CONNECT	AD1	INDEX[5]	I/O
AA12	VDD	1.2V	AB27	NC	NO CONNECT	AD10	NC/INT_VSS	NO CONNECT
AA13	VDD	1.2V	AB28	NC	NO CONNECT	AD11	VDD	1.2V
AA14	VDD	1.2V	AB29	VDDQ_S	1.5V/1.8V/2.5V	AD12	VDD	1.2V
AA15	VDD	1.2V	AB3	SINDEX[9]	INPUT	AD13	VDD	1.2V
AA16	VDD	1.2V	AB30	VDDQ_S	1.5V/1.8V/2.5V	AD14	VDD	1.2V
AA17	VDD	1.2V	AB31	AD_SADR[2]	OUTPUT	AD15	VDD	1.2V
AA18	VSS	GND	AB32	AD_SADR[4]	OUTPUT	AD16	VDD	1.2V
AA19	VSS	GND	AB33	NC	NO CONNECT	AD17	VDD	1.2V
AA2	INDEX[10]	I/O	AB34	NC	NO CONNECT	AD18	VSS	GND
AA20	VSS	GND	AB4	SINDEX[8]	INPUT	AD19	VSS	GND

Note:

27. NC/INT_VSS and NC/INT_VDD indicate that the Ayama 20000 pin is a true No-Connect, but if the board is to be designed for use with the optional decoupling interposer, the board pads should be connected to VSS or VDD. A board built by connecting the NC/INT_VSS and NC/INT_VDD pins to VSS and VDD respectively can be used for either the base Ayama 20000 or Ayama 20000 + interposer combinations.

Table 22. Signal Assignment (continued)

Package Ball Number	CYNSE20XXX-XXXXFGC		Package Ball Number	CYNSE20XXX-XXXXFGC		Package Ball Number	CYNSE20XXX-XXXXFGC	
	Signal Name	Signal Type		Signal Name	Signal Type		Signal Name	Signal Type
AA21	VSS	GND	AB5	NSEREF4	INPUT	AD2	INDEX[4]	I/O
AA22	VSS	GND	AB6	VDDQ_A	1.5V/1.8V/2.5V	AD20	VSS	GND
AA23	VSS	GND	AB7	NC	NO CONNECT	AD21	VSS	GND
AD22	VSS	GND	AE6	VDDQ_A	1.5V/1.8V/2.5V	AG20	NC	NO CONNECT
AD23	VSS	GND	AE7	NC	NO CONNECT	AG21	NC	NO CONNECT
AD24	VSS	GND	AE8	NC	NO CONNECT	AG22	NC	NO CONNECT
AD25	VSS	GND	AE9	NC	NO CONNECT	AG23	NC	NO CONNECT
AD26	NC/INT_VDD	NO CONNECT	AF1	INDEX[1]	I/O	AG24	NC	NO CONNECT
AD27	NC	NO CONNECT	AF10	NC	NO CONNECT	AG25	NC	NO CONNECT
AD28	NC/INT_VDD	NO CONNECT	AF11	NC	NO CONNECT	AG26	NC	NO CONNECT
AD29	VSS	GND	AF12	NC	NO CONNECT	AG27	NC	NO CONNECT
AD3	SINDEX[5]	INPUT	AF13	NC	NO CONNECT	AG28	NC/INT_VDD	NO CONNECT
AD30	VSS	GND	AF14	NC	NO CONNECT	AG29	VSS	GND
AD31	AD_SADR[14]	OUTPUT	AF15	NC	NO CONNECT	AG3	VDDQ_A	1.5V/1.8V/2.5V
AD32	AD_SADR[16]	OUTPUT	AF16	NC	NO CONNECT	AG30	VSS	GND
AD33	AD_SADR[18]	OUTPUT	AF17	NC	NO CONNECT	AG31	AD_SDATA[19]	I/O
AD34	AD_SADR[20]	OUTPUT	AF18	NC	NO CONNECT	AG32	AD_SDATA[18]	I/O
AD4	SINDEX[4]	INPUT	AF19	NC	NO CONNECT	AG33	AD_SDATA[27]	I/O
AD5	VSS	GND	AF2	INDEX[0]	I/O	AG34	AD_SDATA[26]	I/O
AD6	VSS	GND	AF20	NC	NO CONNECT	AG4	NC	NO CONNECT
AD7	NC/INT_VDD	NO CONNECT	AF21	NC	NO CONNECT	AG5	VSS	GND
AD8	NC	NO CONNECT	AF22	NC	NO CONNECT	AG6	VSS	GND
AD9	NC	NO CONNECT	AF23	NC	NO CONNECT	AG7	NC/INT_VDD	NO CONNECT
AE1	INDEX[3]	I/O	AF24	NC	NO CONNECT	AG8	NC	NO CONNECT
AE10	NC	NO CONNECT	AF25	NC	NO CONNECT	AG9	NC	NO CONNECT
AE11	NC	NO CONNECT	AF26	NC	NO CONNECT	AH1	CMD[9]	OUTPUT
AE12	NC	NO CONNECT	AF27	NC	NO CONNECT	AH10	NC	NO CONNECT
AE13	NC/INT_VSS	NO CONNECT	AF28	NC	NO CONNECT	AH11	NC/INT_VDD	NO CONNECT
AE14	NC/INT_VSS	NO CONNECT	AF29	VDDQ_S	1.5V/1.8V/2.5V	AH12	NC/INT_VDD	NO CONNECT
AE15	NC/INT_VSS	NO CONNECT	AF3	SINDEX[1]	INPUT	AH13	NC	NO CONNECT
AE16	NC/INT_VSS	NO CONNECT	AF30	VDDQ_S	1.5V/1.8V/2.5V	AH14	NC	NO CONNECT
AE17	NC	NO CONNECT	AF31	AD_SDATA[17]	I/O	AH15	NC/INT_VDD	NO CONNECT
AE18	NC	NO CONNECT	AF32	AD_SDATA[16]	I/O	AH16	NC/INT_VDD	NO CONNECT
AE19	NC	NO CONNECT	AF33	AD_SDATA[25]	I/O	AH17	NC	NO CONNECT
AE2	INDEX[2]	I/O	AF34	AD_SDATA[24]	I/O	AH18	NC	NO CONNECT
AE20	NC	NO CONNECT	AF4	SINDEX[0]	INPUT	AH19	NC/INT_VDD	NO CONNECT
AE21	NC	NO CONNECT	AF5	VDDQ_A	1.5V/1.8V/2.5V	AH2	CMD[8]	OUTPUT
AE22	NC	NO CONNECT	AF6	VDDQ_A	1.5V/1.8V/2.5V	AH20	NC/INT_VDD	NO CONNECT
AE23	NC	NO CONNECT	AF7	NC	NO CONNECT	AH21	NC	NO CONNECT
AE24	NC	NO CONNECT	AF8	NC	NO CONNECT	AH22	NC	NO CONNECT
AE25	NC	NO CONNECT	AF9	NC	NO CONNECT	AH23	NC/INT_VDD	NO CONNECT
AE26	NC	NO CONNECT	AG1	VDDQ_A	1.5V/1.8V/2.5V	AH24	NC/INT_VDD	NO CONNECT
AE27	NC	NO CONNECT	AG10	NC	NO CONNECT	AH25	NC	NO CONNECT
AE28	NC	NO CONNECT	AG11	NC	NO CONNECT	AH26	NC	NO CONNECT
AE29	VDDQ_S	1.5V/1.8V/2.5V	AG12	NC	NO CONNECT	AH27	NC	NO CONNECT
AE3	SINDEX[3]	INPUT	AG13	NC	NO CONNECT	AH28	NC/INT_VDD	NO CONNECT
AE30	VDDQ_S	1.5V/1.8V/2.5V	AG14	NC	NO CONNECT	AH29	VSS	GND
AE31	AD_SDATAP[3]	I/O	AG15	NC	NO CONNECT	AH3	SCMDV	OUTPUT
AE32	AD_SADR[22]	OUTPUT	AG16	NC	NO CONNECT	AH30	VSS	GND
AE33	NC	NO CONNECT	AG17	NC	NO CONNECT	AH31	AD_SDATA[21]	I/O

Table 22. Signal Assignment (continued)

Package Ball Number	CYNSE20XXX-XXXXFGC		Package Ball Number	CYNSE20XXX-XXXXFGC		Package Ball Number	CYNSE20XXX-XXXXFGC	
	Signal Name	Signal Type		Signal Name	Signal Type		Signal Name	Signal Type
AE34	AD_SDATAP[2]	I/O	AG18	NC	NO CONNECT	AH32	AD_SDATA[20]	I/O
AE4	SINDEX[2]	INPUT	AG19	NC	NO CONNECT	AH33	AD_SDATA[29]	I/O
AE5	VDDQ_A	1.5V/1.8V/2.5V	AG2	CMD[10]	OUTPUT	AH34	AD_SDATA[28]	I/O
AH4	NC	NO CONNECT	AK19	VSS	GND	AL33	RSVD	RESERVED
AH5	VSS	GND	AK2	CMD[4]	OUTPUT	AL34	FULI[6]	INPUT
AH6	VSS	GND	AK20	VSS	GND	AL4	VDDQ_A	1.5V/1.8V/2.5V
AH7	NC/INT_VDD	NO CONNECT	AK21	VDDQ_A	1.5V/1.8V/2.5V	AL5	VDDQ_A	1.5V/1.8V/2.5V
AH8	NC	NO CONNECT	AK22	VDDQ_A	1.5V/1.8V/2.5V	AL6	VDDQ_A	1.5V/1.8V/2.5V
AH9	NC	NO CONNECT	AK23	VSS	GND	AL7	DQ[3]	I/O
AJ1	CMD[7]	OUTPUT	AK24	VSS	GND	AL8	DQ[7]	I/O
AJ10	VDDQ_A	1.5V/1.8V/2.5V	AK25	VDDQ_A	1.5V/1.8V/2.5V	AL9	DQ[11]	I/O
AJ11	VSS	GND	AK26	VDDQ_A	1.5V/1.8V/2.5V	AM1	CMD[1]	OUTPUT
AJ12	VSS	GND	AK27	VSS	GND	AM10	DQ[13]	I/O
AJ13	VDDQ_A	1.5V/1.8V/2.5V	AK28	VSS	GND	AM11	DQ[17]	I/O
AJ14	VDDQ_A	1.5V/1.8V/2.5V	AK29	VDDQ_J	1.8V/2.5V	AM12	DQ[21]	I/O
AJ15	VSS	GND	AK3	RSVD	RESERVED	AM13	DQ[25]	I/O
AJ16	VSS	GND	AK30	VDDQ_A	1.5V/1.8V/2.5V	AM14	DQ[29]	I/O
AJ17	VDDQ_A	1.5V/1.8V/2.5V	AK31	VDDQ_A	1.5V/1.8V/2.5V	AM15	DQ[33]	I/O
AJ18	VDDQ_A	1.5V/1.8V/2.5V	AK32	SRAMSEL	INPUT	AM16	DQ[37]	I/O
AJ19	VSS	GND	AK33	FULO[1]	OUTPUT	AM17	DQ[41]	I/O
AJ2	CMD[6]	OUTPUT	AK34	FULO[0]	OUTPUT	AM18	DQ[45]	I/O
AJ20	VSS	GND	AK4	VDDQ_A	1.5V/1.8V/2.5V	AM19	DQ[49]	I/O
AJ21	VDDQ_A	1.5V/1.8V/2.5V	AK5	VDDQ_A	1.5V/1.8V/2.5V	AM2	CMD[0]	OUTPUT
AJ22	VDDQ_A	1.5V/1.8V/2.5V	AK6	VSS	GND	AM20	DQ[53]	I/O
AJ23	VSS	GND	AK7	VSS	GND	AM21	DQ[57]	I/O
AJ24	VSS	GND	AK8	VSS	GND	AM22	DQ[61]	I/O
AJ25	VDDQ_A	1.5V/1.8V/2.5V	AK9	VDDQ_A	1.5V/1.8V/2.5V	AM23	DQ[65]	I/O
AJ26	VDDQ_A	1.5V/1.8V/2.5V	AL1	CMD[3]	OUTPUT	AM24	DQ[69]	I/O
AJ27	VSS	GND	AL10	DQ[15]	I/O	AM25	TDI	INPUT
AJ28	VSS	GND	AL11	DQ[19]	I/O	AM26	TMS	INPUT
AJ29	VSS	GND	AL12	DQ[23]	I/O	AM27	TCK	INPUT
AJ3	RSVD	RESERVED	AL13	DQ[27]	I/O	AM28	TRST*	INPUT
AJ30	NSREF3	INPUT	AL14	DQ[31]	I/O	AM29	TDO	OUTPUT-T
AJ31	AD_SDATA[23]	I/O	AL15	DQ[35]	I/O	AM3	VDDQ_A	1.5V/1.8V/2.5V
AJ32	AD_SDATA[22]	I/O	AL16	DQ[39]	I/O	AM30	BHI[2]	INPUT
AJ33	AD_SDATA[31]	I/O	AL17	DQ[43]	I/O	AM31	BHO[2]	OUTPUT
AJ34	AD_SDATA[30]	I/O	AL18	DQ[47]	I/O	AM32	VDDQ_A	1.5V/1.8V/2.5V
AJ4	VDDQ_A	1.5V/1.8V/2.5V	AL19	DQ[51]	I/O	AM33	FULI[5]	INPUT
AJ5	VSS	GND	AL2	CMD[2]	OUTPUT	AM34	FULI[4]	INPUT
AJ6	VSS	GND	AL20	DQ[55]	I/O	AM4	FULL_IN	INPUT
AJ7	VSS	GND	AL21	DQ[59]	I/O	AM5	NC	NO CONNECT
AJ8	VSS	GND	AL22	DQ[63]	I/O	AM6	PAR[1]	I/O
AJ9	VDDQ_A	1.5V/1.8V/2.5V	AL23	DQ[67]	I/O	AM7	DQ[1]	I/O
AK1	CMD[5]	OUTPUT	AL24	DQ[71]	I/O	AM8	DQ[5]	I/O
AK10	VDDQ_A	1.5V/1.8V/2.5V	AL25	ID[0]	INPUT	AM9	DQ[9]	I/O
AK11	VSS	GND	AL26	ID[1]	INPUT	AN1	CMDV	OUTPUT
AK12	VSS	GND	AL27	ID[2]	INPUT	AN10	DQ[14]	I/O
AK13	VDDQ_A	1.5V/1.8V/2.5V	AL28	ID[3]	INPUT	AN11	DQ[18]	I/O
AK14	VDDQ_A	1.5V/1.8V/2.5V	AL29	ID[4]	INPUT	AN12	DQ[22]	I/O
AK15	VSS	GND	AL3	HS_PWRSAVE	OUTPUT	AN13	DQ[24]	I/O

Table 22. Signal Assignment (continued)

Package Ball Number	CYNSE20XXX-XXXXFGC		Package Ball Number	CYNSE20XXX-XXXXFGC		Package Ball Number	CYNSE20XXX-XXXXFGC	
	Signal Name	Signal Type		Signal Name	Signal Type		Signal Name	Signal Type
AK16	VSS	GND	AL30	VDDQ_A	1.5V/1.8V/2.5V	AN14	DQ[30]	I/O
AK17	VDDQ_A	1.5V/1.8V/2.5V	AL31	VDDQ_A	1.5V/1.8V/2.5V	AN15	DQ[34]	I/O
AK18	VDDQ_A	1.5V/1.8V/2.5V	AL32	NSESEL	INPUT	AN16	DQ[36]	I/O
AN17	DQ[40]	I/O	AP31	BHO[0]	OUTPUT	C15	A0[19]	INPUT
AN18	DQ[44]	I/O	AP32	FULI[0]	INPUT	C16	EP0[0]	INPUT
AN19	DQ[48]	I/O	AP33	FULI[2]	INPUT	C17	RA0	OUTPUT
AN2	VDDQ_A	1.5V/1.8V/2.5V	AP34	No Ball [NC]	No Ball [NC]	C18	see Table 23	
AN20	DQ[52]	I/O	AP4	ACK	I/O	C19	see Table 23	
AN21	DQ[56]	I/O	AP5	RSVD	RESERVED	C2	QP0[1]	OUTPUT
AN22	DQ[62]	I/O	AP6	PAR[0]	I/O	C20	see Table 23	
AN23	DQ[66]	I/O	AP7	DQ[0]	I/O	C21	NC	NO CONNECT
AN24	DQ[70]	I/O	AP8	DQ[4]	I/O	C22	NC	NO CONNECT
AN25	LHI[0]	INPUT	AP9	DQ[8]	I/O	C23	NC	NO CONNECT
AN26	LHI[2]	INPUT	B1	IFC0[1]	INPUT	C24	NC	NO CONNECT
AN27	LHI[4]	INPUT	B10	Q0[12]	OUTPUT	C25	NC	NO CONNECT
AN28	LHI[6]	INPUT	B11	NC	NO CONNECT	C26	NC	NO CONNECT
AN29	LHO[1]	OUTPUT	B12	D0[11]	INPUT	C27	VDDQ_Q	1.5V
AN3	SPARERR_L	INPUT	B13	NC	NO CONNECT	C28	NC	NO CONNECT
AN30	BHI[1]	INPUT	B14	Q0[9]	OUTPUT	C29	NC	NO CONNECT
AN31	BHO[1]	OUTPUT	B15	NC/A0[21]	NO CONNECT	C3	QP0[0]	OUTPUT
AN32	FULI[1]	INPUT	B16	E0[1]	INPUT	C30	NC	NO CONNECT
AN33	VDDQ_A	1.5V/1.8V/2.5V	B17	CLK_MODE	INPUT	C31	NC	NO CONNECT
AN34	FULI[3]	INPUT	B18	RST_L	INPUT	C32	NC	NO CONNECT
AN4	PHS_OUT_L	OUTPUT	B19	see Table 23		C33	NC	NO CONNECT
AN5	VDDQ_A	1.5V/1.8V/2.5V	B2	NC	NO CONNECT	C34	see Table 23	
AN6	PARERR_L	I/O	B20	see Table 23		C4	DP0[0]	INPUT
AN7	DQ[2]	I/O	B21	NC	NO CONNECT	C5	D0[15]	INPUT
AN8	DQ[6]	I/O	B22	see Table 23		C6	Q0[14]	OUTPUT
AN9	DQ[10]	I/O	B23	NC	NO CONNECT	C7	D0[14]	INPUT
AP1	No Ball [NC]	No Ball [NC]	B24	see Table 23		C8	VDDQ_Q	1.5V
AP10	DQ[12]	I/O	B25	NC	NO CONNECT	C9	Q0[13]	OUTPUT
AP11	DQ[16]	I/O	B26	NC	NO CONNECT	D1	A0[8]	INPUT
AP12	DQ[20]	I/O	B27	QDR1REF0	INPUT	D10	VDDQ_Q	1.5V
AP13	DQ[26]	I/O	B28	see Table 23		D11	VDDQ_Q	1.5V
AP14	DQ[28]	I/O	B29	see Table 23		D12	VSS	GND
AP15	DQ[32]	I/O	B3	DP0[1]	INPUT	D13	VSS	GND
AP16	DQ[38]	I/O	B30	NC	NO CONNECT	D14	A0[4]	INPUT
AP17	DQ[42]	I/O	B31	see Table 23		D15	W0#	INPUT
AP18	DQ[46]	I/O	B32	NC	NO CONNECT	D16	EP0[1]	INPUT
AP19	DQ[50]	I/O	B33	see Table 23		D17	NC	NO CONNECT
AP2	TERM	I/O	B34	see Table 23		D18	NC	NO CONNECT
AP20	DQ[54]	I/O	B4	NC	NO CONNECT	D19	see Table 23	
AP21	DQ[58]	I/O	B5	Q0[15]	OUTPUT	D2	A0[10]	INPUT
AP22	DQ[60]	I/O	B6	NC	NO CONNECT	D20	see Table 23	
AP23	DQ[64]	I/O	B7	NC	NO CONNECT	D21	see Table 23	
AP24	DQ[68]	I/O	B8	QDR0REF1	INPUT	D22	VSS	GND
AP25	RSVD	RESERVED	B9	D0[13]	INPUT	D23	VSS	GND
AP26	LHI[1]	INPUT	C1	A0[6]	INPUT	D24	VDDQ_Q	1.5V
AP27	LHI[3]	INPUT	C10	D0[12]	INPUT	D25	VDDQ_Q	1.5V
AP28	LHI[5]	INPUT	C11	Q0[11]	OUTPUT	D26	VDDQ_Q	1.5V

Table 22. Signal Assignment (continued)

Package Ball Number	CYNSE20XXX-XXXXFGC		Package Ball Number	CYNSE20XXX-XXXXFGC		Package Ball Number	CYNSE20XXX-XXXXFGC	
	Signal Name	Signal Type		Signal Name	Signal Type		Signal Name	Signal Type
AP29	LHO[0]	OUTPUT	C12	Q0[10]	OUTPUT	D27	VDDQ_Q	1.5V
AP3	FULL_OUT	OUTPUT	C13	D0[10]	INPUT	D28	VDDQ_Q	1.5V
AP30	BHI[0]	INPUT	C14	D0[9]	INPUT	D29	VDDQ_Q	1.5V
D3	VSS_PLL	GND	F13	A0[0]	INPUT	G28	VDD	1.2V
D30	VDDQ_Q	1.5V	F14	K0	INPUT	G29	VDD	1.2V
D31	VSS	GND	F15	K0#	INPUT	G3	A0[13]	INPUT
D32	VSS	GND	F16	TEST_PB	INPUT	G30	VSS	GND
D33	see Table 23		F17	NC	NO CONNECT	G31	VSS	GND
D34	see Table 23		F18	RSVD	RESERVED	G32	see Table 23	
D4	VSS	GND	F19	RSVD	RESERVED	G33	see Table 23	
D5	VDDQ_Q	1.5V	F2	C0	INPUT	G34	see Table 23	
D6	VDDQ_Q	1.5V	F20	see Table 23		G4	VSS	GND
D7	VDDQ_Q	1.5V	F21	see Table 23		G5	VSS	GND
D8	VDDQ_Q	1.5V	F22	see Table 23		G6	VDD	1.2V
D9	VDDQ_Q	1.5V	F23	VSS	GND	G7	VDD	1.2V
E1	A0[18]	INPUT	F24	VSS	GND	G8	VDD	1.2V
E10	VDD	1.2V	F25	VSS	GND	G9	VDD	1.2V
E11	VSS	GND	F26	VSS	GND	H1	A0[9]	INPUT
E12	VSS	GND	F27	VSS	GND	H10	VDDQ_Q	1.5V
E13	A0[2]	INPUT	F28	VSS	GND	H11	VDDQ_Q	1.5V
E14	NC	NO CONNECT	F29	VSS	GND	H12	VSS	GND
E15	BW0#[1]	INPUT	F3	A0[12]	INPUT	H13	VSS	GND
E16	RSVD	RESERVED	F30	VSS	GND	H14	A0[3]	INPUT
E17	NC	NO CONNECT	F31	VSS	GND	H15	R0#	INPUT
E18	NC	NO CONNECT	F32	see Table 23		H16	NC	NO CONNECT
E19	RSVD	RESERVED	F33	see Table 23		H17	NC	NO CONNECT
E2	A0[16]	INPUT	F34	see Table 23		H18	NC	NO CONNECT
E20	NC	NO CONNECT	F4	VSS	GND	H19	NC	NO CONNECT
E21	see Table 23		F5	VSS	GND	H2	A0[11]	INPUT
E22	see Table 23		F6	VSS	GND	H20	see Table 23	
E23	VSS	GND	F7	VSS	GND	H21	see Table 23	
E24	VSS	GND	F8	VSS	GND	H22	VSS	GND
E25	VDD	1.2V	F9	VSS	GND	H23	VSS	GND
E26	VDD	1.2V	G1	A0[17]	INPUT	H24	VDDQ_Q	1.5V
E27	VDD	1.2V	G10	VDD	1.2V	H25	VDDQ_Q	1.5V
E28	VDD	1.2V	G11	VSS	GND	H26	VDDQ_Q	1.5V
E29	VDD	1.2V	G12	VSS	GND	H27	VDDQ_Q	1.5V
E3	A0[14]	INPUT	G13	A0[1]	INPUT	H28	VDDQ_Q	1.5V
E30	VSS	GND	G14	BW0#[0]	INPUT	H29	VDDQ_Q	1.5V
E31	VSS	GND	G15	NC	NO CONNECT	H3	VSS	GND
E32	see Table 23		G16	RSVD	RESERVED	H30	VDDQ_Q	1.5V
E33	see Table 23		G17	NC	NO CONNECT	H31	VSS	GND
E34	see Table 23		G18	NC	NO CONNECT	H32	VSS	GND
E4	VSS	GND	G19	RSVD	RESERVED	H33	see Table 23	
E5	VSS	GND	G2	A0[15]	INPUT	H34	see Table 23	
E6	VDD_PLL	1.2V	G20	see Table 23		H4	VSS	GND
E7	VDD	1.2V	G21	NC	NO CONNECT	H5	VDDQ_Q	1.5V
E8	VDD	1.2V	G22	see Table 23		H6	VDDQ_Q	1.5V
E9	VDD	1.2V	G23	VSS	GND	H7	VDDQ_Q	1.5V
F1	C0#	INPUT	G24	VSS	GND	H8	VDDQ_Q	1.5V

Table 22. Signal Assignment (continued)

Package Ball Number	CYNSE20XXX-XXXXFGC		Package Ball Number	CYNSE20XXX-XXXXFGC		Package Ball Number	CYNSE20XXX-XXXXFGC	
	Signal Name	Signal Type		Signal Name	Signal Type		Signal Name	Signal Type
F10	VSS	GND	G25	VDD	1.2V	H9	VDDQ_Q	1.5V
F11	VSS	GND	G26	VDD	1.2V	J1	A0[7]	INPUT
F12	VSS	GND	G27	VDD	1.2V	J10	NC	NO CONNECT
J11	NC	NO CONNECT	see Table 23			L8	NC	NO CONNECT
J12	NC	NO CONNECT	K26	see Table 23		L9	D0[5]	INPUT
J13	NC	NO CONNECT	K27	QDR1REF1	INPUT	M1	EINTR	OUTPUT
J14	NC	NO CONNECT	K28	NC	NO CONNECT	M10	NC/INT_VSS	NO CONNECT
J15	A0[5]	INPUT	K29	NC	NO CONNECT	M11	VDD	1.2V
J16	NC	NO CONNECT	K3	NC	NO CONNECT	M12	VDD	1.2V
J17	NC	NO CONNECT	K30	see Table 23		M13	VDD	1.2V
J18	NC	NO CONNECT	K31	NC	NO CONNECT	M14	VDD	1.2V
J19	NC	NO CONNECT	K32	see Table 23		M15	VDD	1.2V
J2	NC	NO CONNECT	K33	NC	NO CONNECT	M16	VDD	1.2V
J20	see Table 23		K34	see Table 23		M17	VDD	1.2V
J21	see Table 23		K4	Q0[1]	OUTPUT	M18	VSS	GND
J22	see Table 23		K5	NC	NO CONNECT	M19	VSS	GND
J23	see Table 23		K6	D0[3]	INPUT	M2	RSVD	RESERVED
J24	see Table 23		K7	Q0[4]	OUTPUT	M20	VSS	GND
J25	see Table 23		K8	QDR0REF0	INPUT	M21	VSS	GND
J26	see Table 23		K9	NC	NO CONNECT	M22	VSS	GND
J27	VDDQ_Q	1.5V	L1	NC	NO CONNECT	M23	VSS	GND
J28	see Table 23		L10	Q0[5]	OUTPUT	M24	VSS	GND
J29	see Table 23		L11	Q0[6]	OUTPUT	M25	HIGH_SPEEDI_L	INPUT
J3	NC	NO CONNECT	L12	D0[7]	INPUT	M26 ^[29]	see Table 23	
J30	see Table 23		L13	D0[8]	INPUT	M27 ^[29]	see Table 23	
J31	see Table 23		L14	Q0[8]	OUTPUT	M28 ^[29]	see Table 23	
J32	see Table 23		L15	CQ0	OUTPUT	M29	VDDQ_J	1.8V/2.5V
J33	see Table 23		L16	NC	NO CONNECT	M3	RSVD	RESERVED
J34	see Table 23		L17	NC	NO CONNECT	M30	SRAMREF	INPUT
J4	NC	NO CONNECT	L18	NC	NO CONNECT	M31	NC	NO CONNECT
J5	NC	NO CONNECT	L19	NC	NO CONNECT	M32	NC	NO CONNECT
J6	NC	NO CONNECT	L2	Q0[0]	OUTPUT	M33	NC	NO CONNECT
J7	NC	NO CONNECT	L20	see Table 23		M34	NC	NO CONNECT
J8	VDDQ_Q	1.5V	L21	NC	NO CONNECT	M4	RSVD	RESERVED
J9	NC	NO CONNECT	L22	NC	NO CONNECT	M5	NSEREF1	INPUT
K1	IFC0[0]	INPUT	L23	NC	NO CONNECT	M6	NSEREF2	INPUT
K10	NC	NO CONNECT	L24	NC	NO CONNECT	M7	NC	NO CONNECT
K11	D0[6]	INPUT	L25	NC	NO CONNECT	M8	NC	NO CONNECT
K12	NC	NO CONNECT	L26	NC	NO CONNECT	M9	NC	NO CONNECT
K13	Q0[7]	OUTPUT	L27	see Table 23		N1	SSV	I/O
K14	NC	NO CONNECT	L28	NC	NO CONNECT	N10	NC/INT_VSS	NO CONNECT
K15	NC/A0[20] ^[28]	NO CONNECT	L29	NC	NO CONNECT	N11	VDD	1.2V
K16	NC	NO CONNECT	L3	D0[1]	INPUT	N12	VDD	1.2V
K17	NC	NO CONNECT	L30	NC	NO CONNECT	N13	VDD	1.2V
K18	NC	NO CONNECT	L31	NC	NO CONNECT	N14	VDD	1.2V
K19	NC	NO CONNECT	L32	NC	NO CONNECT	N15	VDD	1.2V
K2	D0[0]	INPUT	L33	NC	NO CONNECT	N16	VDD	1.2V

Notes:

28. Refer to A0[21.0], A1[21.0] in signal description for more information.

29. To migrate from a lower density to a higher density Ayama 20000, or from a single LA-1 port to a dual LA-1 port Ayama 20000, M26, M27 and M28 should be driven to a jumper/header for configuration to avoid board redesign.

Table 22. Signal Assignment (continued)

Package Ball Number	CYNSE20XXX-XXXXFGC		Package Ball Number	CYNSE20XXX-XXXXFGC		Package Ball Number	CYNSE20XXX-XXXXFGC	
	Signal Name	Signal Type		Signal Name	Signal Type		Signal Name	Signal Type
K20	see Table 23		L34	NC	NO CONNECT	N17	VDD	1.2V
K21	see Table 23		L4	D0[2]	INPUT	N18	VSS	GND
K22	NC	NO CONNECT	L5	Q0[2]	OUTPUT	N19	VSS	GND
K23	see Table 23		L6	Q0[3]	OUTPUT	N2	SSF	I/O
K24	NC	NO CONNECT	L7	D0[4]	INPUT	N20	VSS	GND
N21	VSS	GND	P5	VDDQ_A	1.5V/1.8V/2.5V	T2	INDEX[20]	I/O
N22	VSS	GND	P6	VDDQ_A	1.5V/1.8V/2.5V	T20	VSS	GND
N23	VSS	GND	P7	NC	NO CONNECT	T21	VSS	GND
N24	VSS	GND	P8	NC	NO CONNECT	T22	VSS	GND
N25	VSS	GND	P9	NC	NO CONNECT	T23	VSS	GND
N26	NC/INT_VDD	NO CONNECT	R1	INDEX[23]	I/O	T24	VSS	GND
N27	NC	NO CONNECT	R10	NC/INT_VSS	NO CONNECT	T25	VSS	GND
N28	NC/INT_VDD	NO CONNECT	R11	VDD	1.2V	T26	NC	NO CONNECT
N29	VDDQ_S	1.5V/1.8V/2.5V	R12	VDD	1.2V	T27	NC	NO CONNECT
N3	SSSV	INPUT	R13	VDD	1.2V	T28	NC/INT_VDD	NO CONNECT
N30	VDDQ_S	1.5V/1.8V/2.5V	R14	VDD	1.2V	T29	VSS	GND
N31	AD_SDAT[7]	I/O	R15	VDD	1.2V	T3	SINDEX[21]	INPUT
N32	AD_SDAT[6]	I/O	R16	VDD	1.2V	T30	VSS	GND
N33	AD_SDAT[15]	I/O	R17	VDD	1.2V	T31	AD_SDAT[1]	I/O
N34	AD_SDAT[14]	I/O	R18	VSS	GND	T32	AD_SDAT[0]	I/O
N4	SSSF	INPUT	R19	VSS	GND	T33	AD_SDAT[9]	I/O
N5	VDDQ_A	1.5V/1.8V/2.5V	R2	INDEX[22]	I/O	T34	AD_SDAT[8]	I/O
N6	VDDQ_A	1.5V/1.8V/2.5V	R20	VSS	GND	T4	SINDEX[20]	INPUT
N7	NC	NO CONNECT	R21	VSS	GND	T5	VSS	GND
N8	NC	NO CONNECT	R22	VSS	GND	T6	VSS	GND
N9	NC	NO CONNECT	R23	VSS	GND	T7	NC/INT_VDD	NO CONNECT
P1	RSVD	RESERVED	R24	VSS	GND	T8	NC	NO CONNECT
P10	NC/INT_VSS	NO CONNECT	R25	VSS	GND	T9	NC	NO CONNECT
P11	VDD	1.2V	R26	NC	NO CONNECT	U1	INDEX[19]	I/O
P12	VDD	1.2V	R27	NC	NO CONNECT	U10	NC/INT_VSS	NO CONNECT
P13	VDD	1.2V	R28	NC/INT_VDD	NO CONNECT	U11	VDD	1.2V
P14	VDD	1.2V	R29	VSS	GND	U12	VDD	1.2V
P15	VDD	1.2V	R3	SINDEX[23]	INPUT	U13	VDD	1.2V
P16	VDD	1.2V	R30	VSS	GND	U14	VDD	1.2V
P17	VDD	1.2V	R31	AD_SDAT[3]	I/O	U15	VDD	1.2V
P18	VSS	GND	R32	AD_SDAT[2]	I/O	U16	VDD	1.2V
P19	VSS	GND	R33	AD_SDAT[11]	I/O	U17	VDD	1.2V
P2	RSVD	RESERVED	R34	AD_SDAT[10]	I/O	U18	VSS	GND
P20	VSS	GND	R4	SINDEX[22]	INPUT	U19	VSS	GND
P21	VSS	GND	R5	VSS	GND	U2	INDEX[18]	I/O
P22	VSS	GND	R6	VSS	GND	U20	VSS	GND
P23	VSS	GND	R7	NC/INT_VDD	NO CONNECT	U21	VSS	GND
P24	VSS	GND	R8	NC	NO CONNECT	U22	VSS	GND
P25	VSS	GND	R9	NC	NO CONNECT	U23	VSS	GND
P26	NC	NO CONNECT	T1	INDEX[21]	I/O	U24	VSS	GND
P27	NC	NO CONNECT	T10	NC/INT_VSS	NO CONNECT	U25	VSS	GND
P28	NC	NO CONNECT	T11	VDD	1.2V	U26	NC/INT_VDD	NO CONNECT
P29	VDDQ_S	1.5V/1.8V/2.5V	T12	VDD	1.2V	U27	NC	NO CONNECT
P3	NC	NO CONNECT	T13	VDD	1.2V	U28	NC	NO CONNECT

Table 22. Signal Assignment (continued)

Package Ball Number	CYNSE20XXX-XXXXFGC		Package Ball Number	CYNSE20XXX-XXXXFGC		Package Ball Number	CYNSE20XXX-XXXXFGC	
	Signal Name	Signal Type		Signal Name	Signal Type		Signal Name	Signal Type
P30	VDDQ_S	1.5V/1.8V/2.5V	T14	VDD	1.2V	U29	VDDQ_S	1.5V/1.8V/2.5V
P31	AD_SDATA[5]	I/O	T15	VDD	1.2V	U3	SINDEX[19]	INPUT
P32	AD_SDATA[4]	I/O	T16	VDD	1.2V	U30	VDDQ_S	1.5V/1.8V/2.5V
P33	AD_SDATA[13]	I/O	T17	VDD	1.2V	U31	AD_SDATA[0]	I/O
P34	AD_SDATA[12]	I/O	T18	VSS	GND	U32	AD_SADR[23]	OUTPUT
P4	NC	NO CONNECT	T19	VSS	GND	U33	NC	NO CONNECT
U34	AD_SDATA[1]	I/O	V5	VDDQ_A	1.5V/1.8V/2.5V	W7	NC/INT_VDD	NO CONNECT
U4	SINDEX[18]	INPUT	V6	VDDQ_A	1.5V/1.8V/2.5V	W8	NC	NO CONNECT
U5	VDDQ_A	1.5V/1.8V/2.5V	V7	NC/INT_VDD	NO CONNECT	W9	NC	NO CONNECT
U6	VDDQ_A	1.5V/1.8V/2.5V	V8	NC	NO CONNECT	Y1	INDEX[13]	I/O
U7	NC	NO CONNECT	V9	NC	NO CONNECT	Y10	NC/INT_VSS	NO CONNECT
U8	NC	NO CONNECT	W1	INDEX[15]	I/O	Y11	VDD	1.2V
U9	NC	NO CONNECT	W10	NC/INT_VSS	NO CONNECT	Y12	VDD	1.2V
V1	INDEX[17]	I/O	W11	VDD	1.2V	Y13	VDD	1.2V
V10	NC/INT_VSS	NO CONNECT	W12	VDD	1.2V	Y14	VDD	1.2V
V11	VDD	1.2V	W13	VDD	1.2V	Y15	VDD	1.2V
V12	VDD	1.2V	W14	VDD	1.2V	Y16	VDD	1.2V
V13	VDD	1.2V	W15	VDD	1.2V	Y17	VDD	1.2V
V14	VDD	1.2V	W16	VDD	1.2V	Y18	VSS	GND
V15	VDD	1.2V	W17	VDD	1.2V	Y19	VSS	GND
V16	VDD	1.2V	W18	VSS	GND	Y2	INDEX[12]	I/O
V17	VDD	1.2V	W19	VSS	GND	Y20	VSS	GND
V18	VSS	GND	W2	INDEX[14]	I/O	Y21	VSS	GND
V19	VSS	GND	W20	VSS	GND	Y22	VSS	GND
V2	INDEX[16]	I/O	W21	VSS	GND	Y23	VSS	GND
V20	VSS	GND	W22	VSS	GND	Y24	VSS	GND
V21	VSS	GND	W23	VSS	GND	Y25	VSS	GND
V22	VSS	GND	W24	VSS	GND	Y26	NC/INT_VDD	NO CONNECT
V23	VSS	GND	W25	VSS	GND	Y27	NC	NO CONNECT
V24	VSS	GND	W26	NC	NO CONNECT	Y28	NC/INT_VDD	NO CONNECT
V25	VSS	GND	W27	NC	NO CONNECT	Y29	VSS	GND
V26	NC/INT_VDD	NO CONNECT	W28	NC/INT_VDD	NO CONNECT	Y3	SINDEX[13]	INPUT
V27	NC	NO CONNECT	W29	VSS	GND	Y30	VSS	GND
V28	NC	NO CONNECT	W3	SINDEX[15]	INPUT	Y31	AD_SADR[3]	OUTPUT
V29	VDDQ_S	1.5V/1.8V/2.5V	W30	VSS	GND	Y32	AD_SADR[5]	OUTPUT
V3	SINDEX[17]	INPUT	W31	AD_SADR[7]	OUTPUT	Y33	AD_CE_L	OUTPUT
V30	VDDQ_S	1.5V/1.8V/2.5V	W32	AD_SADR[9]	OUTPUT	Y34	AD_WE_L	OUTPUT
V31	AD_SADR[15]	OUTPUT	W33	AD_SADR[11]	OUTPUT	Y4	SINDEX[12]	INPUT
V32	AD_SADR[17]	OUTPUT	W34	AD_SADR[13]	OUTPUT	Y5	VSS	GND
V33	AD_SADR[19]	OUTPUT	W4	SINDEX[14]	INPUT	Y6	VSS	GND
V34	AD_SADR[21]	OUTPUT	W5	VSS	GND	Y7	NC	NO CONNECT
V4	SINDEX[16]	INPUT	W6	VSS	GND	Y8	NC	NO CONNECT
						Y9	NC	NO CONNECT

Table 23. Signal Assignment Differences Between Devices

Package Ball Number	CYNSE20512-XXX2FGC		CYNSE20512-XXX1FGC		CYNSE20256-XXX2FGC		CYNSE20256-XXX1FGC	
	Signal Name	Signal Type	Signal Name	Signal Type	Signal Name	Signal Type	Signal Name	Signal Type
A19	E1[0]	INPUT	VSS	GND	E1[0]	INPUT	VSS	GND
A20	CQ1	OUTPUT	RSVD	RESERVED	CQ1	OUTPUT	RSVD	RESERVED
A21	Q1[8]	OUTPUT	RSVD	RESERVED	Q1[8]	OUTPUT	RSVD	RESERVED
A22	D1[8]	INPUT	VSS	GND	D1[8]	INPUT	VSS	GND
A23	D1[7]	INPUT	VSS	GND	D1[7]	INPUT	VSS	GND
A24	Q1[6]	OUTPUT	RSVD	RESERVED	Q1[6]	OUTPUT	RSVD	RESERVED
A25	Q1[5]	OUTPUT	RSVD	RESERVED	Q1[5]	OUTPUT	RSVD	RESERVED
A26	D1[5]	INPUT	VSS	GND	D1[5]	INPUT	VSS	GND
A28	D1[4]	INPUT	VSS	GND	D1[4]	INPUT	VSS	GND
A29	Q1[3]	OUTPUT	RSVD	RESERVED	Q1[3]	OUTPUT	RSVD	RESERVED
A30	Q1[2]	OUTPUT	RSVD	RESERVED	Q1[2]	OUTPUT	RSVD	RESERVED
A31	D1[2]	INPUT	VSS	GND	D1[2]	INPUT	VSS	GND
A32	D1[1]	INPUT	VSS	GND	D1[1]	OUTPUT	VSS	GND
A33	Q1[0]	OUTPUT	RSVD	RESERVED	Q1[0]	OUTPUT	RSVD	RESERVED
B19	E1[1]	INPUT	VSS	GND	E1[1]	INPUT	VSS	GND
B20	NC/A1[21] ^[28]	NO CONNECT	NC	NO CONNECT	NC/A1[21] ^[28]	NO CONNECT	NC	NO CONNECT
B22	Q1[7]	OUTPUT	RSVD	RESERVED	Q1[7]	OUTPUT	RSVD	RESERVED
B24	D1[6]	INPUT	VSS	GND	D1[6]	INPUT	VSS	GND
B28	Q1[4]	OUTPUT	RSVD	RESERVED	Q1[4]	OUTPUT	RSVD	RESERVED
B29	D1[3]	INPUT	VSS	GND	D1[3]	INPUT	VSS	GND
B31	Q1[1]	OUTPUT	RSVD	RESERVED	Q1[1]	OUTPUT	RSVD	RESERVED
B33	D1[0]	INPUT	VSS	GND	D1[0]	INPUT	VSS	GND
B34	IFC1[0]	INPUT	VSS	GND	IFC1[0]	INPUT	VSS	GND
C18	RA1	OUTPUT	RSVD	RESERVED	RA1	OUTPUT	RSVD	RESERVED
C19	EP1[0]	INPUT	VDDQ_Q	1.5V	EP1[0]	INPUT	VDDQ_Q	1.5
C20	A1[5]	INPUT	VSS	GND	A1[5]	INPUT	VSS	GND
C34	A1[7]	INPUT	VSS	GND	A1[7]	INPUT	VSS	GND
D19	EP1[1]	INPUT	VDDQ_Q	1.5V	EP1[1]	INPUT	VDDQ_Q	1.5V
D20	R1#	INPUT	VDDQ_Q	1.5V	R1#	INPUT	VDDQ_Q	1.5V
D21	A1[3]	INPUT	VSS	GND	A1[3]	INPUT	VSS	GND
D33	A1[11]	INPUT	VSS	GND	A1[11]	INPUT	VSS	GND
D34	A1[9]	INPUT	VSS	GND	A1[9]	INPUT	VSS	GND
E21	BW1#[0]	INPUT	VDDQ_Q	1.5V	BW1#[0]	INPUT	VDDQ_Q	1.5V
E22	A1[1]	INPUT	VSS	GND	A1[1]	INPUT	VSS	GND
E32	A1[13]	INPUT	VSS	GND	A1[13]	INPUT	VSS	GND
E33	A1[15]	INPUT	VSS	GND	A1[15]	INPUT	VSS	GND
E34	A1[17]	INPUT	VSS	GND	A1[17]	INPUT	VSS	GND
F20	K1#	INPUT	VSS	GND	K1#	INPUT	VSS	GND
F21	K1	INPUT	VSS	GND	K1	INPUT	VSS	GND
F22	A1[0]	INPUT	VSS	GND	A1[0]	INPUT	VSS	GND
F32	A1[12]	INPUT	VSS	GND	A1[12]	INPUT	VSS	GND
F33	C1	INPUT	VSS	GND	C1	INPUT	VSS	GND
F34	C1#	INPUT	VSS	GND	C1#	INPUT	VSS	GND
G20	BW1#[1]	INPUT	VDDQ_Q	1.5V	BW1#[1]	INPUT	VDDQ_Q	1.5V
G22	A1[2]	INPUT	VSS	GND	A1[2]	INPUT	VSS	GND
G32	A1[14]	INPUT	VSS	GND	A1[14]	INPUT	VSS	GND
G33	A1[16]	INPUT	VSS	GND	A1[16]	INPUT	VSS	GND
G34	A1[18]	INPUT	VSS	GND	A1[18]	INPUT	VSS	GND
H20	W1#	INPUT	VDDQ_Q	1.5V	W1#	INPUT	VDDQ_Q	1.5V
H21	A1[4]	INPUT	VSS	GND	A1[4]	INPUT	VSS	GND

Table 23. Signal Assignment Differences Between Devices (continued)

Package Ball Number	CYNSE20512-XXX2FGC		CYNSE20512-XXX1FGC		CYNSE20256-XXX2FGC		CYNSE20256-XXX1FGC	
	Signal Name	Signal Type	Signal Name	Signal Type	Signal Name	Signal Type	Signal Name	Signal Type
H33	A1[10]	INPUT	VSS	GND	A1[10]	INPUT	VSS	GND
H34	A1[8]	INPUT	VSS	GND	A1[8]	INPUT	VSS	GND
J20	A1[19]	INPUT	VSS	GND	A1[19]	INPUT	VSS	GND
J21	D1[9]	INPUT	VSS	GND	D1[9]	INPUT	VSS	GND
J22	D1[10]	INPUT	VSS	GND	D1[10]	INPUT	VSS	GND
J23	Q1[10]	OUTPUT	RSVD	RESERVED	Q1[10]	OUTPUT	RSVD	RESERVED
J24	Q1[11]	OUTPUT	RSVD	RESERVED	Q1[11]	OUTPUT	RSVD	RESERVED
J25	D1[12]	INPUT	VSS	GND	D1[12]	INPUT	VSS	GND
J26	Q1[13]	OUTPUT	RSVD	RESERVED	Q1[13]	OUTPUT	RSVD	RESERVED
J28	D1[14]	INPUT	VSS	GND	D1[14]	INPUT	VSS	GND
J29	Q1[14]	OUTPUT	RSVD	RESERVED	Q1[14]	OUTPUT	RSVD	RESERVED
J30	D1[15]	INPUT	VSS	GND	D1[15]	INPUT	VSS	GND
J31	DP1[0]	INPUT	VSS	GND	DP1[0]	INPUT	VSS	GND
J32	QP1[0]	OUTPUT	RSVD	RESERVED	QP1[0]	OUTPUT	RSVD	RESERVED
J33	QP1[1]	OUTPUT	RSVD	RESERVED	QP1[1]	OUTPUT	RSVD	RESERVED
J34	A1[6]	INPUT	VSS	GND	A1[6]	INPUT	VSS	GND
K20	NC/A1[21] ^[28]	NO CONNECT	NC	NO CONNECT	NC/A1[21] ^[28]	NO CONNECT	NC	NO CONNECT
K21	Q1[9]	OUTPUT	RSVD	RESERVED	Q1[9]	OUTPUT	RSVD	RESERVED
K23	D1[11]	INPUT	VSS	GND	D1[11]	INPUT	VSS	GND
K25	Q1[12]	OUTPUT	RSVD	RESERVED	Q1[12]	OUTPUT	RSVD	RESERVED
K26	D1[13]	INPUT	VSS	GND	D1[13]	INPUT	VSS	GND
K30	Q1[15]	OUTPUT	RSVD	RESERVED	Q1[15]	OUTPUT	RSVD	RESERVED
K32	DP1[1]	INPUT	VSS	GND	DP1[1]	INPUT	VSS	GND
K34	IFC1[1]	INPUT	VSS	GND	IFC1[1]	INPUT	VSS	GND
L20	CQ1#	OUTPUT	RSVD	RESERVED	CQ1#	OUTPUT	RSVD	RESERVED
L27	DOFF1#	INPUT	VSS	GND	DOFF1#	INPUT	VSS	GND
M26 ^[29]	VSS ^[29]	GND	VSS ^[29]	GND	VDDQ_J ^[29]	1.8V/2.5V	VDDQ_J ^[29]	1.8V/2.5V
M27 ^[29]	VDDQ_J ^[29]	1.8V/2.5V	VDDQ_J ^[29]	1.8V/2.5V	VSS ^[29]	GND	VSS ^[29]	GND
M28 ^[29]	VDDQ_J ^[29]	1.8V/2.5V	VSS ^[29]	GND	VDDQ_J ^[29]	1.8V/2.5V	VSS ^[29]	GND

Ordering Information

Table 24 provides ordering information.

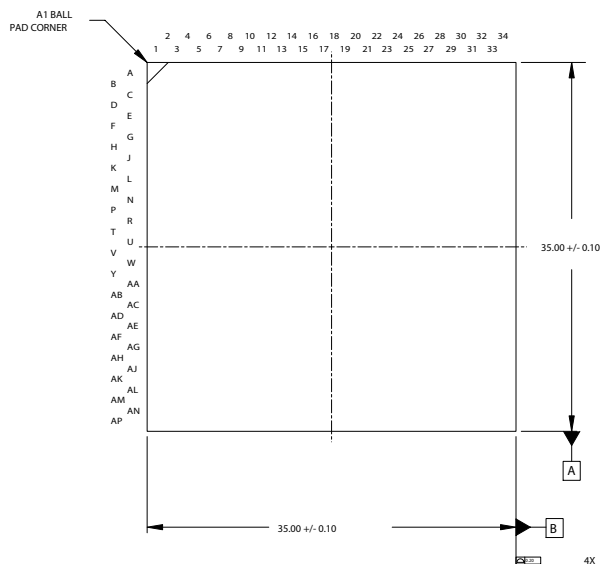
Table 24. Ordering Information

Part Number ^[30, 31]	Description	I/O Voltage	Temperature Range
CYNSE20512-2661FGC	512K x 36-bit Entries NSE with one LA-1 Port	HSTL 1.5V LVCMOS 1.8V/2.5V	Commercial
CYNSE20512-2662FGC	512K x 36-bit Entries NSE with two LA-1 Ports	HSTL 1.5V LVCMOS 1.8V/2.5V	Commercial
CYNSE20512-2001FGC	512K x 36-bit Entries NSE with one LA-1 Port	HSTL 1.5V LVCMOS 1.8V/2.5V	Commercial
CYNSE20512-2002FGC	512K x 36-bit Entries NSE with two LA-1 Ports	HSTL 1.5V LVCMOS 1.8V/2.5V	Commercial
CYNSE20512-1661FGC/I	512K x 36-bit Entries NSE with one LA-1 Port	HSTL 1.5V LVCMOS 1.8V/2.5V	Commercial/Industrial
CYNSE20512-1662FGC/I	512K x 36-bit Entries NSE with two LA-1 Ports	HSTL 1.5V LVCMOS 1.8V/2.5V	Commercial/Industrial
CYNSE20256-2661FGC	256K x 36-bit Entries NSE with one LA-1 Port	HSTL 1.5V LVCMOS 1.8V/2.5V	Commercial
CYNSE20256-2662FGC	256K x 36-bit Entries NSE with two LA-1 Ports	HSTL 1.5V LVCMOS 1.8V/2.5V	Commercial
CYNSE20256-2001FGC	256K x 36-bit Entries NSE with one LA-1 Port	HSTL 1.5V LVCMOS 1.8V/2.5V	Commercial
CYNSE20256-2002FGC	256K x 36-bit Entries NSE with two LA-1 Ports	HSTL 1.5V LVCMOS 1.8V/2.5V	Commercial
CYNSE20256-1661FGC/I	256K x 36-bit Entries NSE with one LA-1 Port	HSTL 1.5V LVCMOS 1.8V/2.5V	Commercial/Industrial
CYNSE20256-1662FGC/I	256K x 36-bit Entries NSE with two LA-1 Port	HSTL 1.5V LVCMOS 1.8V/2.5V	Commercial/Industrial

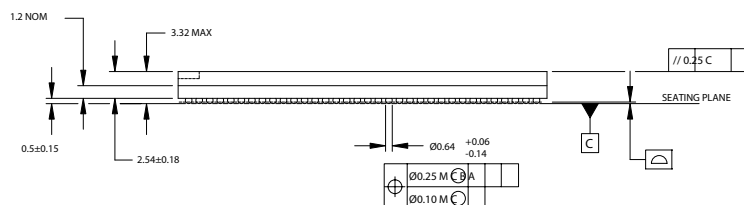
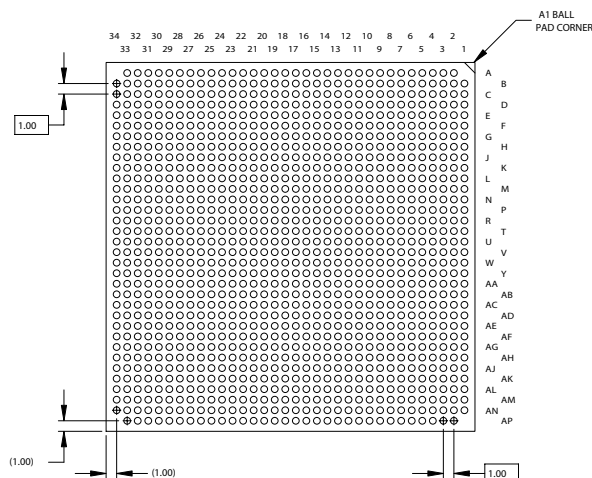
Notes:

30. Extension refers to core speed (266 MHz, 200 MHz, 166 MHz). Refer to Table 13 for the maximum LA-1 operating frequency for each speed bin.

31. Speed bins subject to change.

Package Diagram and Mechanical Information
1152-ball HFC BGA FG1152A
TOP VIEW

BOTTOM VIEW

(1152 SOLDER BALLS)



PACKAGE WEIGHT - 12 grams

 JEDEC PUBLICATION 95
DESIGN GUIDE 4.14

51-85179-*B

QDR RAMs and Quad Data Rate RAMs comprise a new family of products developed by Cypress Semiconductor, Renesas, IDT, NEC, and Samsung. Ayama, FastLink, Mini-Key, Key Capture, No Bus Latency, NoBL, MultiSearch, AgeAssist, Soft Priority, Cynapse and Sahasra are trademarks of Cypress Semiconductor Corporation. All product and company names mentioned in this document may be the trademarks of their respective holders.

Document History Page

Document Title: Ayama™ 20000 Network Search Engine Family Data Sheet Document Number: 38-02075				
REV.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	124600	3/14/03	ITL	New data sheet
*A	128099	10/2/03	NXZ	Eliminated the use of "Ayama 20000" as a noun. Phrases using "Ayama 20000" as a noun have been replaced with "the Ayama 20000 device" or "the Ayama 20000 NSE" Changed "AgeAssist" to "AgeAssist" Updated feature nomenclature; TIB->ADM, SPEAR->APM, dual-bank search->Multi-Search, CC->RA Updated signal descriptions, pin assignment lists, pinout diagrams Added bin information for 266, 200 and 166 Updated LA-1 QDR-II and QDR-II Electrical Characteristics Added section on "AgeAssist" Removed section on Result Delivery Removed section on Depth Cascading Across Blocks Removed ADM register and SRAM offset calculations section Updated Errors section to match Architecture Specification In Overview Corrected the number of BGA pin to 1152-pin BGA package; 1.0 Added different expansion NSE type description; 1.1 Corrected Soft Priority assignable per sub-block; 1.1 Corrected package to 1.0-mm pitch FBGA package; 1.1 Updated <i>Figure 6</i>) 1.1 Added note that Sahasra NSE cannot cascade with other class two devices; 1.1 Removed clock domain from block diagram; 1.2 Added supported transactions section In Pin Description Changed the following pin descriptions: CLK, CLK_MODE, PHS_L, ID[4:04], CFG_L; (Removed following signals from signal description: CFG_L, SINDE[25:24], BW_L[3:0], SCAN_EN, SCAN_MODE, ZQ0, ZQ1; 2.0 Changed INDEX[25:0] to INDEX[23:0] In Functional Description 3.1 rephrased; 3.1.1 tables reorganized; 3.2 inserted new section on cascading multiple Ayama 20000 devices; 3.3 inserted new section on clamshelling QDR devices off 20K; 3.4 rephrased, inserted new diagram on the address space of 20K; 3.4.1 new subsection and diagram on Context Structure; 3.4.2 reorganized and rephrased; 3.4.3 new subsection on transaction initiation; 3.4.3.1 new subsection on Atomic Command sequence; 3.4.4 inserted new subsection on Result reporting; 3.4.4.1 new subsection on empty FIFO indicator; 3.4.5 new subsection on register space; 3.4.6 new subsection on Reading and Writing to a Register; 3.4.7 reorganized and rephrased; 3.5 rephrased and added new diagrams; 3.6 rephrased, reorganized <i>Table 2</i>; 3.6.1 rephrased; 3.6.2 rephrased; 3.8 rephrased, inserted new diagram; 3.9 inserted new section on internal NSE; 3.1.1 rephrased; 3.1.2.3 new subsection on modes of operation; Corrected QDR-II burst 2 will run at 167, 200 and 250 MHz; Atomic Command sequence command; In JTAG Corrected the Initial Value column of Part Number entries to reflect correct values In AC Timing Parameters, Waveforms, and Test Conditions 9.0 Updated latest pinout <i>Figure 16</i>, <i>Figure 18</i>, <i>Figure 19</i> and created new pinout table; Added <i>Figure 21</i>, RA timing waveform In Pin Assignment and Pinout Diagram Added the following pins to the Pin Diagram and the Pin Assignment Table: ZQ0, ZQ1, A0[20], A0[21], A1[20], A1[21]; Moved RA0 and RA1 to C17 AND C18; Reassigned E16 to NC and F16 to Vss; 10.0 Updated the part number from "CYNSE20XXXXXXX-XBGC" to "CYNSE20XXXXXXX-XFGC" in order information table In Ordering Information Added part numbers for the 9-Mbit density of Ayama 20000

Document History Page (continued)

Document Title: Ayama™ 20000 Network Search Engine Family Data Sheet Document Number: 38-02075				
REV.	ECN No.	Issue Date	Orig. of Change	Description of Change
*B	210973	4/14/04	SUA	Removed Table of Contents, List of Figures, List of Tables Changed from single-column to double-column format per Cypress data sheet standard Removed section numbering, reordered sections per standard Cypress data sheet headings Changed section order to follow standard Cypress data sheet practice Replaced "SDRV[1:0]" with "RESERVED" Removed all CLK1X and CLK2X references, added footnote references to Ayama 10000 data sheet In Features Added "APIs ensure ease of table management" Reworded "Error interrupt signals external and internal errors" Removed "Connect up to 31 logical devices" Replaced cascaded NSE figure with linecard diagram In Signal Descriptions Added Signal Type column (LVCMOS/HSTL) Added Voltage Supply VDD_PLL and VSS_PLL for the PLL block Changed SSF, SSV, INDEX[23:0] signals as I/O signals versus purely Input signals In LA-1 Interface Cleaned up diagram with contexts and RAV, RAVA registers Removed figure with RAV, RAVM and RAVA registers Changed size of LA-1 address bus to 20 bits In Errors Added flowchart explaining how to clear EINTR Added fatal/non-fatal status to each error Renamed IERR/DERR Added explanation on error detection on primary/secondary cascade In Clocking Removed CLK1X/CLK2X references Added timing diagram with SDR and DDR clocks In Reset and Power-on Sequence Requirements Added tables explaining signal behavior during reset In Maximum Ratings and Operating Conditions Added junction temperature In AC Timing Parameters, Waveforms and Test Conditions Added max timing parameters for tKHK_LH and tK_LHKH to Table titled LA-1 QDR-II Timing Parameters Updated CL loads for tCKHDV and tCKHDZ; updated tCKHDZ @ 200 MHz in Table titled FastLink AC Timing Parameters. In Signal Assignments and Pinout Diagram Compacted existing table and referred duplicate entries to secondary table Changed 166 speed bin to industrial Removed VDDQ_CONFIG from "Pin Description List" Removed JTAG_ID_Select[2] from "Signal Assignment Differences Between Devices" and assigned it as VSS since it is not customer configurable Assigned D3 to VSS_PLL and E6 to VDD_PLL Included section on "Data Array, Mask Array and Table Widths" Added sections on Mini-Key, Soft Priority and MultiSearch Added a table of interface standards supported with each core frequency bin Added Burst-of-4 Timing Diagram

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Document Title: Ayama™ 20000 Network Search Engine Family Data Sheet Document Number: 38-02075				
REV.	ECN No.	Issue Date	Orig. of Change	Description of Change
*C	241512	See ECN	HFW	All internal functions, details on operations and register information were moved to the device manual The flow of the document was changed The following terms have been revised across the entire document: “72-bit entry” was replaced by “TCAM word” Class-1, Class-2, Primary, Secondary have been simplified to Type-1 and Type-2 Half-rate and full-rate was replaced by DDR and SDR clocking modes. Changes have been made in the following section: The Ayama 20000 interfaces LA-1 command FIFO length was changed from 32 to 16, and the width was changed from 5 bits to 6 bits Reset and Power-on Requirements New names were assigned to parameters in table 3: t_{RESET} was assigned to System Reset while t_{RST_DELAY} was assigned to Software Reset. New parameter, t_{RISE} was created for the rise time of RST_L Added $t_{CHCQ\#H}$, $t_{C\#HCQH}$, $t_{CQ\#HCH}$, $t_{CQHC\#H}$ in QDR-II AC timing table Updated the AC timing table of NoBL SRAM interface Electrical Characteristics and Pin List: V_{DDQ_CONFIG} has been changed to V_{DDQ_J} Multi-Hit to RSVD. HIGH_SPEED1 and HIGH_SPEED2 to V_{DDQ_A} SPS to V_{SS} or V_{DDQ_J} SCMDV[1:0] to SCMDV(remaining signal is labeled as reserved) SADR[23:0] to AD_SADR[23:0] SDATA[3:0] to AD_SDATA[3:0] SDATAP[3:0] to AD_SDATAP[3:0] CE_L to AD_CE_L WE_L to AD_WE_L PHS_L_10k to PHS_OUT_L PHS_SEL driven HIGH (tied to V_{DDQ_A}) PHS_L driven LOW (tied to V_{SS}) NSEVREF, HSVREF, both labeled as NSEVREF VREF max on LA-1 interface was changed from 0.95V to 0.9V to comply with JEDEC 8-6 spec HSTL VDDQ was changed from 1.8V and 1.5V versions to 1.5V version only Sections of tables containing current consumption (IDD) values were removed SRAM and FastLink figures were updated for clarity; timing parameters updated Added industrial temperature grade

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Document Title: Ayama™ 20000 Network Search Engine Family Data Sheet Document Number: 38-02075				
REV.	ECN No.	Issue Date	Orig. of Change	Description of Change
*D	293013	See ECN	TNT	Functional Description <i>Figure 2:</i> Changed application diagram from Linecard to typical NPU_based search subsystem Added explanation of the max. number of outstanding contexts limited by the data/command FIFO. Features Added Associated Data Management feature Updated MultiSearch description with MultiWidth MultiSearch, added example and Updated <i>Figure 9</i> with example Fixed working on Clamshelling feature description Pinlist Changed AP2 from RSVD to TERM, with instruction to terminate per the FastLink interface I/O standard Changed AP5 from EOT to RSVD Changed AL3 from RSVD to HIGH_SPEEDO_L Changed M25 from Vss to HIGH_SPEEDI_L Added description for HIGH_SPEEDI_L and HIGH_SPEEDO_L Changed all references to NSEVREF, SRAMVREF and QDRVREF to NSEREF, SRAMREF, QDRREF. Changed their description from reference voltage to analog input Changed F16 from VSS to TEST_PB. Added description that it must be driven for JTAG testing Added external pulldown requirement for SSV, SSSV Changed resistor combination for weak bias from 65 and 170 ohms, to 70 and 165 ohms Added description to LHI, BHI to tie LOW and FULI to tie HIGH when Ayama 20000 is first device in cascade Changed PHS_OUT_L description to indicate that it's driven LOW when in DDR clocking mode VDDQ_J supply was previously only 2.5V, but was changed to 2.5V or 1.8V Ayama 20000 Interfaces LA-1 interface: Changed 16-bit data transfer, plus four bits of even byte parity, to 32-bit data transfer, plus four bits of even byte parity LA-1 interface: Added note to explain that the two LA-1 port frequencies are independent LA-1 interface: <i>Figure 4</i> CMD FIFO width corrected to five bits, not six bits SRAM interface: Changed from 266-MHz HSTL to 200 MHz for both HSTL and LVCMOS SRAM interface: Added explanation of half-rate clocking FastLink interface: Changed <i>Figure 5</i> to reflect Type-1 and 2, vs. Class 1 and 2 Features Changed soft-priority field from eight bits to six bits Clocking <i>Figure 14:</i> Ayama 20000 clocks. Inverted phase of DDR Clock, added description Added description of restrictions on core clocking above 200 MHz Reset Changed t_{RST_DELAY} from 500 us to 1024 K clock cycles of the slowest LA-1 port Changed t_{RESET} from 500 us to 100 us Added note that no delay required after soft reset Voltages VDDQ_J supply was previously only 2.5V, but was changed to 2.5V or 1.8V Capacitance Changed max Cin (FastLink and SRAM) to 10 pF, added max Cin for LA-1 of 4 pF Removed Cout definition AC Timing <i>Table 13:</i> Changed SRAM interface max operating frequency from 266 MHz to 200 MHz <i>Table 13:</i> Changed QDR-II max. operating speed from 166 to 200 MHz for -166 speed bin <i>Table 14:</i> Added note explaining QDR timing's relationship to speed bins <i>Table 14:</i> Removed 166-MHz timing numbers; all offered parts meet 200 or 250MHz timing <i>Table 14:</i> QDR-II timing: t_{KHKKH} max cycle time set to 7.5 ns for all speed bins <i>Table 14:</i> QDR-II timing: Changed t_{AVKH}, t_{IVKH}, t_{KHAX}, t_{KHIX} from 0.5 to 0.4 ns

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Document Title: Ayama™ 20000 Network Search Engine Family Data Sheet Document Number: 38-02075				
REV.	ECN No.	Issue Date	Orig. of Change	Description of Change
*D cont	293013	See ECN	TNT	AC Timing (contd) Table 14: QDR-II timing: Changed t_{COHQZ}, t_{COHQX1} description from C HIGH to output HIGH/LOWZ to CQ HIGH to output HIGH/LOWZ Table 16: QDR-II: Figure 19: Renamed t_{KHK_LH} to $t_{KHK\#H}$, t_{K_LHKH} to $t_{K\#HKH}$, and t_{CHHQV} to t_{COHQV} Updated footnote references in Table 15–Table18 Added Table 17: CLK timing parameters Table 18: FastLink: Added note that timing applies to rising edge of CLK if in SDR mode, or either rising or falling edge of CLK in DDR mode Table 18: FastLink: Added cascade signal timing t_{IS_HIT}, t_{IS_FUL}, t_{IH_HIT}, t_{IH_FUL}, t_{CKHOH_HIT}, t_{CKHOH_FUL}, t_{CKHOH_F}, t_{CKCDV_HIT}, t_{CKCDV_FUL}, t_{CKHDV_F}, t_{CKHDV_E} Table 18: FastLink: Added t_{ISIND}, t_{IHIND}, t_{CKHOH_CMD}, t_{CQHDV_PHS}, t_{CKHDV_CMD}, t_{CKHOH_E} parameters Table 18, 29: Moved t_{CKHZD}, t_{CKHZD_AD} parameters to MIN column instead of MAX Table 19 and 20: AC test parameters: Added note on test condition $T_j = 85^\circ\text{C}$ Added Table 21: JTAG timing Redrew RA Vector, FastLink and SRAM timing diagrams for clarity Signal Assignments Pin H30 changed to VDDQ_Q; previously the single-ported options had this pin labelled VSS while the dual-ported devices had this pin labelled VDDQ_Q Other pinout changes described under 'Pinlist' description are also updated Corrected INDEX[23:0], ACK, PARERR_L, SSV, SSF to be I/O, not INPUT Corrected D1[1], D0[8], D0[7] to be INPUT, not OUTPUT Corrected BHO[2], AD_SADR, AD_CE_L, AD_WE_L to OUTPUT, not OUTPUT-T Corrected K8 description from QDR0REF0-2 to QDR0REF0 References to VDDQ_JTAG changed to VDDQ_J for consistency References to VDDQ_QDR changed to VDDQ_Q for consistency References to VDDQ_ASIC changed to VDDQ_A for consistency References to VDDQ_SRAM changed to VDDQ_S for consistency Fixed Figure 29 to include columns 33 and 34

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Document Title: Ayama™ 20000 Network Search Engine Family Data Sheet Document Number: 38-02075				
REV.	ECN No.	Issue Date	Orig. of Change	Description of Change
*E	391333	See ECN	TNT	Pin Descriptions Changed TMS, TDI and TRST_L descriptions to show internal weak pullup. Changed pin name and description: HIGH_SPEEDO_L to HS_PWRSERVE. Edited description to require an inverter only above 200 MHz. Added requirement that C, C# clocks are driven. Added power rail to each pin's description. Remove QDRI option. Changed DOFFn_L pin description to require it driven HIGH, removing QDRI references. Changed IFCx[1:0] to remove QDRI references. Edited ID and TEST_PB pin levels description to include LVCMOS and HSTL. Changed Footnotes 3 and 4 on signals requiring weak bias HIGH and LOW to only recommend biasing for terminated lines. Core clocking Changed estimated max. core clocking frequency to 220MHz. Cascading for Storage Modified Table 2: Operation and Features for Cascaded Type-1 devices table to show the number of Cascaded devices, not the total number of NSEs cascaded. Advanced Power Management Removed this feature from datasheet, no software support Reset Removed comment that if C clock is not active then K must be running during reset. JTAG Removed table with JTAG device IDs, refer to BSDL model for information. Speed-Bin to Interface Speed Mapping Changed bin2 (-200MHz part) QDR interface timing to 235 MHz, retaining the 250MHz AC parameters. Electrical Specs Added Maximum Ratings Section. Operating Conditions V_{REF} set to V_{DDQ_X/2} Junction temperature range of 0 to 110°C added. Capacitance C_{IN_LA1} max changed from 4 pF to 5 pF. C_{IN_FastLink} max changed from 10 pF to 18 pF. Electrical Characteristics Broke out AC and DC output HIGH and LOW levels. LA-1 interface Added Data valid and hold time parameters for RA signal. QDR-II mode Added KC_Var input clock jitter requirement Added maximum clock cycle time to provide lower-limit on QDRII LA-1 frequency. Changed t_{KHKL}, t_{KLKH} 250MHz from 1.6 to 1.75ns Changed t_{KHCH_MIN} 250MHz from 0 to 0.45ns Changed input setup time t_{AVKH}, t_{DVKH} 250MHz from 0.4 to 0.3ns Changed input setup time t_{DVKH} 200 MHz from 0.5 to 0.6ns per LA-1 spec Changed input hold time t_{KHAX}, 200/250MHz from 0.4/0.6 to 0.55/0.65ns Changed input hold time t_{KHDX}, 200/250MHz from 0.4/0.5 to 0.55/0.65ns Changed input hold time t_{KHIX}, 200/250MHz from 0.4/0.5 to 0.6/0.65ns Changed C to output valid time t_{CHQV} 200/250MHz from 0.45/0.45 to 0.7/0.75ns Changed C to echo clock valid time t_{CHCOV} 200/250MHz from 0.40/0.45 to 0.55/0.5ns Changed CQ to output valid time t_{CQHCV} 200/250MHz from 0.35/0.3 to 0.5/0.47ns Changed C to output hold time t_{CHQX} 200/250MHz from -0.45/-0.45 to -0.4/-0.3ns Changed C to echo clock hold time t_{CHCOX} 250MHz from -0.4 to -0.3ns Changed CQ to output hold time t_{CQHGX} 200/250MHz from -0.35/-0.3 to -0.55, -0.45ns t_{C#HCQH}, t_{CQHCO#H}, t_{CQ#HCH}, t_{CHCQ#H} removed as they are not in LA-1B spec. Added t_{RADV} and t_{RADH} parameters Modified Figure 16, 18, 19 and 20 to better align timing diagrams with device timing specs. FastLink Changed clock HIGH/LOW time specs to duty cycle requirements.

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REV.	ECN No.	Issue Date	Orig. of Change	Description of Change
*E... cont	391333	See ECN	TNT	Broke out t_{ISCH_DQ} from t_{ISCH} for 166/200/266MHz, changed from 1.1/0.95/0.85ns to 0/0/0ns Changed t_{ISCH} for 166/200/266MHz from 1.1/0.95/0.85ns to 0.9/0.75/0.65ns Broke out t_{IHCH_DQ} from t_{IHCH} for 166/200/266MHz, changed from 0.7/0.6/0.6ns to 0.7/0.6/0.55ns Changed t_{IHCH} for 166/200/266MHz from 0.7/0.6/0.6ns to 0.85/0.75/0.7ns Changed t_{ISIND} for 166/200/266MHz from 1/0.85/0.75ns to 1/0.95/0.85ns Changed t_{IHIND} for 166/200/266MHz from 0.7/0.6/0.6ns to 0.9/0.8/0.7ns Changed t_{IS_FUL} for 200 MHz from 1.5ns to 1.8ns Broke out t_{CKHOH_HSTL} and t_{CKHOH_CMOS}. Changed 166/200/266MHz spec from 0.6/0.6/0.8ns to 0.7/0.8/0.95 for HSTL and 0.4/0.5ns for LVCMOS. Changed t_{CKHOH_CMD} for 166/200/266MHz from 0.6/0.6/0.8ns to 1/0.95/0.85ns Changed t_{CKHOH_PHS} for 166/200/266MHz from 1/1/1ns to 0.8/0.9/1.1ns Changed t_{CKHOH_FUL} for 166/200/266MHz from 1.2/1.2/1.2ns to 1/1.1/1.2ns Changed t_{CKHOH_E} for 166/200/266MHz from 0.6/0.6/0.8ns to 0.3/0.4/0.5ns Broke out t_{CKHDV_HSTL} and t_{CKHDV_CMOS}. Changed 166/200/266MHz spec from 3.3/3.0/2.55ns to 3.3/3.1/3.0 for HSTL and 2.9/2.75ns for LVCMOS. Changed t_{CKHDV_CMD} for 166/200/266MHz from 3.3/2.9/2.5ns to 2.6/2.4/2.3ns Changed t_{CKHDV_PHS} for 166/200/266MHz from 3.3/2.7/2.4ns to 3.1/2.9/2.8ns Changed t_{CKHDV_HIT} for 166/200/266MHz from 3.9/3.4/2.6ns to 4.3/3.4/3.4ns Changed t_{CKHDV_FUL} for 166/200/266MHz from 7/6.5/5.8ns to 7.4/6.5/6.2ns Changed t_{CKHDV_F} for 166/200/266MHz from 3.5/3/2.6ns to 3.6/3.4/3ns Changed t_{CKHDV_E} for 166/200/266MHz from 3.15/2.75/2.4ns to 2.6/2.4/2.2ns SRAM Changed t_{IS_AD} for 166/200LVCMOS/200HSTL from 0.96/0.8/0.6ns to 0.95/0.6/0.6ns Changed t_{IH_AD} for 166/200LVCMOS/200HSTL from 0.7/0.6/0.6ns to 1/0.85/0.85ns Changed t_{CKHDV_AD} for 166/200LVCMOS/200HSTL from 3.15/2.75/2.4ns to 2.7/2.0/2.4ns Changed t_{OH_AD} for 166/200LVCMOS/200HSTL from 0.6/0.6/0.7ns to 0.3/0.45/0.65ns Changed t_{CKHDZ_AD} for 166/200LVCMOS/200HSTL from 3.15/2.75/2.4ns to 2.7/2.0/2.4ns Changed t_{CKHZD_AD} for 166/200LVCMOS/200HSTL from 0.6/0.6/0.7ns to 0.3/0.45/0.65ns Test Conditions Updated T_j from 85 to 110°C. Updated notes clarifying which parameters are not tested in production testing. JTAG Timing Changed t_{TDOX} from 10ns max to 0ns min. Pinout Added Interposer pins: NC/INT_VDD and NC/INT_VSS. Added footnote explaining their use.