

SN54ALS857, SN74ALS857 HEX 2-TO-1 UNIVERSAL MULTIPLEXERS WITH 3-STATE OUTPUTS

SDAS170A – DECEMBER 1982 – REVISED JANUARY 1995

- Select True or Complementary Data
- Perform AND/NAND (Masking) of A or B Operand
- Cascadable to Expand Number of Operands
- Detect Zeros on A or B Operands
- 3-State Outputs Interface Directly With System Bus
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

description

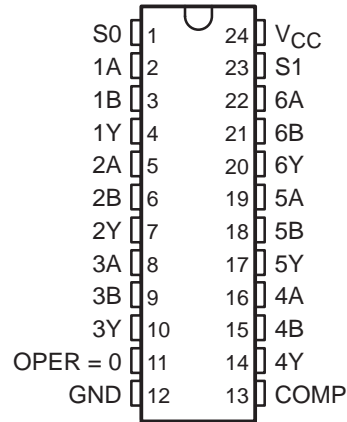
The 'ALS857 are hextuple 2-line to 1-line multiplexers with 3-state outputs. The devices can provide either true (COMP low) or inverted (COMP high) data at the Y outputs. In addition, the 'ALS857 perform the logical AND function ($A \cdot B$) and the clear function as well. The four modes of operation are:

- Select A-data inputs
- Select B-data inputs
- AND A inputs with B inputs
- Clear

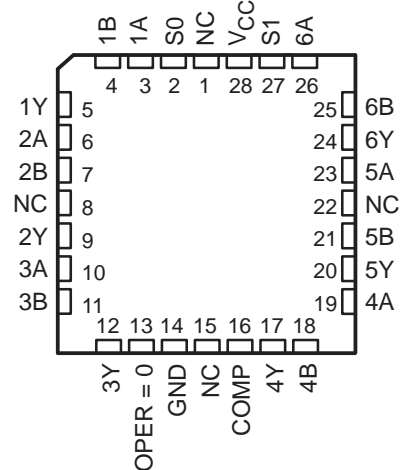
In either of the first two modes, OPER = 0 is high if all the selected A or B inputs are low. The six Y outputs and the OPER = 0 output are all 3-state and rated at 12-mA and 24-mA I_{OL} for the SN54ALS857 and SN74ALS857, respectively. All outputs can be placed in the high-impedance state by applying a high level to the COMP, S0, and S1 inputs simultaneously.

The SN54ALS857 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS857 is characterized for operation from 0°C to 70°C .

SN54ALS857 . . . JT PACKAGE
SN74ALS857 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS857 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

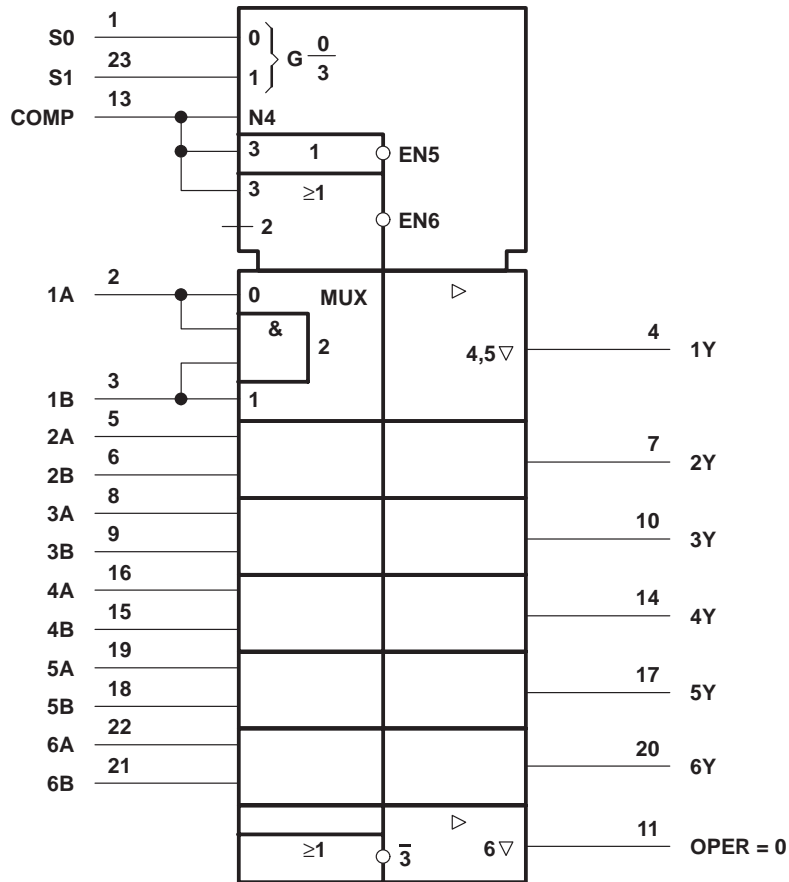
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FUNCTION TABLE

INPUTS			OUTPUTS	
COMP	S1	S0	Y	OPER = 0
L	L	L	A	H = all A inputs L
L	L	H	B	H = all B inputs L
L	H	L	$A \cdot B$	Z
L	H	H	L	L
H	L	L	\bar{A}	H = all A inputs L
H	L	H	\bar{B}	H = all B inputs L
H	H	L	$\overline{A \cdot B}$	Z
H	H	H	Z	Z

logic symbol†

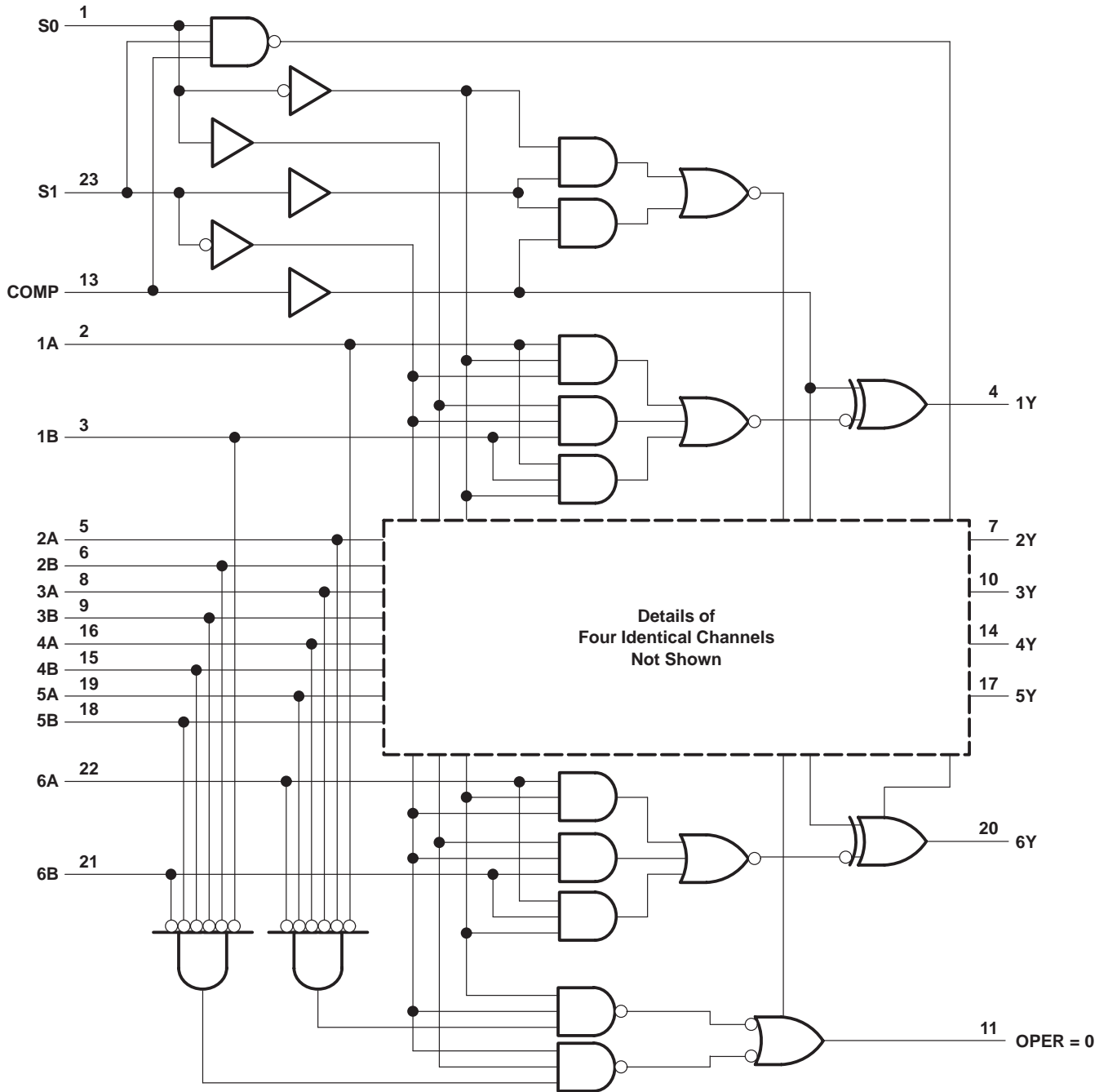


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DW, JT, and NT packages.

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logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A : SN54ALS857	–55°C to 125°C
SN74ALS857	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54ALS857			SN74ALS857			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			–1			–2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS857			SN74ALS857			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = 4.5 V$,	$I_I = -18 mA$			–1.5			–1.5	V
V_{OH}	$V_{CC} = 4.5 V$ to $5.5 V$,	$I_{OH} = -0.4 mA$	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5 V$	$I_{OH} = -1 mA$	2.4	3.3					
		$I_{OH} = -2.6 mA$			2.4	3.2			
V_{OL}	$V_{CC} = 4.5 V$	$I_{OL} = 12 mA$	0.25	0.4	0.25	0.4		V	
		$I_{OL} = 24 mA$			0.35	0.5			
I_{OZH}	$V_{CC} = 5.5 V$,	$V_O = 2.7 V$			20		20	μA	
I_{OZL}	$V_{CC} = 5.5 V$,	$V_O = 0.4 V$			–20		–20	μA	
I_I	$V_{CC} = 5.5 V$,	$V_I = 7 V$			0.1		0.1	mA	
I_{IH}	$V_{CC} = 5.5 V$,	$V_I = 2.7 V$			20		20	μA	
I_{IL}	$V_{CC} = 5.5 V$,	$V_I = 0.4 V$			–0.2		–0.2	mA	
$I_{O\text{§}}$	$V_{CC} = 5.5 V$,	$V_O = 2.25 V$	–15		–70	–15		–70	mA
I_{CC}	$V_{CC} = 5.5 V$, See Note 1	Outputs high	11	24	11	24		mA	
		Outputs low	16	33	16	33			
		Outputs disabled	18	36	18	36			

‡ All typical values are at $V_{CC} = 5 V$, $T_A = 25^\circ C$.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

NOTE 1: I_{CC} is measured with all possible inputs grounded while achieving the stated output conditions.



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switching characteristics (see Figure 1)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX‡				UNIT
			SN54ALS857		SN74ALS857		
			MIN	MAX	MIN	MAX	
t _{pd}	A or B (COMP high)	Y (inverting)	2	35	4	25	ns
	A or B (COMP low)	Y (noninverting)	2	27	4	18	
	S0 or S1	Y	2	37	7	33	
	COMP		2	26	6	18	
	A or B	OPER = 0	2	45	5	37	
	S0 to S1		2	30	5	23	
t _{en}	S0 to S1	Y	2	38	7	35	ns
t _{dis}			2	43	2	23	
t _{en}	COMP	Y	2	37	8	24	ns
t _{dis}			2	45	6	21	
t _{en}	S0	OPER = 0	2	29	6	20	ns
t _{dis}			2	42	11	27	
t _{en}	S1	OPER = 0	2	28	6	25	ns
t _{dis}			2	37	3	19	
t _{en}	COMP	OPER = 0	2	43	9	25	ns
t _{dis}			2	36	6	20	

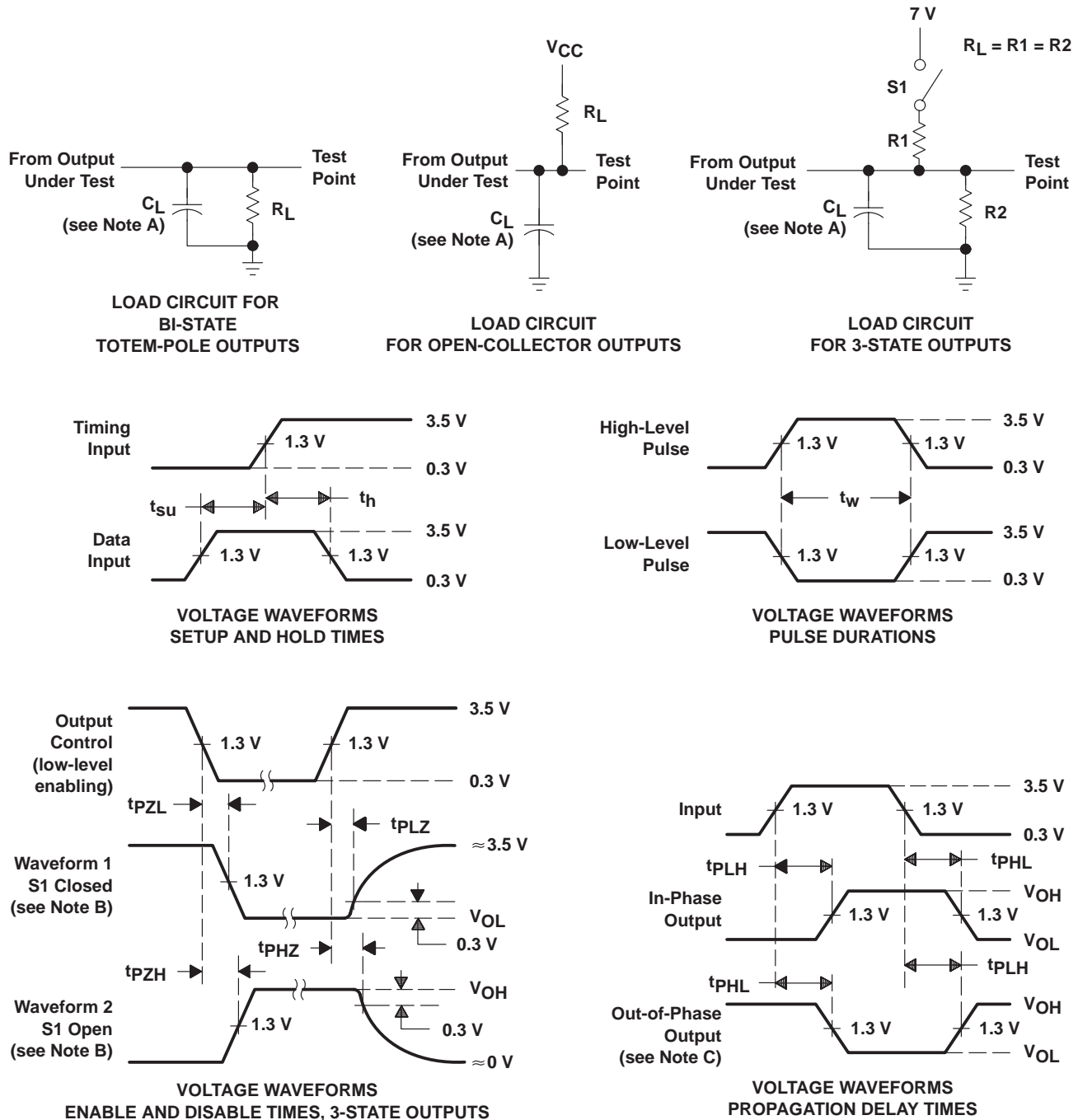
† t_{pd} = t_{PLH} or t_{PHL}; t_{en} = t_{PZH} or t_{PZL}; t_{dis} = t_{PHZ} or t_{PLZ}

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-87533013A	OBSOLETE	LCCC	FK	24		TBD	Call TI	Call TI
5962-8753301LA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
SN74ALS857NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS857NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SNJ54ALS857FK	OBSOLETE	LCCC	FK	24		TBD	Call TI	Call TI
SNJ54ALS857JT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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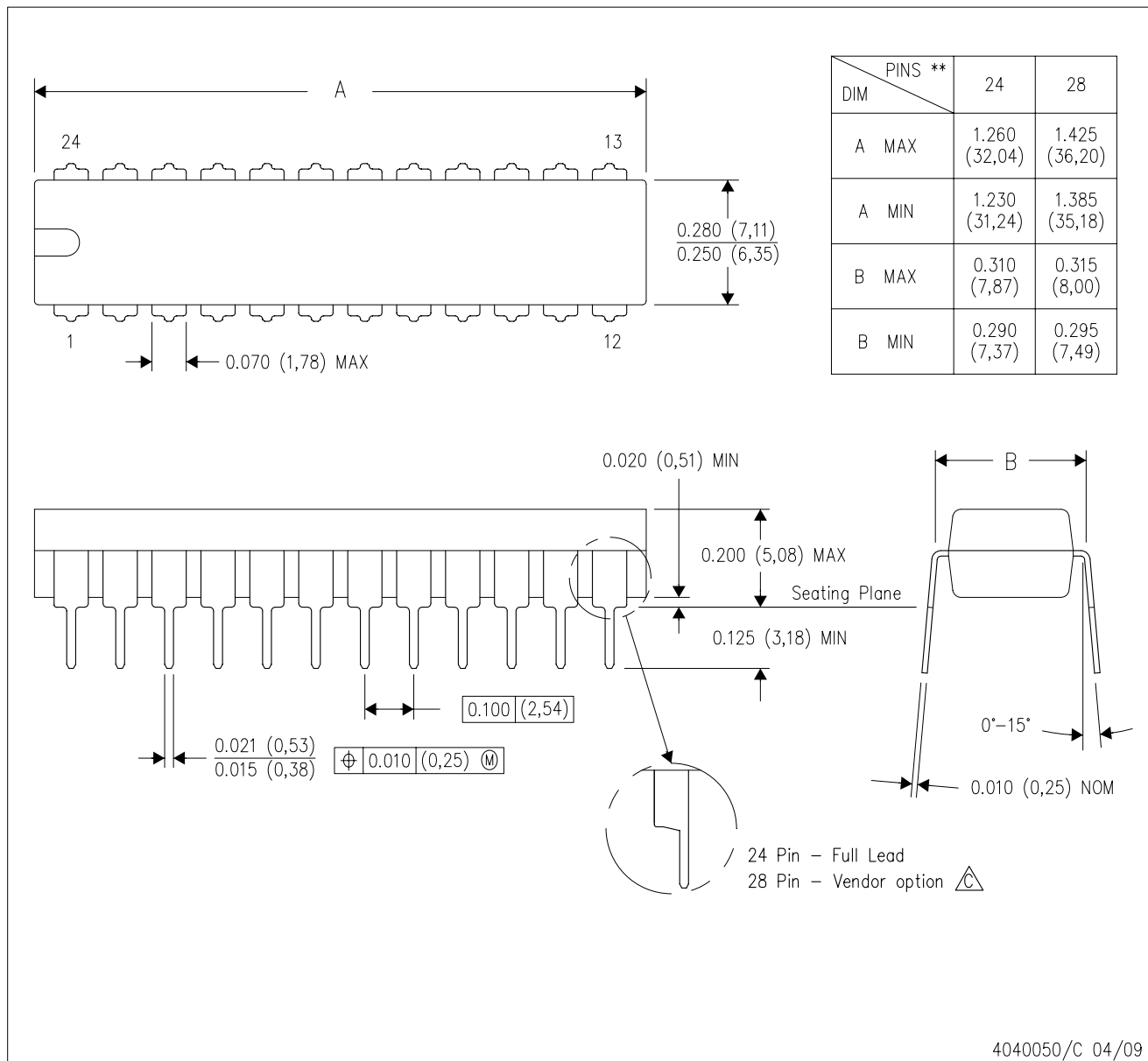
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MECHANICAL DATA

NT (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN

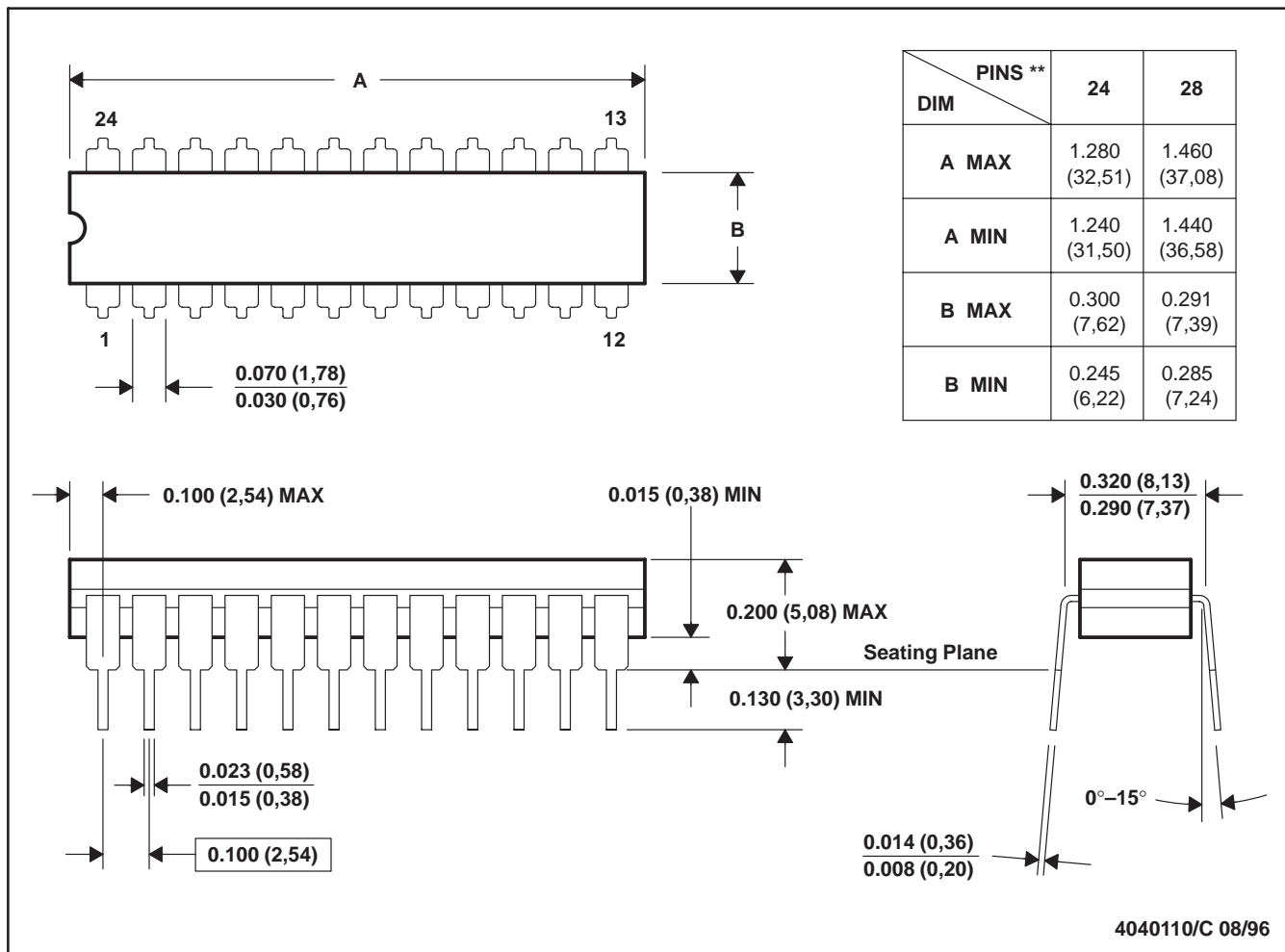


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  The 28 pin end lead shoulder width is a vendor option, either half or full width.

JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

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