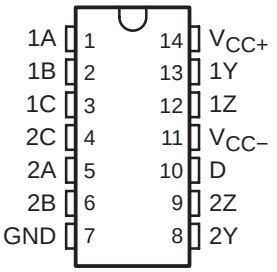
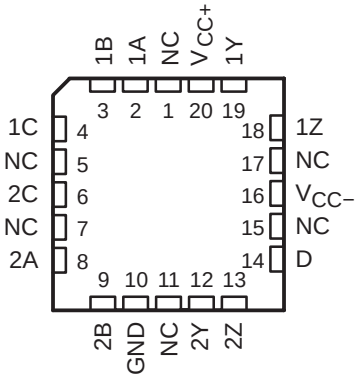
- **Improved Stability Over Supply Voltage and Temperature Ranges**
- **Constant-Current Outputs**
- **High Speed**
- **Standard Supply Voltages**
- **High Output Impedance**
- **High Common-Mode Output Voltage Range . . . −3 V to 10 V**
- **TTL-Input Compatibility**
- **Inhibitor Available for Driver Selection**
- **Glitch Free During Power Up/Power Down**
- **SN75112 and External Circuit Meets or Exceeds the Requirements of CCITT Recommendation V.35**

SN55110A . . . J OR W PACKAGE
SN75110A . . . D, N, OR NS PACKAGE
SN75112 . . . D OR N PACKAGE
(TOP VIEW)



SN55110A . . . FK PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

The SN55110A, SN75110A, and SN75112 dual line drivers have improved output current regulation with supply-voltage and temperature variations. In addition, the higher current of the SN75112 (27 mA) allows data to be transmitted over longer lines. These drivers offer optimum performance when used with the SN55107A, SN75107A, and SN75108A line receivers.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (N)	Tube of 25	SN75110AN	SN75110AN
			SN75112N	SN75112N
	SOIC (D)	Tube of 50	SN75110AD	SN75110A
		Reel of 2500	SN75110ADR	
		Tube of 50	SN75112D	SN75112
		Reel of 2500	SN75112DR	
	SOP (NS)	Reel of 2000	SN75110ANSR	SN75110A
−55°C to 125°C	CDIP (J)	Tube of 25	SN55110AJ	SN55110AJ
			SNJ55110AJ	SNJ55110AJ
	CFP (W)	Tube of 150	SNJ55110AW	SNJ55110AW
	LCCC (FK)	Tube of 55	SNJ55110AFK	SNJ55110AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

description/ordering information (continued)

These drivers feature independent channels with common voltage supply and ground terminals. The significant difference between the three drivers is in the output-current specification. The driver circuits feature a constant output current that is switched to either of two output terminals by the appropriate logic levels at the input terminals. The output current can be switched off (inhibited) by low logic levels on the enable inputs. The output current nominally is 12 mA for the ’110A devices and is 27 mA for the SN75112.

The enable/inhibit feature is provided so the circuits can be used in party-line or data-bus applications. A strobe or inhibitor (enable D), common to both drivers, is included for increased driver-logic versatility. The output current in the inhibited mode, $I_{O(off)}$, is specified so that minimum line loading is induced when the driver is used in a party-line system with other drivers. The output impedance of the driver in the inhibited mode is very high. The output impedance of a transistor is biased to cutoff.

The driver outputs have a common-mode voltage range of −3 V to 10 V, allowing common-mode voltage on the line without affecting driver performance.

All inputs are diode clamped and are designed to satisfy TTL-system requirements. The inputs are tested at 2 V for high-logic-level input conditions and 0.8 V for low-logic-level input conditions. These tests ensure 400-mV noise margin when interfaced with TTL Series 54/74 devices.

The SN55110A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN75110A and SN75112 are characterized for operation from 0°C to 70°C.

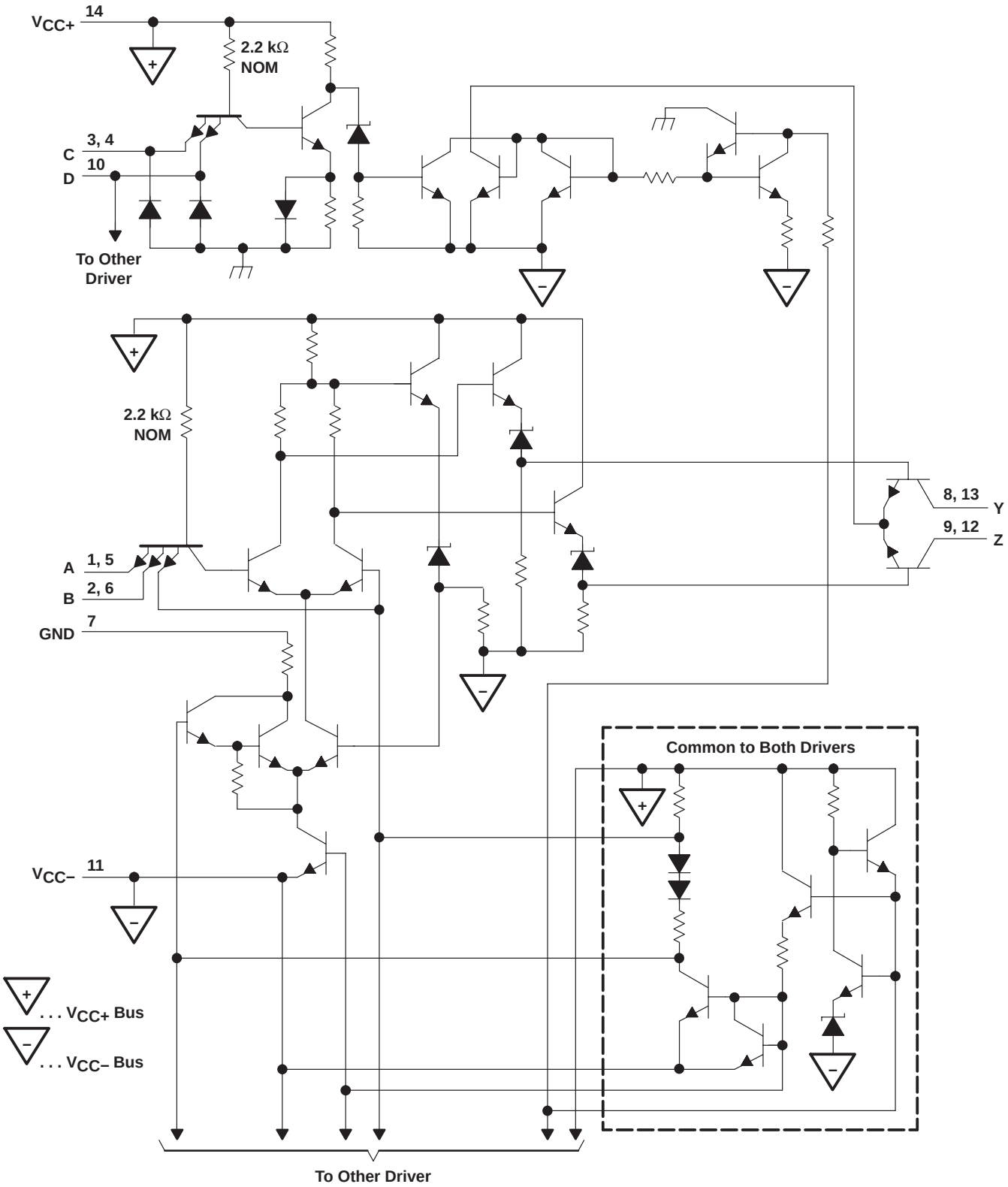
FUNCTION TABLE
(each driver)

LOGIC INPUTS		ENABLE INPUTS		OUTPUTS†	
A	B	C	D	Y	Z
X	X	L	X	Off	Off
X	X	X	L	Off	Off
L	X	H	H	On	Off
X	L	H	H	On	Off
H	H	H	H	Off	On

H = high level, L = low level, X = irrelevant

† When using only one channel of the line drivers, the other channel should be inhibited and/or have its outputs grounded.

schematic (each driver)



Pin numbers shown are for the D, J, N, NS, and W packages.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage: V_{CC+} (see Note 1) . . . . . 7 V
V_{CC-} (see Note 1) . . . . . −7 V
Input voltage, V_I . . . . . 5.5 V
Output voltage range, V_O . . . . . −5 V to 12 V
Package thermal impedance, θ_{JA} (see Notes 2 and 3): D package . . . . . 86°C/W
N package . . . . . 80°C/W
NS package . . . . . 76°C/W
Package thermal impedance, θ_{JC} (see Notes 4 and 5): FK package . . . . . 13.42°C/W
J package . . . . . 15.05°C/W
W package . . . . . 14.65°C/W
Operating virtual junction temperature . . . . . 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package . . . . . 300°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. Maximum power dissipation is a function of $T_J(max)$, θ_{JC}, and T_C. The maximum allowable power dissipation at any allowable case temperature is $P_D = (T_J(max) - T_C)/\theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
5. The package thermal impedance is calculated in accordance with MIL-STD-883.

recommended operating conditions (see Note 6)

		SN55110A			SN75110A SN75112			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC+}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{CC-}	Supply voltage	−4.5	−5	−5.5	−4.75	−5	−5.25	V
	Positive common-mode output voltage	0		10	0		10	V
	Negative common-mode output voltage	0		−3	0		−3	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level output voltage			0.8			0.8	V
T_A	Operating free-air temperature	−55		125	0		70	°C

NOTE 6: When using only one channel of the line drivers, the other channel should be inhibited and/or have its outputs grounded.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN55110A SN75110A			SN75112			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage		$V_{CC\pm}$ = MIN, I_L = −12 mA		−0.9	−1.5		−0.9	−1.5	V
$I_{O(on)}$	On-state output current		$V_{CC\pm}$ = MAX, V_O = 10 V		12	15		27	40	mA
			V_{CC} = MIN to MAX, V_O = −1 V to 1 V, T_A = 25°C				24	28	32	
			$V_{CC\pm}$ = MIN, V_O = −3 V	6.5	12		15	27		
$I_{O(off)}$	Off-state output current		$V_{CC\pm}$ = MIN, V_O = 10 V			100			100	μA
I_I	Input current at maximum input voltage	A, B, or C inputs	$V_{CC\pm}$ = MAX, V_I = 5.5 V			1			1	mA
		D input				2			2	
I_{IH}	High-level input current	A, B, or C inputs	$V_{CC\pm}$ = MAX, V_I = 2.4 V			40			40	μA
		D input				80			80	
I_{IL}	Low-level input current	A, B, or C inputs	$V_{CC\pm}$ = MAX, V_I = 0.4 V			−3			−3	mA
		D input				−6			−6	
$I_{CC+(on)}$	Supply current from V_{CC} with driver enabled		$V_{CC\pm}$ = MAX, A and B inputs at 0.4 V, C and D inputs at 2 V		23	35		25	40	mA
$I_{CC-(on)}$	Supply current from V_{CC-} with driver enabled		$V_{CC\pm}$ = MAX, A and B inputs at 0.4 V, C and D inputs at 2 V		−34	−50		−65	−100	mA
$I_{CC+(off)}$	Supply current from V_{CC-} with driver inhibited		$V_{CC\pm}$ = MAX, A, B, C, and D inputs at 0.4 V		21			30		mA
$I_{CC-(off)}$	Supply current from $V_{CC\pm}$ with driver inhibited		$V_{CC\pm}$ = MAX, A, B, C, and D inputs at 0.4 V		−17			−32		mA

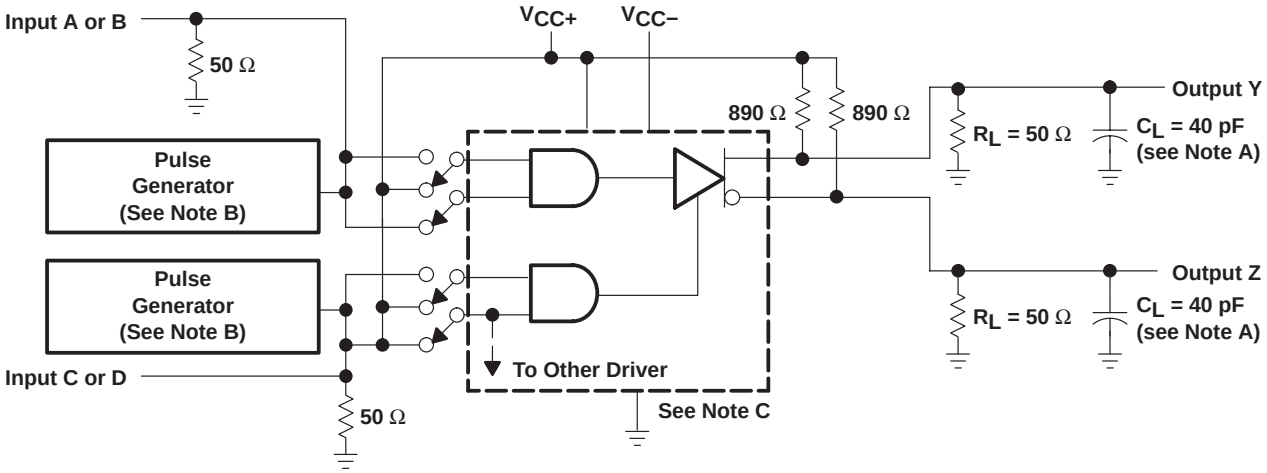
† For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

switching characteristics, $V_{CC\pm}$ = ±5 V, T_A = 25°C (see Figure 1)

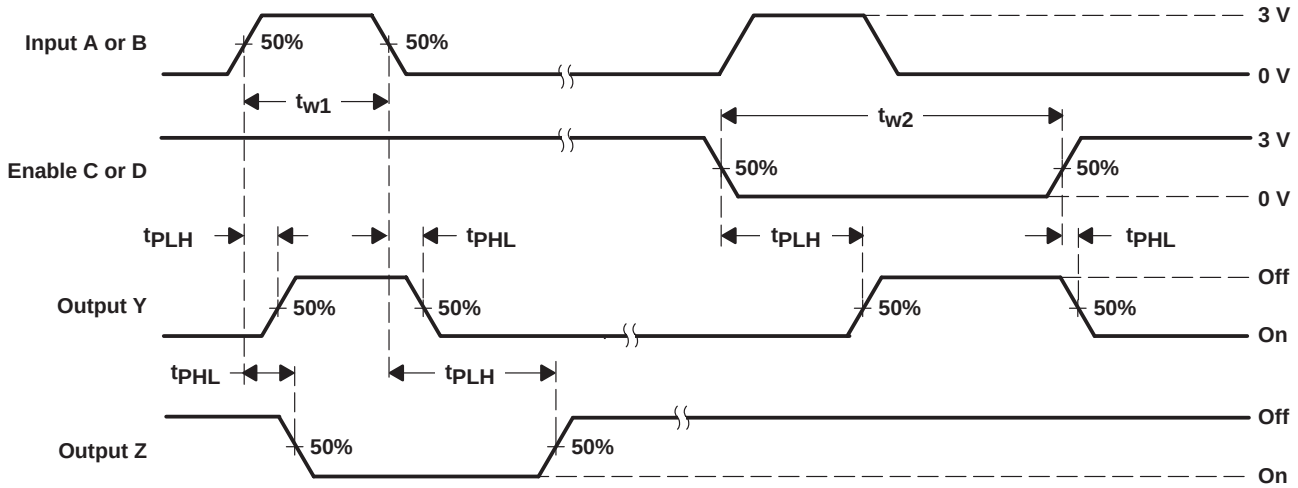
PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y or Z	C_L = 40 pF, R_L = 50 Ω,		9	15	ns
t_{PHL}					9	15	
t_{PLH}	C or D	Y or Z	C_L = 40 pF, R_L = 50 Ω,		16	25	ns
t_{PHL}					13	25	

§ t_{PLH} = propagation delay time, low- to high-level output
t_{PHL} = propagation delay time, high- to low-level output

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generators have the following characteristics: $Z_O = 50\ \Omega$, $t_r = t_f = 10 \pm 5$ ns, $t_{w1} = 500$ ns, PRR ≤ 1 MHz, $t_{w2} = 1\ \mu s$, PRR ≤ 500 kHz.
C. For simplicity, only one channel and the enable connections are shown.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

SN55110A, SN75110A
ON-STATE OUTPUT CURRENT
vs
NEGATIVE SUPPLY VOLTAGE

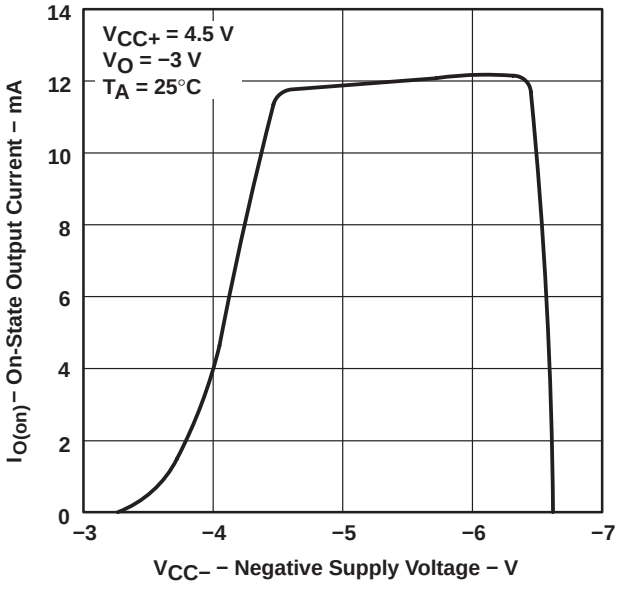


Figure 2

SN75112
ON-STATE OUTPUT CURRENT
vs
NEGATIVE SUPPLY VOLTAGE

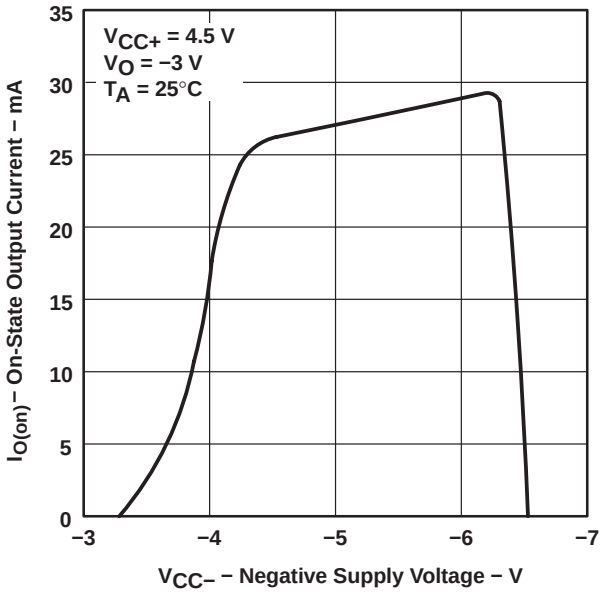


Figure 3

APPLICATION INFORMATION

special pulse-control circuit

Figure 4 shows a circuit that can be used as a pulse-generator output or in many other testing applications.

INPUT A	OUTPUTS Y	OUTPUTS Z
High	Off	On
Low	On	Off

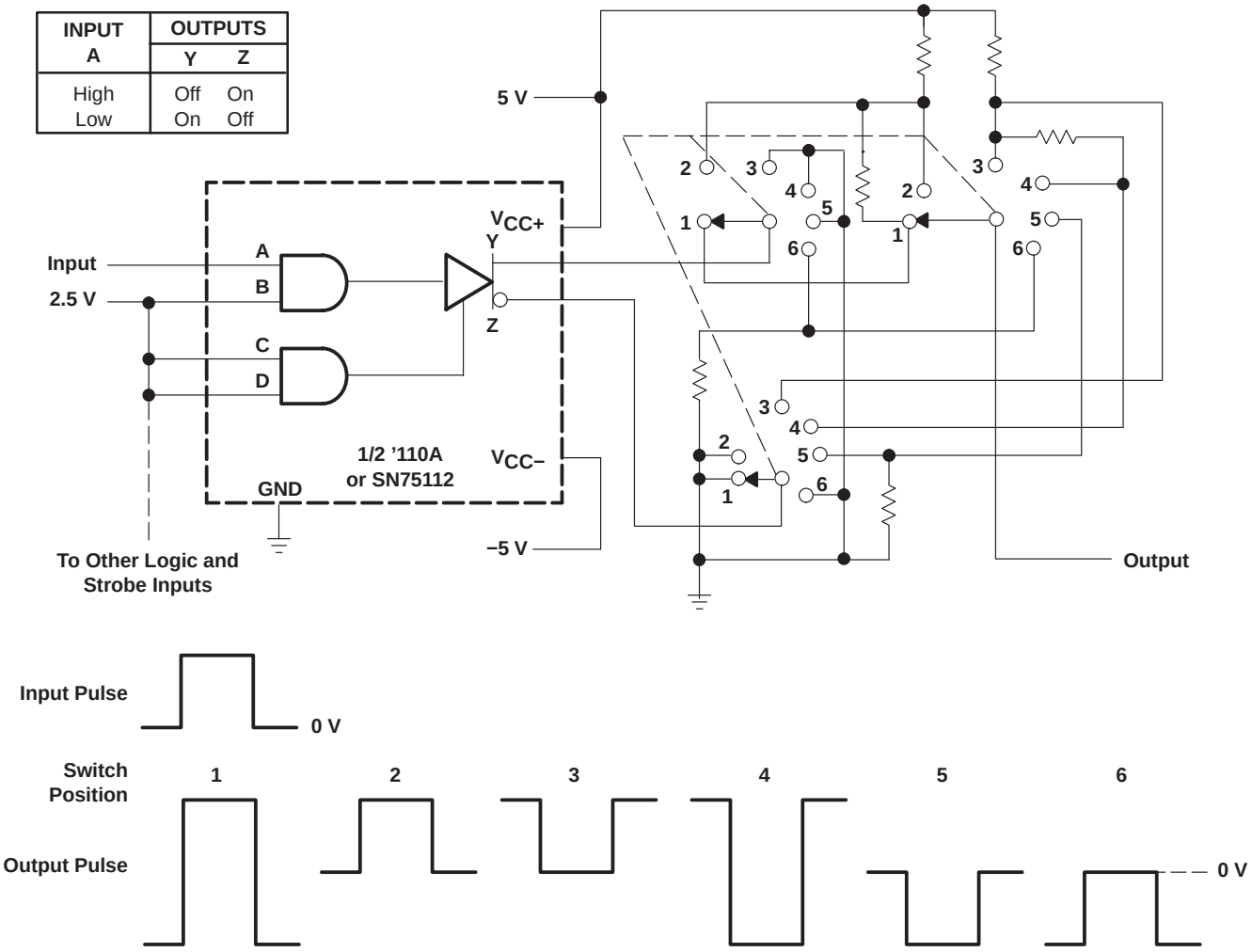


Figure 4. Pulse-Control Circuit

APPLICATION INFORMATION

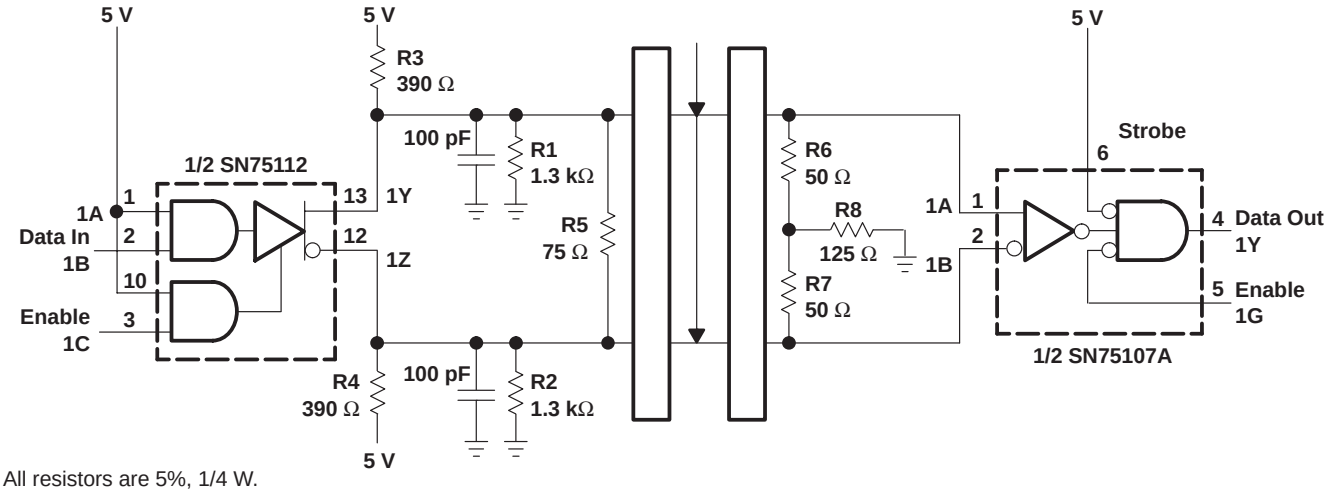
using the SN75112 as a CCITT-recommended V.35 line driver

The SN75112 dual line driver, the SN75107A dual line receiver, and some external resistors can be used to implement the data-interchange circuit of CCITT recommendation V.35 (1976) modem specification. The circuit of one channel is shown in Figure 5 and meets the requirement of the interface as specified by Appendix 11 of CCITT V.35 and is summarized in Table 1 (V.35 has been replaced by ITU V.11).

Table 1. CCITT V.35 Electrical Requirements

GENERATOR	MIN	MAX	UNIT
Source impedance, Z_{source}	50	150	Ω
Resistance to ground, R	135	165	Ω
Differential output voltage, V_{OD}	440	660	mV
10% to 90% rise time, t_r	40		ns
or		0.01 × ui†	
Common-mode output voltage, V_{OC}	−0.6	0.6	V
LOAD (RECEIVER)	**MIN**	**MAX**	**UNIT**
Input impedance, Z_I	90	110	Ω
Resistance to ground, R	135	165	Ω

† ui = unit interval or minimum signal-element pulse duration



All resistors are 5%, 1/4 W.

Figure 5. CCITT-Recommended V.35 Interface Using the SN75112 and SN75107A

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-87547012A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-87547012A SNJ55 110AFK
5962-8754701CA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8754701CA SNJ55110AJ
5962-8754701DA	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8754701DA SNJ55110AW
SN55110AJ	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN55110AJ
SN55110AJ.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN55110AJ
SN75110AD	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75110A
SN75110AD.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75110A
SN75110ADR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75110A
SN75110ADR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75110A
SN75110AN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75110AN
SN75110AN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75110AN
SN75110ANSR	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75110A
SN75110ANSR.A	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75110A
SN75112D	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75112
SN75112D.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75112
SN75112DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75112
SN75112DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75112
SN75112N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75112N
SN75112N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75112N
SNJ55110AFK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-87547012A SNJ55 110AFK
SNJ55110AFK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-87547012A SNJ55 110AFK

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ55110AJ	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8754701CA SNJ55110AJ
SNJ55110AJ.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8754701CA SNJ55110AJ
SNJ55110AW	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8754701DA SNJ55110AW
SNJ55110AW.A	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8754701DA SNJ55110AW

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN55110A, SN75110A :

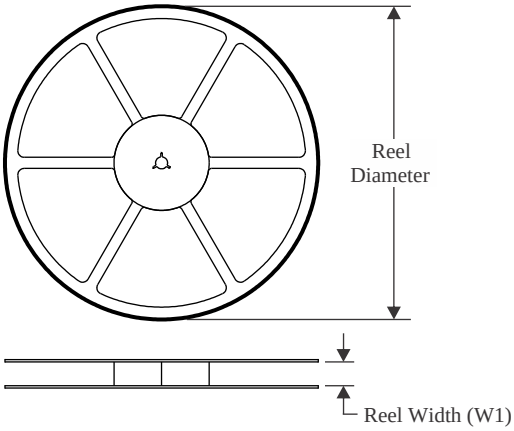
- Catalog : SN75110A
- Military : SN55110A

NOTE: Qualified Version Definitions:

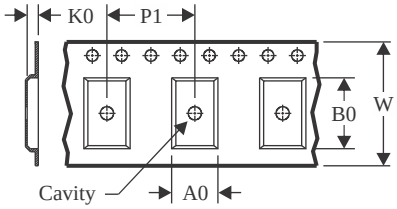
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

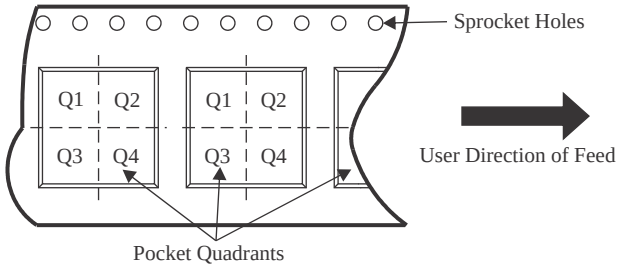


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

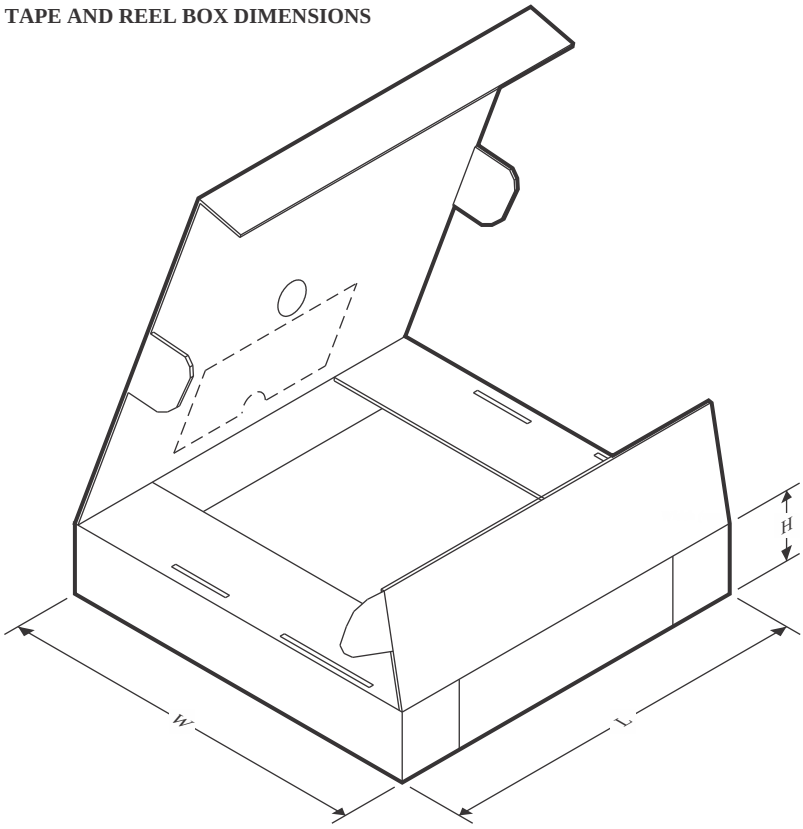
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75110ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN75110ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN75110ANSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN75112DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

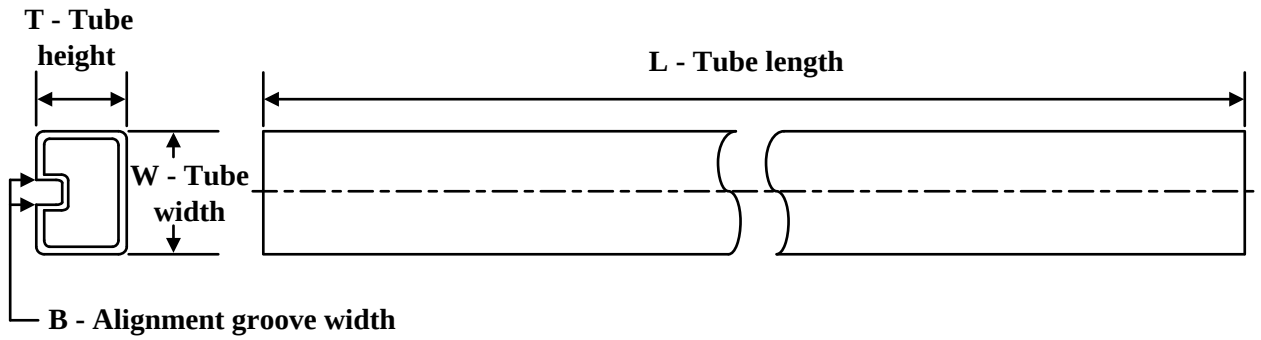
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

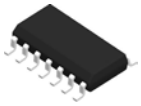
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75110ADR	SOIC	D	14	2500	353.0	353.0	32.0
SN75110ADR	SOIC	D	14	2500	340.5	336.1	32.0
SN75110ANSR	SOP	NS	14	2000	353.0	353.0	32.0
SN75112DR	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-87547012A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8754701DA	W	CFP	14	25	506.98	26.16	6220	NA
SN75110AD	D	SOIC	14	50	506.6	8	3940	4.32
SN75110AD.A	D	SOIC	14	50	506.6	8	3940	4.32
SN75110AN	N	PDIP	14	25	506	13.97	11230	4.32
SN75110AN	N	PDIP	14	25	506	13.97	11230	4.32
SN75110AN.A	N	PDIP	14	25	506	13.97	11230	4.32
SN75110AN.A	N	PDIP	14	25	506	13.97	11230	4.32
SN75112D	D	SOIC	14	50	506.6	8	3940	4.32
SN75112D.A	D	SOIC	14	50	506.6	8	3940	4.32
SN75112N	N	PDIP	14	25	506	13.97	11230	4.32
SN75112N.A	N	PDIP	14	25	506	13.97	11230	4.32
SNJ55110AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ55110AFK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ55110AW	W	CFP	14	25	506.98	26.16	6220	NA
SNJ55110AW.A	W	CFP	14	25	506.98	26.16	6220	NA

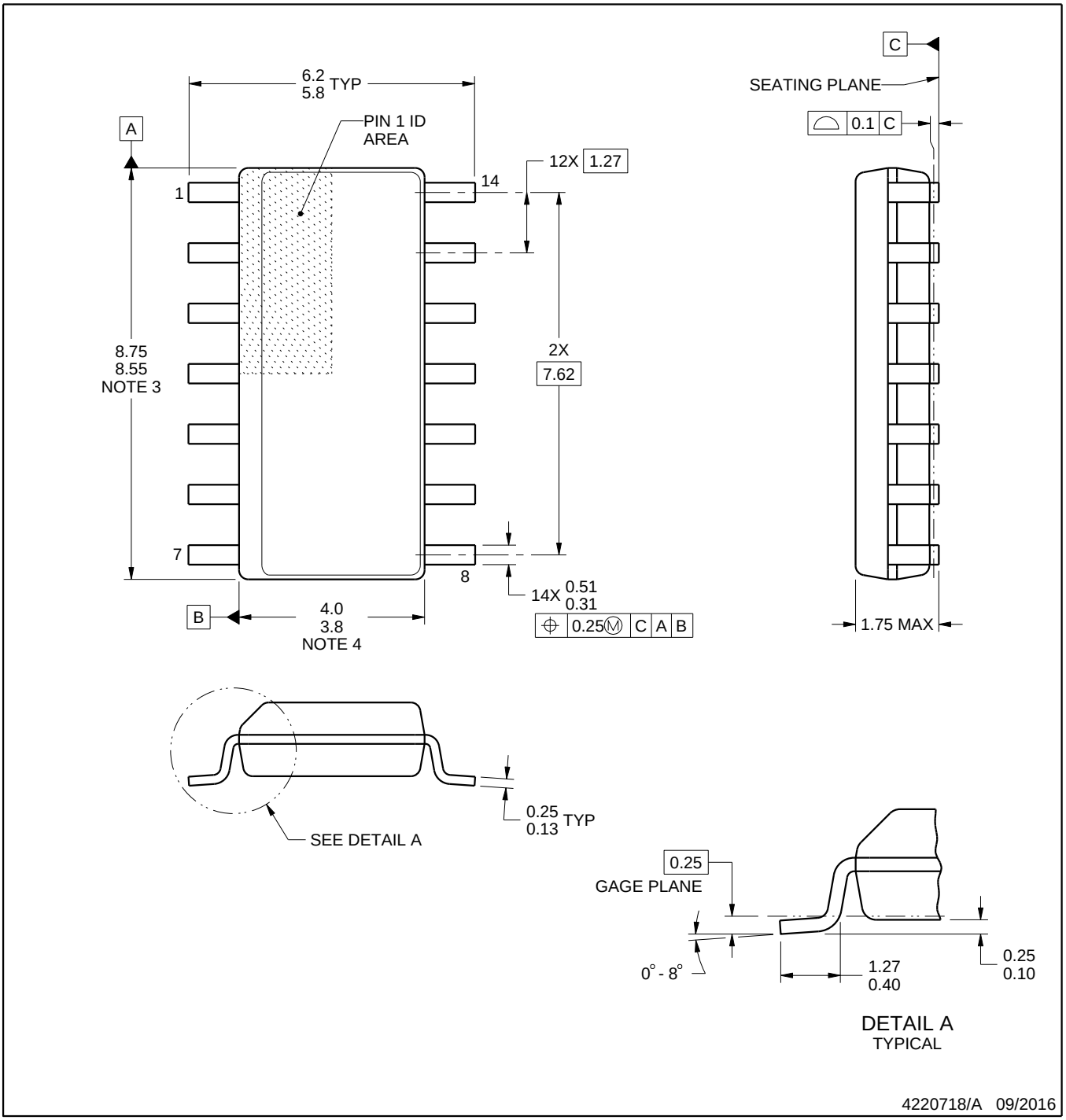


PACKAGE OUTLINE

D0014A

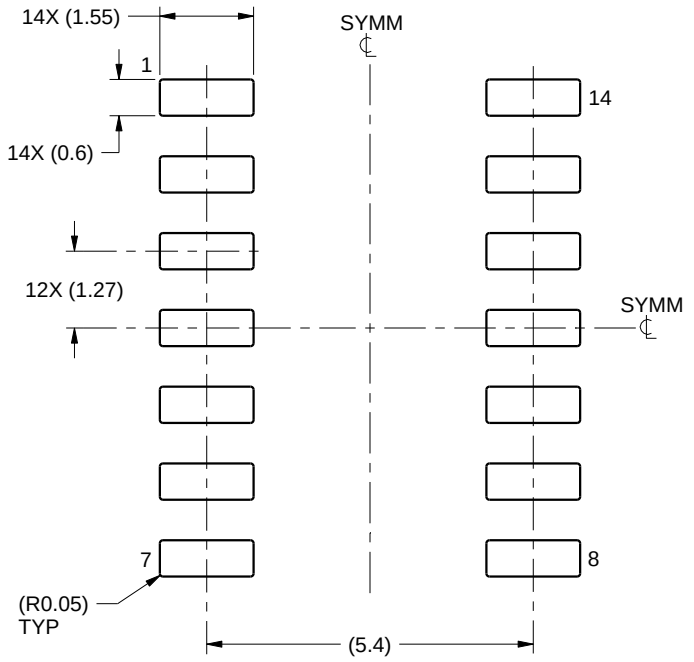
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

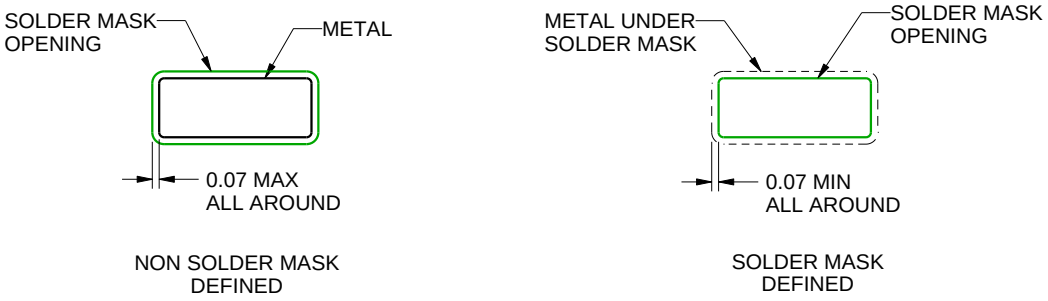


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

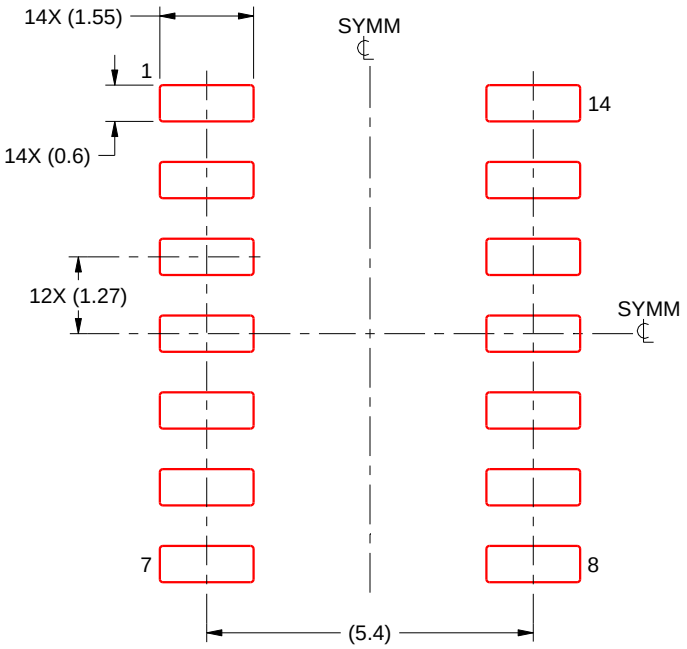
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

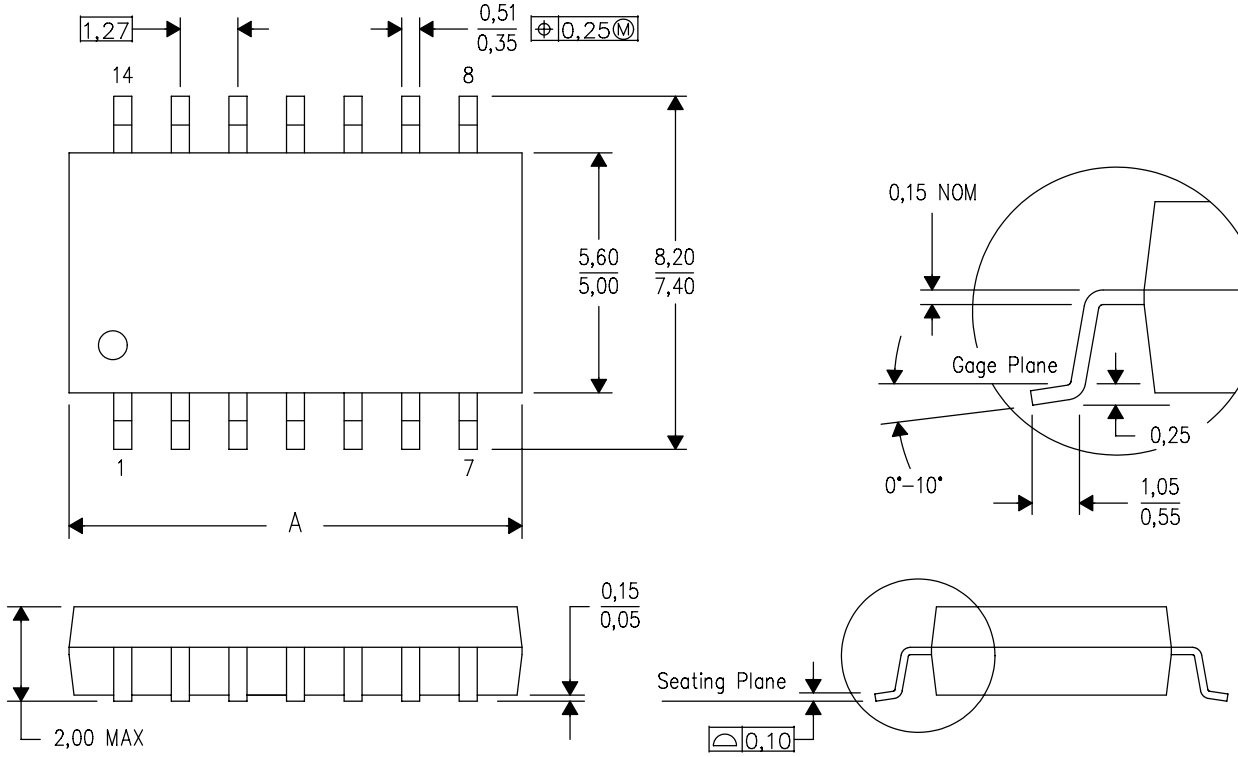
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

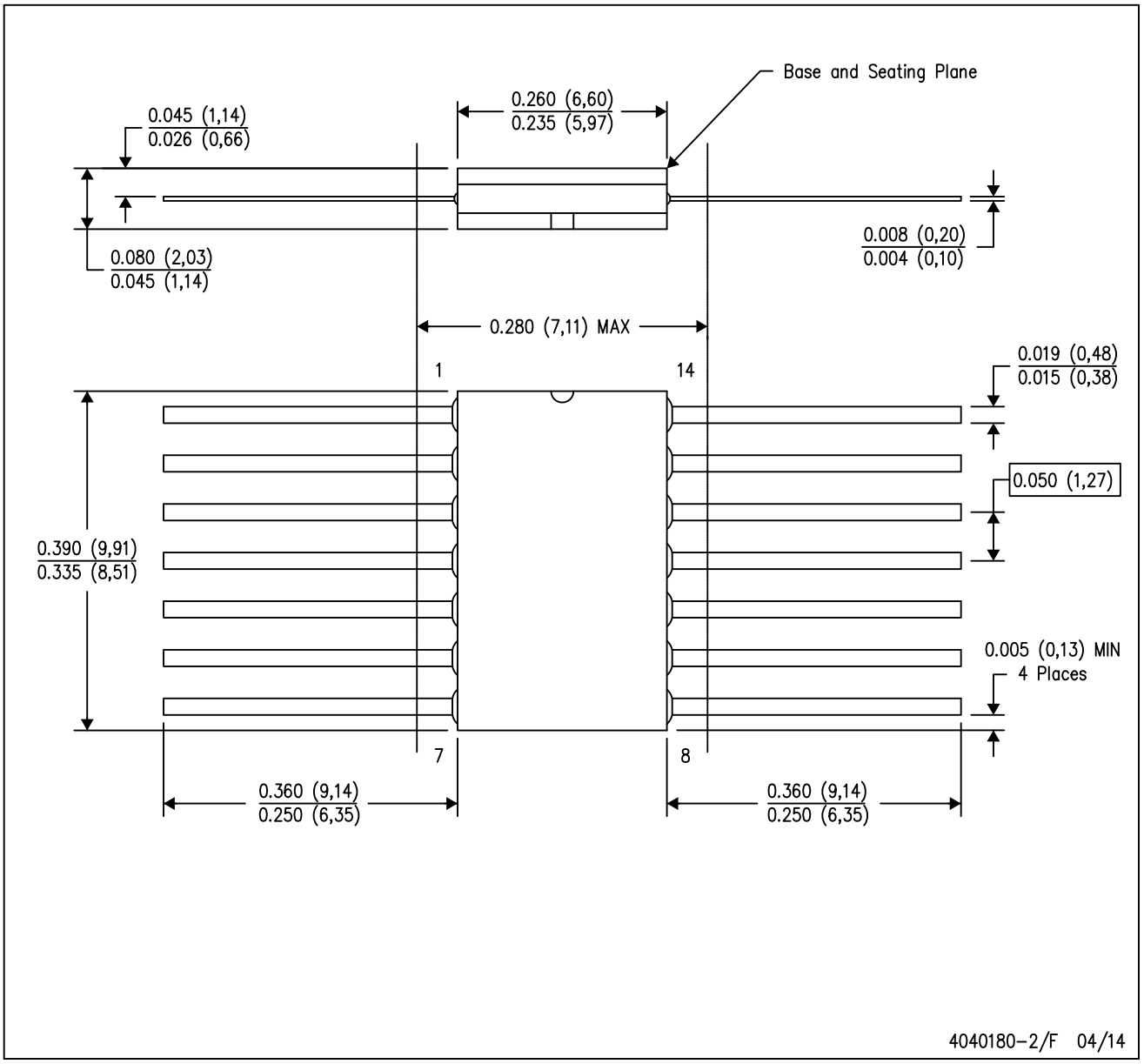


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

GENERIC PACKAGE VIEW

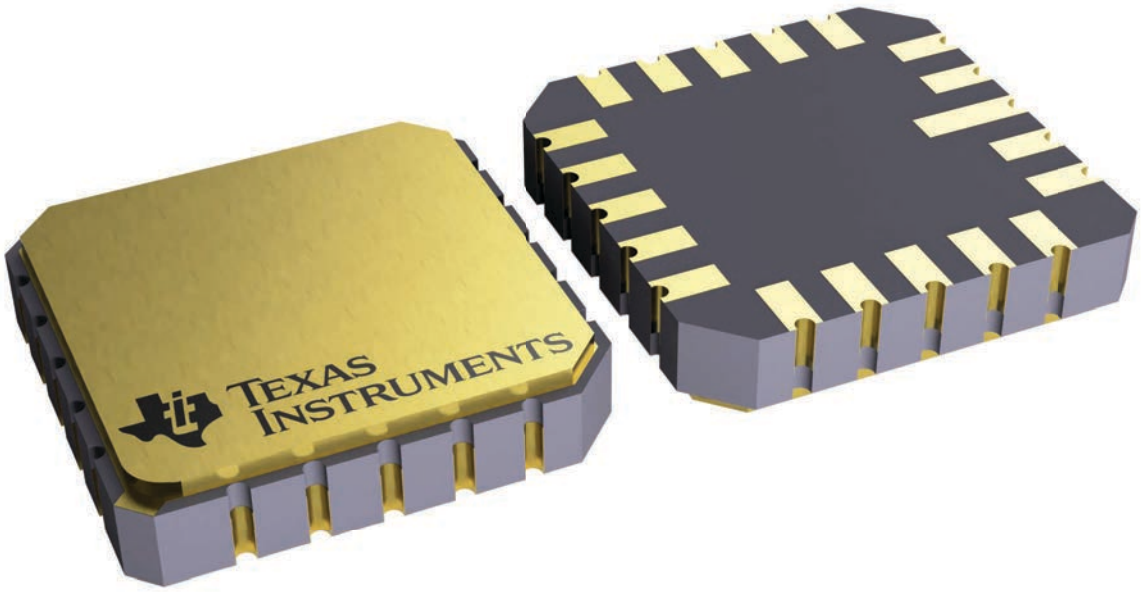
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

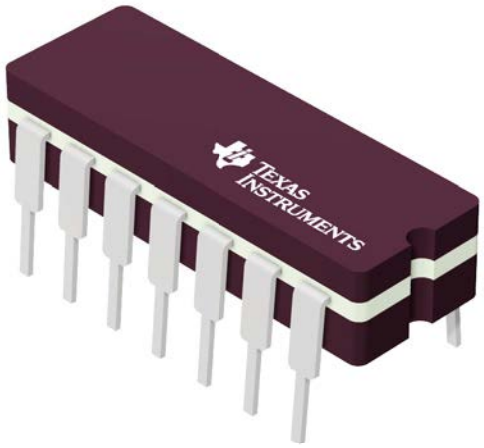


4229370VA\

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

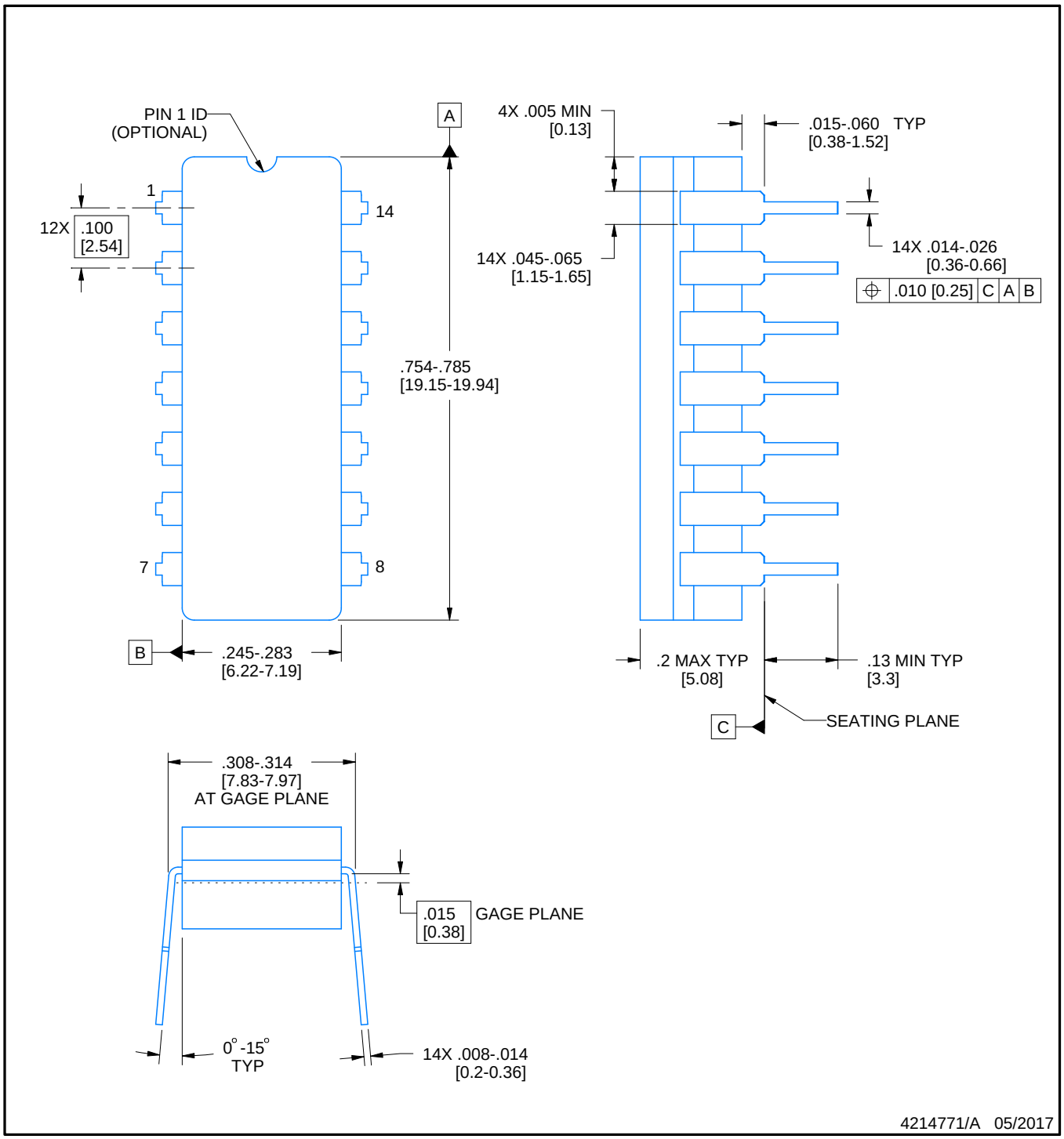
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

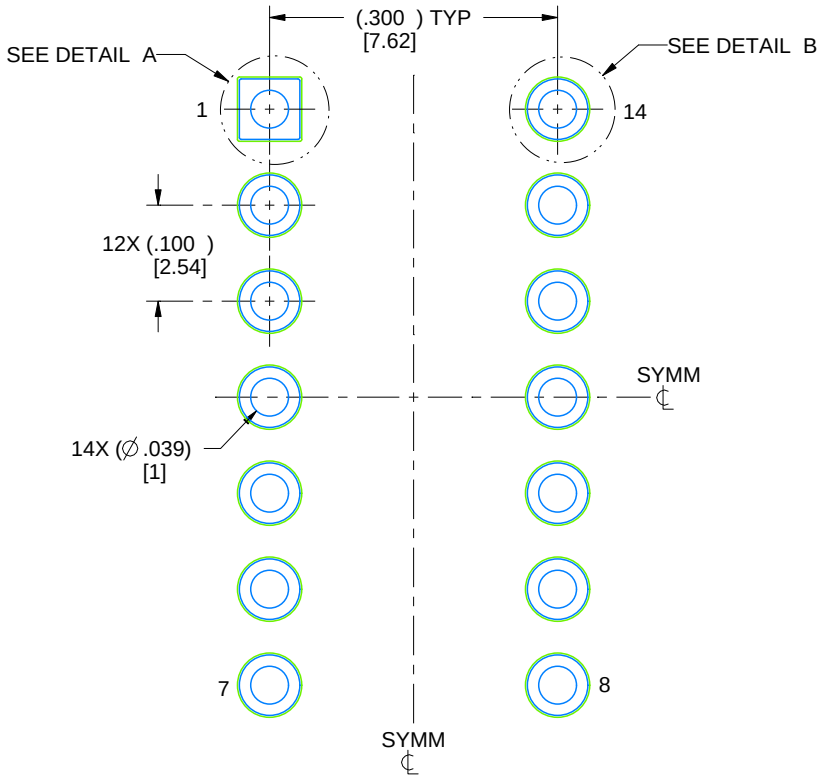
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

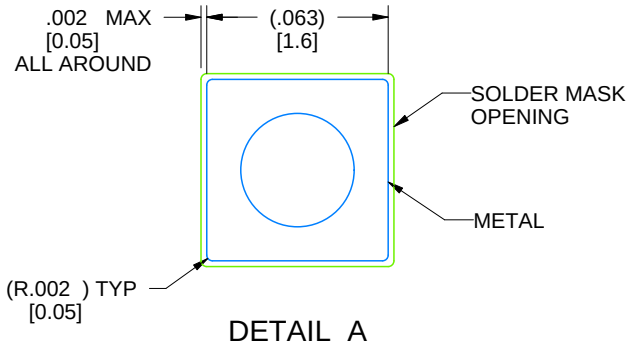
J0014A

CDIP - 5.08 mm max height

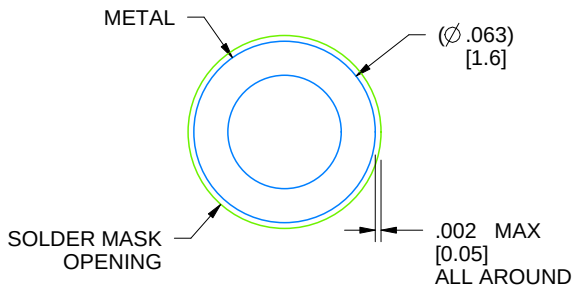
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



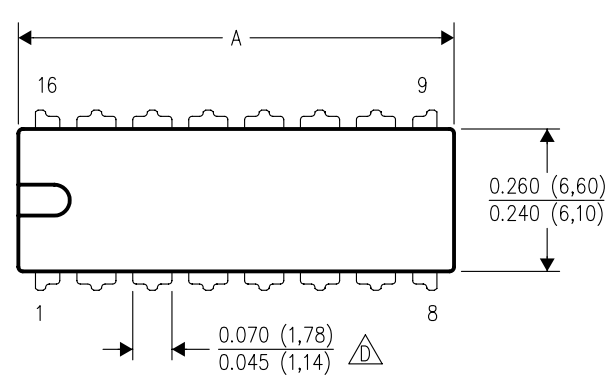
DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

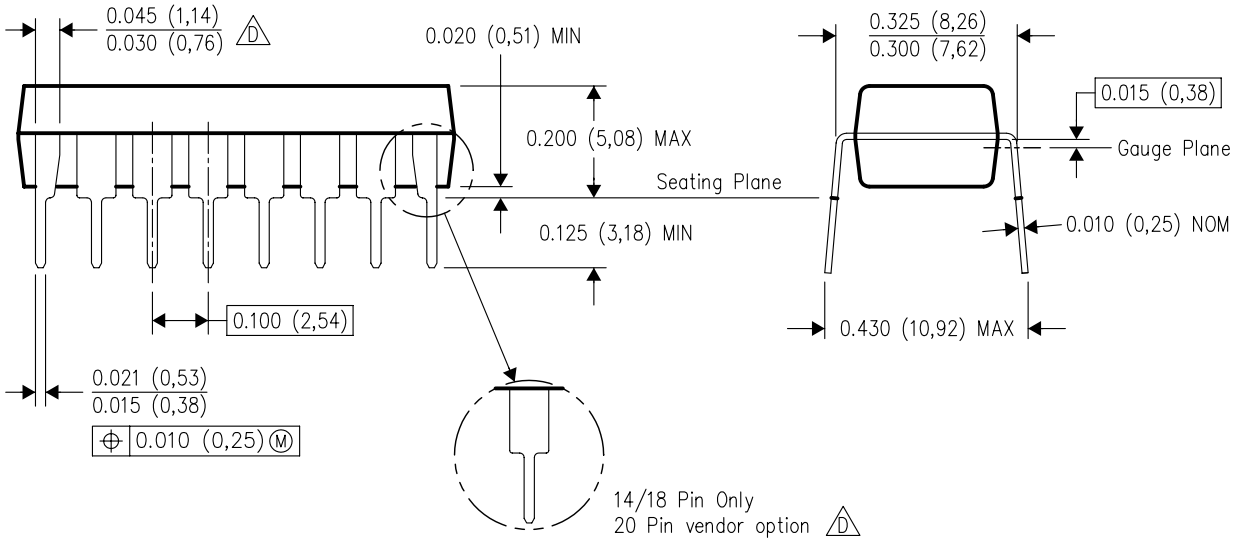
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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