M62023L, P, FP

System Reset IC with Switch for 3V Memory Back-up

REJ03D0528–0100
Rev.1.00
Mar. 11, 2005

General Description

The M62023L/P/FP is a system reset IC that controls the memory backup function of an SRAM and an embedded RAM of a microcontroller.

The IC outputs reset signals (RES/$\overline{\text{RES}}$) to a microcontroller at power-down and power failure. It also shifts the power supply to RAMs from main to backup, outputs a signal ($\overline{\text{CS}}$) that invokes standby mode, and alters RAMs to backup circuit mode.

Features

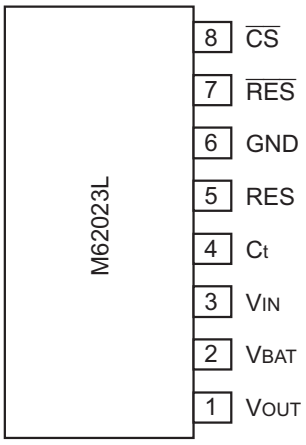
- Built-in switch for selection between main power supply and backup power supply to RAMs
- Small difference between input and output voltages (I_{OUT} = 80mA, V_{IN}=3V): 0.15V typ.
- Detection voltage (power supply monitor voltage): 2.57V typ.
- Chip select signal output ($\overline{\text{CS}}$)
- Two channels of reset outputs (RES/$\overline{\text{RES}}$)
- Power on reset circuit.

Application

Power supply control systems for memory of microcontroller systems in electronic equipment such as OA equipment, industrial equipment, and home-use electronic appliances and SRAM boards with built-in backup function that require switching between external power supply and battery.

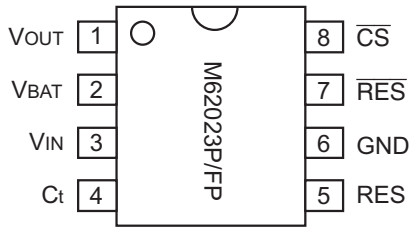
Pin Arrangement

Outline 8P5 (L)



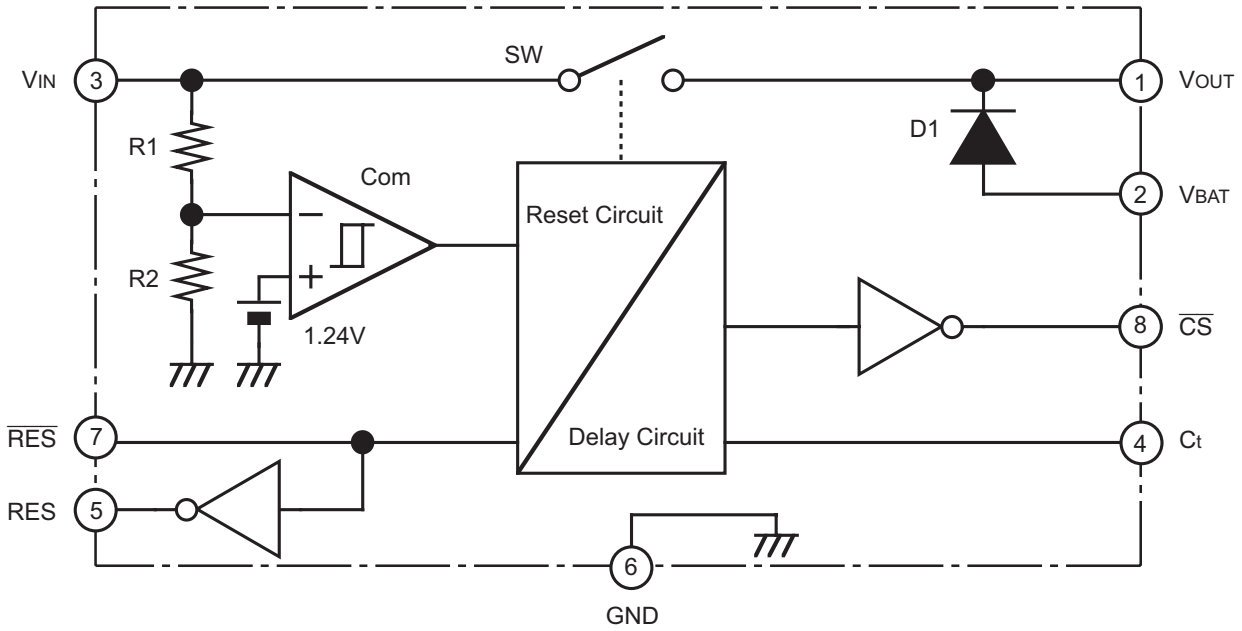
Top view

Outline 8P4 (P)
8P2S-A (FP)



Top view

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Input voltage	V_{IN}	7	V	
Output current	I_{OUT}	100	mA	
Power dissipation	P_d	800 (L) / 625 (P) / 440 (FP)	mW	
Thermal derating	K_θ	8 (L) / 6.25 (P) / 4.4 (FP)	mW/°C	Ta ≥ 25°C
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–40 to +125	°C	

Note: Ta=25°C, unless otherwise noted.

Electrical Characteristics

Item	Sysbol	Min	Typ	Max	Unit	Test Conditions	
Detection voltage	V_S	2.44	2.57	2.70	V	V_{IN} (At change from H→L)	
Hysteresis voltage	ΔV_S	50	100	200	mV	$\Delta V_S = V_{SH} - V_{SL}$	
Circuit current	I_{CC}	—	1.5	3.0	mA	I_{OUT}=0mA	V_{IN}=2V
		—	6.5	10			V_{IN}=3V
Difference between input and output voltage	V_{DROP}	—	0.1	0.2	V	V_{IN}=3V	I_{OUT}=50mA
		—	0.15	0.3			I_{OUT}=80mA
Ct output voltage (high level)	$V_{OH(Ct)}$	2.0	2.4	—	V	V_{IN}=3V*[1]	
Ct output voltage (low level)	$V_{OL(Ct)}$	—	0.02	0.1	V	V_{IN}=2V*[1]	
RES output voltage (high level)	$V_{OH(RES)}$	1.5	2.0	—	V	V_{IN}=2V*[1]	
RES output voltage (low level)	$V_{OL(RES)}$	—	0.02	—	V	V_{IN}=3V*[1]	
		—	0.04	0.2		V_{IN}=3V, Isink=1mA	
$\overline{RES}$ output voltage (high level)	$V_{OH(\overline{RES})}$	2.5	3.0	—	V	V_{IN}=3V*[1]	
$\overline{RES}$ output voltage (low level)	$V_{OL(\overline{RES})}$	—	0.02	—	V	V_{IN}=2V*[1]	
		—	0.04	0.2		V_{IN}=2V, Isink=1mA	
$\overline{CS}$ output voltage (high level)	$V_{OH(\overline{CS})}$	1.3	1.6	—	V	V_{IN}=2V*[2]	
		2.40	2.47	—		V_{IN}=0V, V_{BAT}=3V*[2]	
$\overline{CS}$ output voltage (low level)	$V_{OL(\overline{CS})}$	—	0.07	—	V	V_{IN}=3V*[1]	
		—	0.08	0.3		V_{IN}=3V, Isink=1mA	
Backup Di leak current	I_R	—	—	±0.5	µA	V_{BAT}=3V	V_{IN}=3V
		—	—	±0.5			V_{IN}=0V
Backup Di forward direction voltage	V_F	—	0.54	0.6	V	I_F=10µA	
Delay time	tpd	10	27	55	ms	V_{IN}=0V→3V, Ct=4.7µF	
Response time	td	—	5.0	25.0	µs	V_{IN}=3V→2V	
$\overline{RES}$ limit voltage of operation	$V_{OPL(\overline{RES})}$	—	0.65	—	V	*[3]	

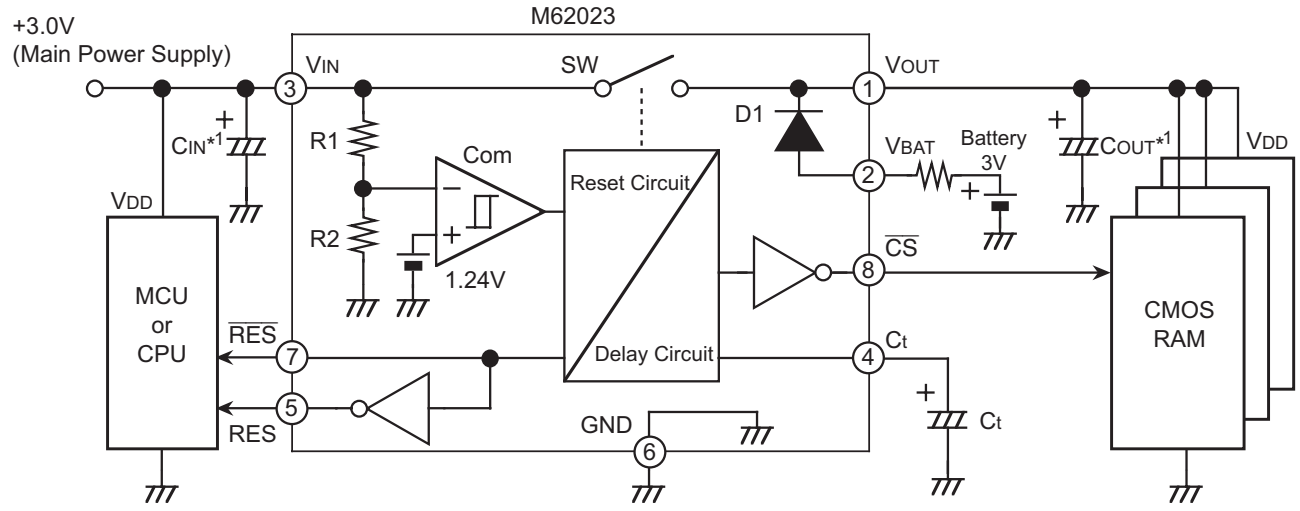
Notes Ta=25°C, unless otherwise noted.

1. Regarding conditions to measure V_{OH} and V_{OL}, voltage values are generated by internal resistance only and no external resistor is used.
2. These values are produced inserting an external resistor, $R_{\overline{CS}}$ = 1MΩ, between the $\overline{CS}$ pin and GND.
3. With no external resistor (10kΩ internal resistance only).

Explanation of Terminals

Pin No.	Symbol	Name	Function
1	V_{OUT}	Power supply output	V_{IN} and V_{BAT} are controlled by means of an internal switch and output through V_{OUT}. The pin is capable of outputting up to 100mA. Use it as V_{DD} of CMOS RAM and the like.
2	V_{BAT}	Backup power supply input	Backup power supply is connected to this pin. If a lithium battery is used, insert a resistor in series for safety purposes.
3	V_{IN}	Power supply input	+3V input pin. Connect to a logic power supply.
4	C_t	Delay capacitor connection pin	A delay capacitor is connected to this pin. By connecting a capacitor, it is possible to delay each output.
5	RES	Positive reset output	Connect to the positive reset input of a microcontroller. The pin is capable of flowing 1mA sink current.
6	GND	Ground	Reference for all signals.
7	$\overline{RES}$	Negative reset output	Connect to the negative reset input of a microcontroller. The pin is capable of flowing 1mA sink current.
8	$\overline{CS}$	Chip select output	Connect to the $\overline{Chip\ Select}$ of RAM. The CS output is at low level in normal state thereby letting RAM be active. Under failure or backup condition, the CS output is set to high level, then RAM enters standby state disabling read/write function. The pin is capable of flowing a 1mA sink current.

Application Example



Note: 1. Capacitance to be connected: C_{IN}: 10μF; C_{OUT}: 4.7μF; C_t: 4.7μF

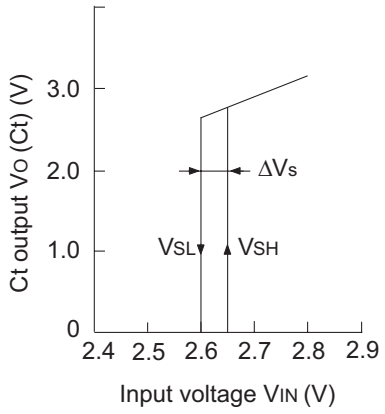
Configuration

<Power supply detector>

The internal reference voltage Vref is compared by means of a comparator with resistor divided voltage VR (resistor-divided voltage produced by R1 and R2 from VIN).

If the input voltage is 3V, VR is set to 1.24V or higher, so the comparator output is at low level and the Ct output (Q1 collector output) is set to high level. If the input voltage drops to below 2.57V in an abnormal condition, VR becomes below 1.24V, so the comparator output goes from low to high level and the Ct output, from high to low. The input voltage at this point is called VSL. Next, when the input voltage, restored from abnormal state, has a rise, the comparator output goes from high to low level and the Ct output, from low to high.

The comparator used for detection has 100mV hysteresis (ΔVs), so that malfunctioning is prevented in case that the input voltage slowly drops or VR nearly equals Vref.



<Delay Circuit>

Connecting an external capacitor to the Ct pin lets RES, $\overline{RES}$, $\overline{CS}$, and VOUT be delayed due to RC transient phenomenon (electric charge).

Delay time is determined as follows.

$$\text{Delay time (tpd)} = Ct \times R3 \times \ln \frac{[V_{OH}(Ct)-V_{OL}(Ct)]}{[V_{OH}(Ct)-INV1(V_{TH})]}$$

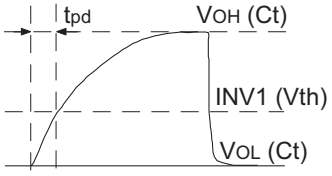
$$= Ct \times 22k\Omega \times 0.2389$$

$$\cong 5.26 \times 10^{3} \times Ct$$

Note: Ct is an external capacitance.

Taking into consideration the time taken by the oscillator of microcomputer to be stable, connect a 4.7µF capacitor to the Ct pin.

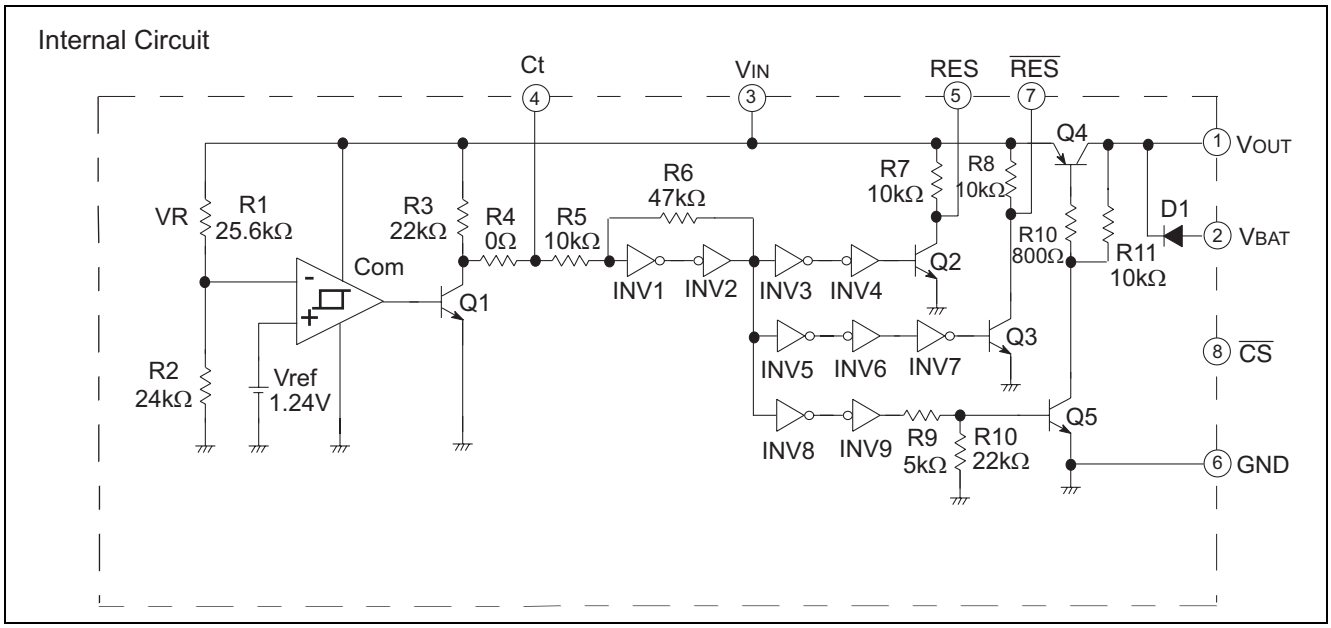
(As the response time of detection can be slowed due to internal structure depending on the rising rate of power supply, avoid connecting a too large capacitance.)



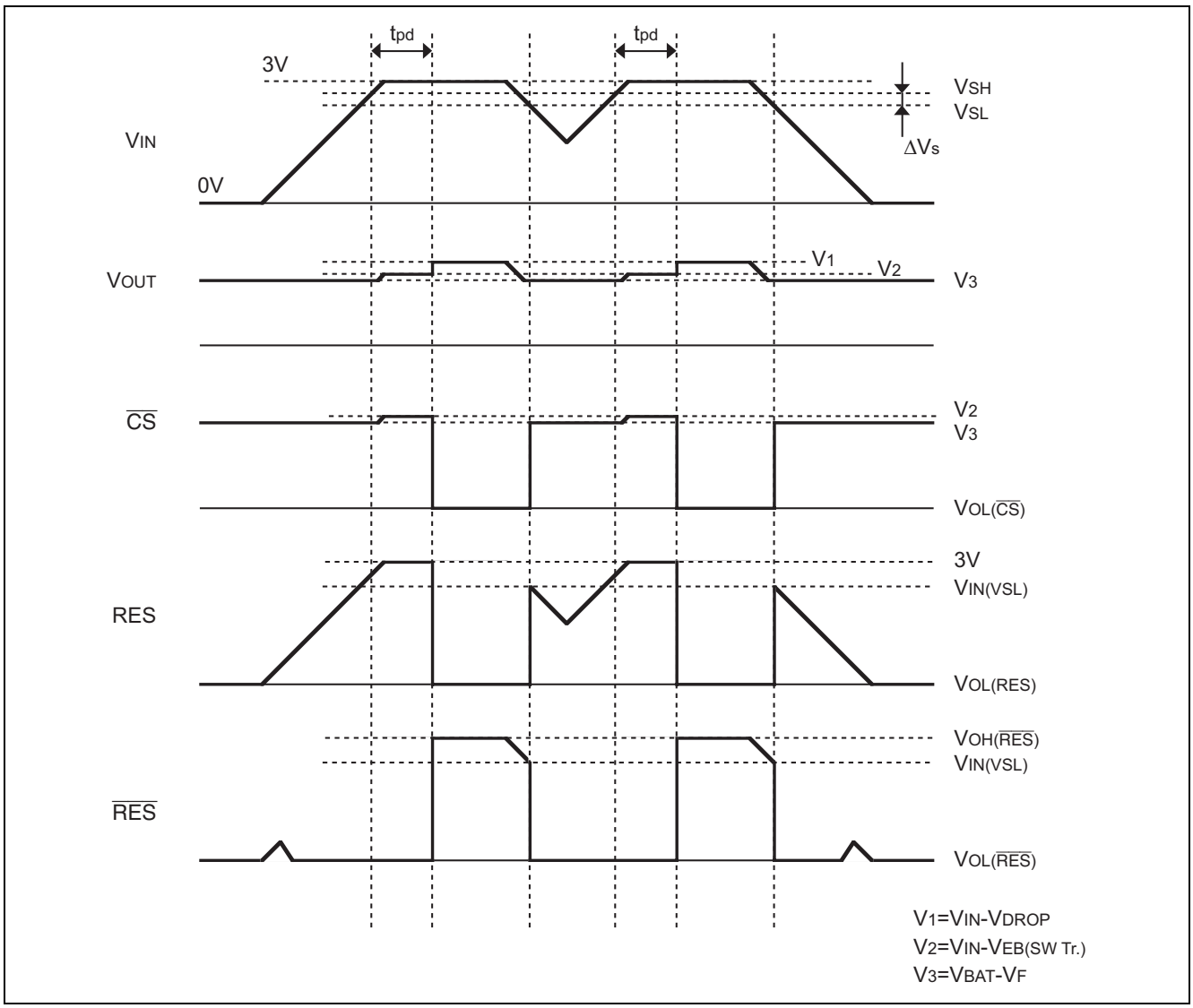
Delayed output waveforms of Ct

<Schmitt trigger circuit>

Since waveforms show a gentle rise due to the RC delay circuit, INV1, INV2, and R6 constitute a Schmitt trigger circuit to produce hysteresis so as to prevent each output from chattering.



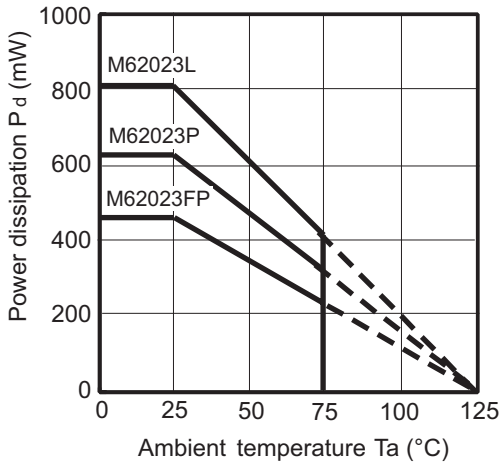
Timing Chart



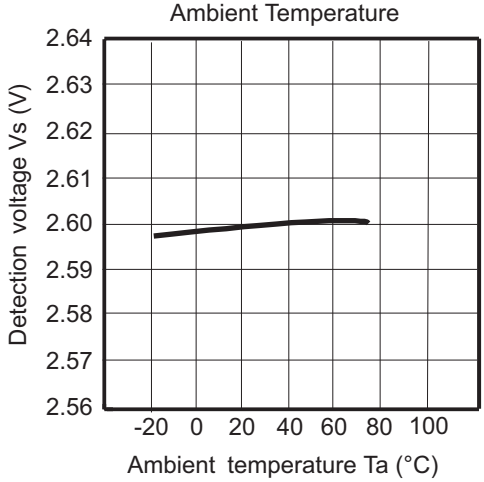
Output pin	Input voltage			
	In normal operation	**In failure (instantaneous drop)**	**Restoration from failure (instantaneous drop)**	**In backup state**
	Input voltage: 3V	Input voltage: 3V→2V Each output varies if the input voltage drops to V_{SL} or under	Input voltage: 2V→3V If the input voltage goes higher than V_{SL} by 100mV, each output varies after delay produced by the delay circuit.	Input voltage: 0V Backup voltage: 3V
V_{OUT}	With SW Tr. set to ON, a voltage (V_{IN}-V_{DROP}) is output.	SW Tr. is turned OFF. A voltage (V_{IN}-V_{EB}) is output by the diode between E and B of SW Tr.	SW Tr. is turned ON after delay and a voltage (V_{IN}-V_{DROP}) is output.	V_{BAT}-V_F
RES	The output level is $V_{OL\ (RES)}$ with a logic low.	As the state shifts from a logic low to logic high, the output level becomes approximately equal to the input voltage.	A logic high is maintained, and then shifts to a logic low.	———
$\overline{RES}$	The output level is $V_{OH(\overline{RES})}$ with a logic high.	As the state shifts from a logic high to logic low, the output level becomes $V_{OL(\overline{RES})}$	A logic low is maintained, and then shifts to a logic high.	———
$\overline{CS}$	The output level is $V_{OL(\overline{CS})}$ with a logic low.	As the state shifts from a logic low to logic high, the output level becomes the voltage V_{IN}-V_{EB}.	A logic high is maintained, and then shifts to a logic low.	The output is a logic high and the output level is V_{BAT}-V_F

Typical Characteristics

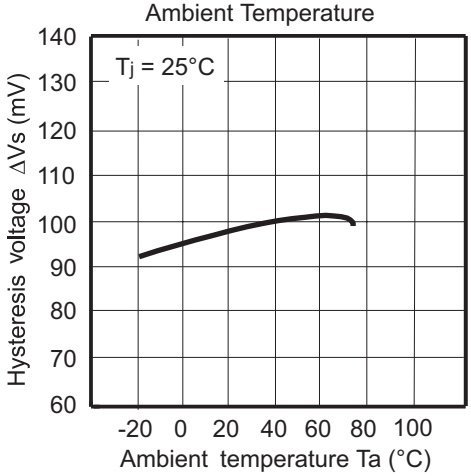
Thermal Derating (Maximum Rating)



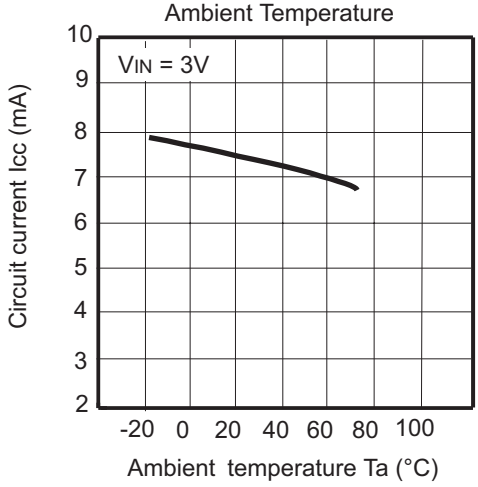
Detection Voltage vs. Ambient Temperature



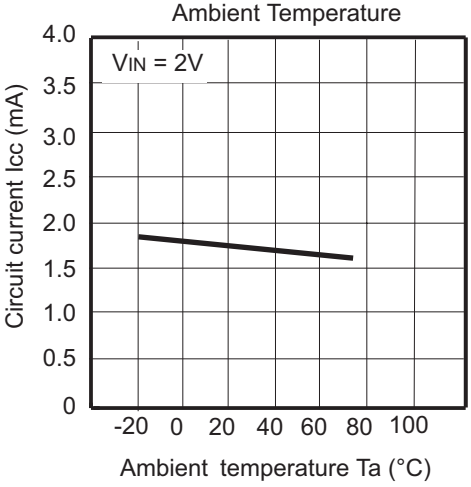
Hysteresis Voltage vs. Ambient Temperature



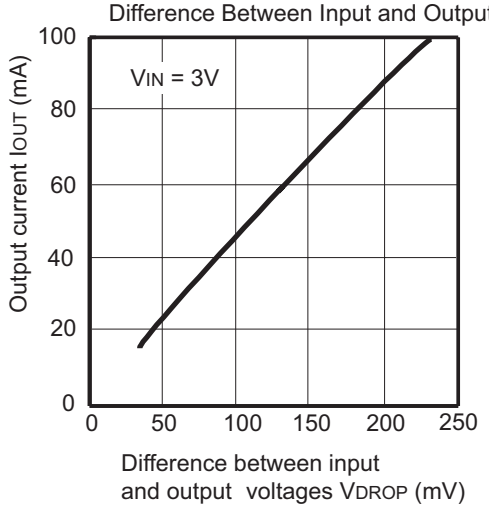
Circuit Current vs. Ambient Temperature



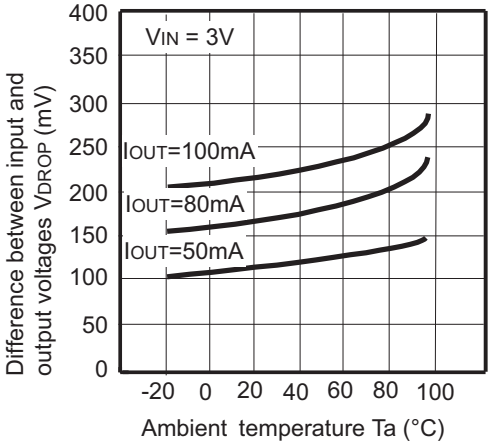
Circuit Current vs. Ambient Temperature



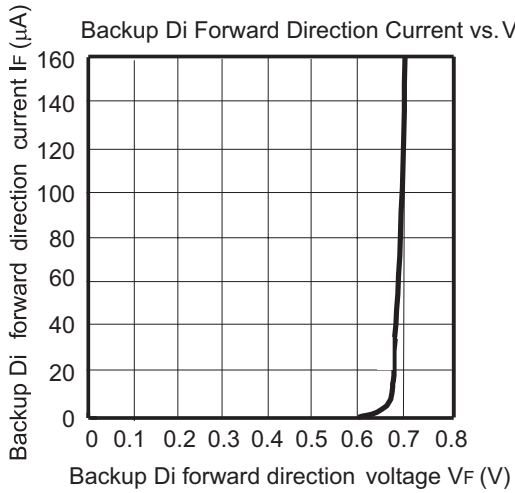
Output Current vs.
Difference Between Input and Output Voltages



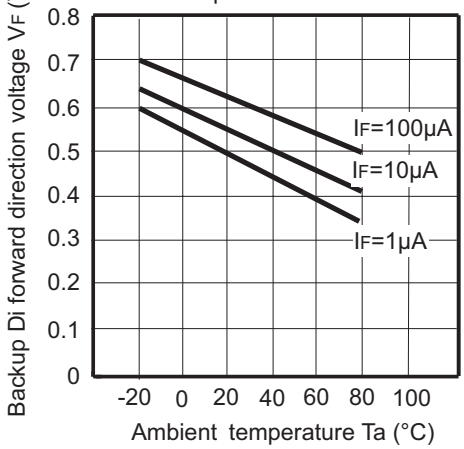
Difference Between Input and Output Voltages vs.
Ambient Temperature



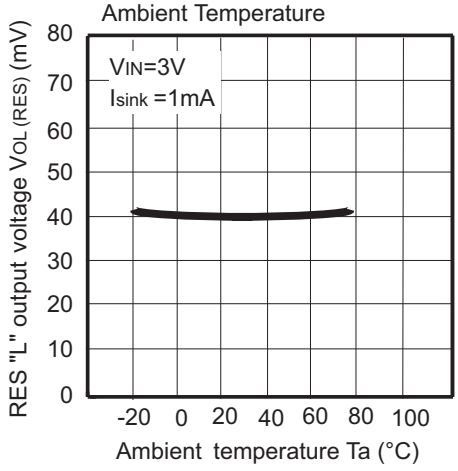
Backup Di Forward Direction Current vs. Voltage



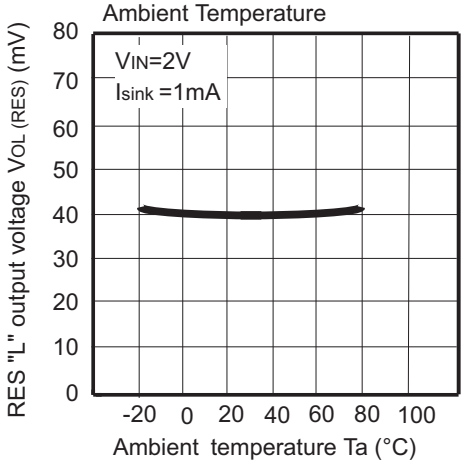
Backup Di Forward Direction Voltage vs.
Ambint Temperature



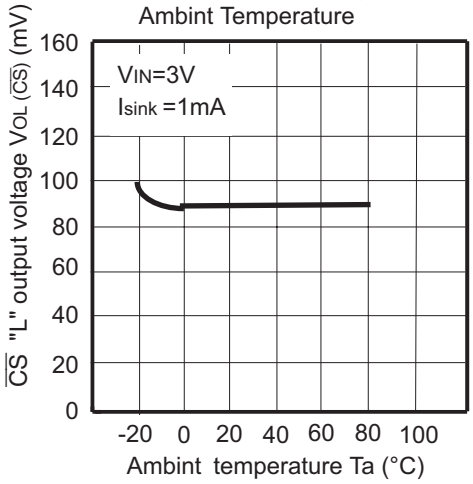
RES "L" Output Voltage vs.
Ambient Temperature



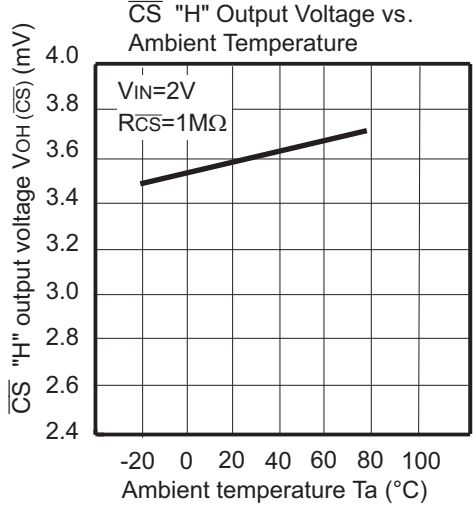
RES "L" Output Voltage vs.
Ambient Temperature



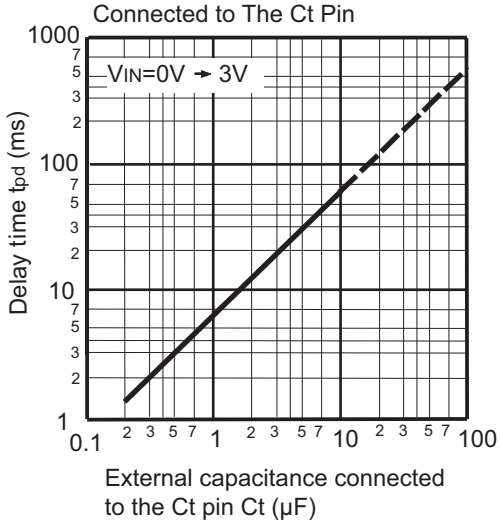
$\overline{CS}$ "L" Output Voltage vs. Ambint Temperature



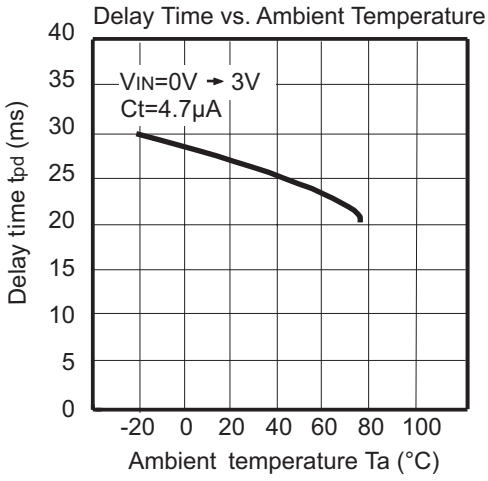
$\overline{CS}$ "H" Output Voltage vs. Ambient Temperature



Delay Time vs. External Capacitance Connected to The Ct Pin

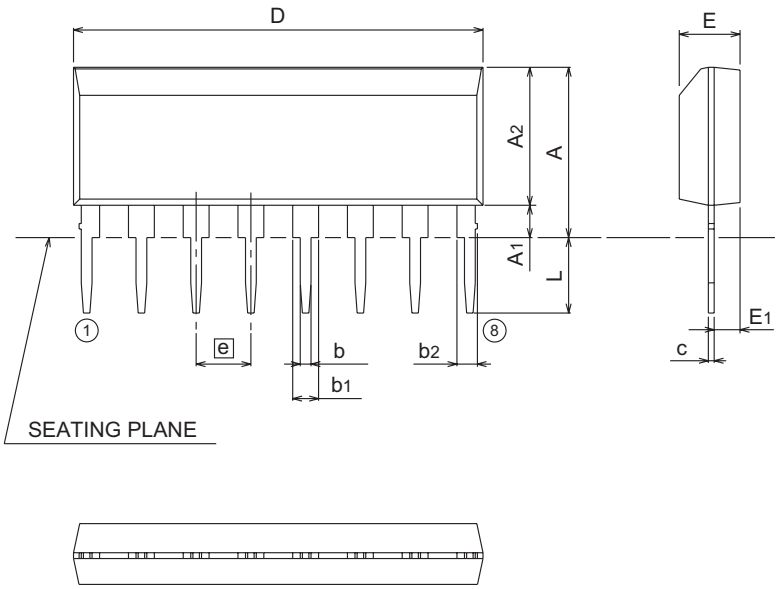


Delay Time vs. Ambient Temperature



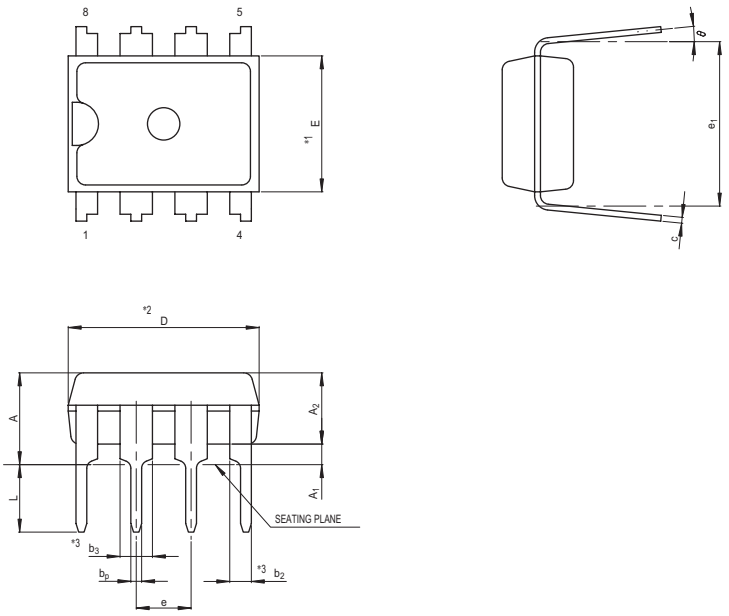
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
SIP8-P-340-2.54	PRSS0008AA-A	8P5	0.73g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	——	——	8.3
A_1	1.2	——	——
A_2	——	6.4	——
b	0.4	0.5	0.6
b_1	1.1	1.2	1.5
b_2	0.75	0.85	1.15
c	0.22	0.27	0.34
D	18.8	19.0	19.2
E	2.6	2.8	3.0
E_1	1.1	1.2	1.3
e	——	2.54	——
L	3.0	——	——

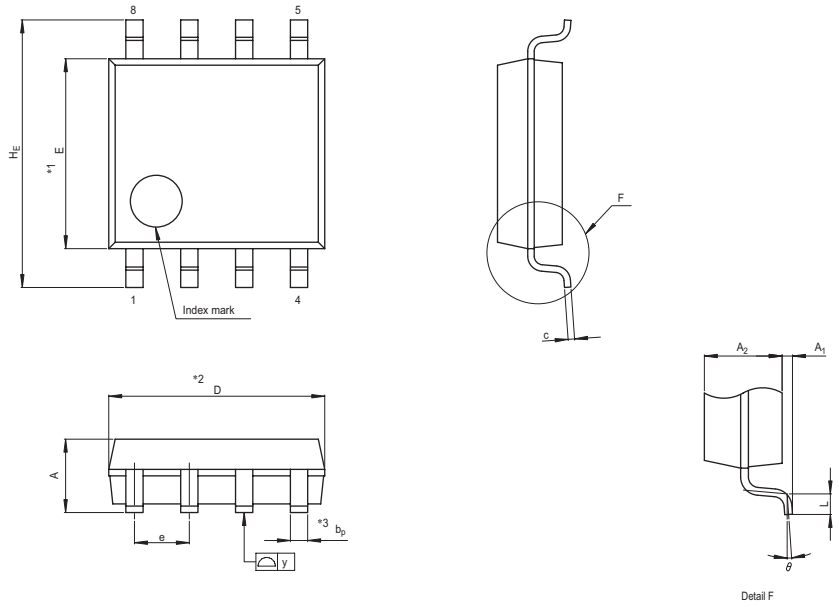
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP8-6.3x8.84-2.54	PRDP0008AA-A	8P4	0.5g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	7.32	7.62	7.92
D	8.7	8.84	9.1
E	6.15	6.3	6.45
A	——	——	4.5
A_1	0.51	——	——
A_2	——	3.3	——
b_p	0.4	0.5	0.6
b_2	0.9	1.0	1.3
b_3	1.4	1.5	1.8
c	0.22	0.27	0.34
θ	0°	——	15°
e	2.29	2.54	2.79
L	3.0	——	——

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP8-4.4x5-1.27	PRSP0008DA-A	8P2S-A	0.07g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.8	5.0	5.2
E	4.2	4.4	4.6
A_2	——	1.5	——
A_1	0.05	——	——
A	——	——	1.9
b_p	0.35	0.4	0.5
c	0.13	0.15	0.2
θ	0°	——	10°
H_E	5.9	6.2	6.5
e	1.12	1.27	1.42
y	——	——	0.1
L	0.2	0.4	0.6

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Colophon .2.0