

RDS FILTER

1 FEATURES

- HIGH PERFORMANCE, STABLE 57KHz FILTER
- HIGH SELECTIVITY
- FLAT GROUP DELAY
- HIGH PERFORMANCE LIMITER
- VERY FEW EXTERNAL COMPONENTS
- 4.332MHz CLOCK OSCILLATOR (8.664MHz OPTIONAL)

2 DESCRIPTION

The TDA7332 is an RDS filter, realized in switched capacitor technique.

The 4 biquad stage architecture is working with 4.332MHz clock.

Figure 1. Package

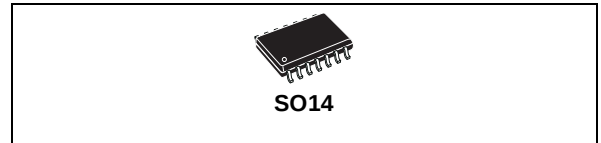


Table 1. Order Codes

Part Number	Package
TDA7332D	SO14
TDA7332D013TR	Tape & Reel
TDA7332DIE1	Chip on wafer

Optionally a 8.664MHz xtal can be used.

The filter has a center frequency of 57KHz and a bandwidth of 3KHz. Input 2nd order antialiasing filter and output smoothing filter are provided.

Block Diagram

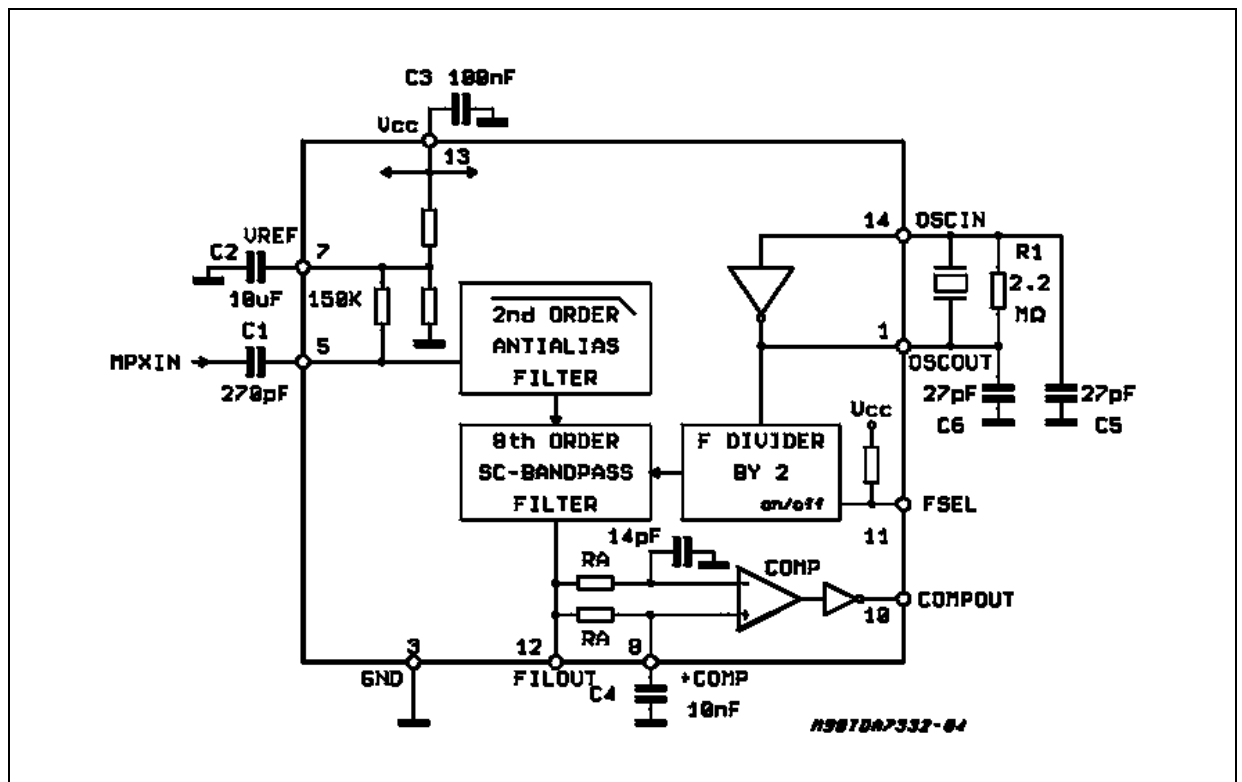


Figure 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V _S	Supply Voltage	7	V
T _{op}	Operating Temperature Range	-40 to 85	°C
T _{stg}	Storage Temperature	-40 to 150	°C

Table 2. Thermal Data

Symbol	Parameter	Value	Unit
R _{th j-case}	Thermal Resistance Junction-case	200	°C

Figure 3. Pin Connection (Top view)

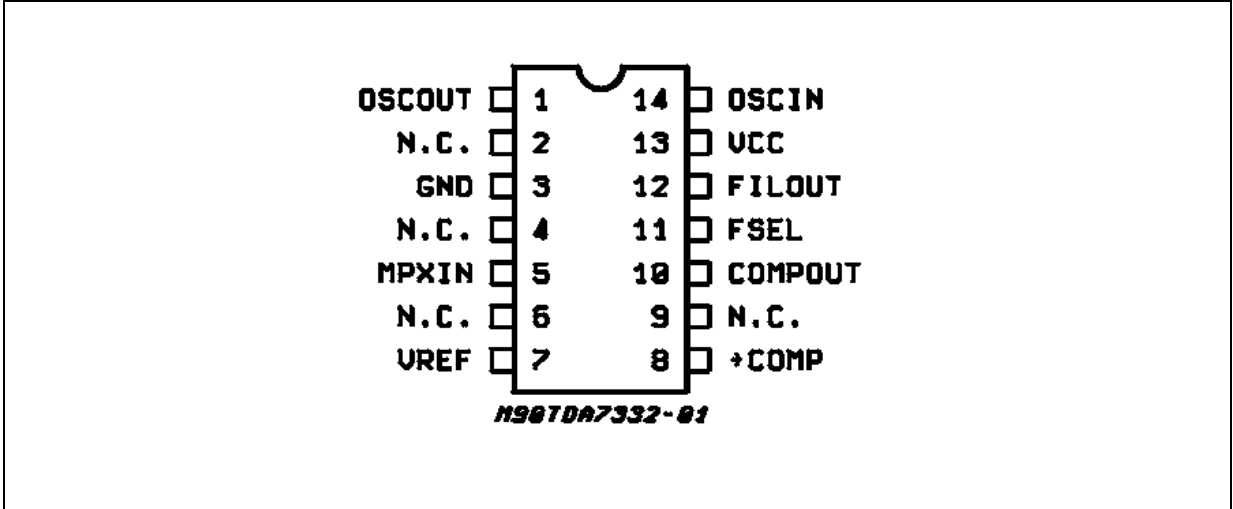


Figure 4. Bonding Pad Locations (Top view)

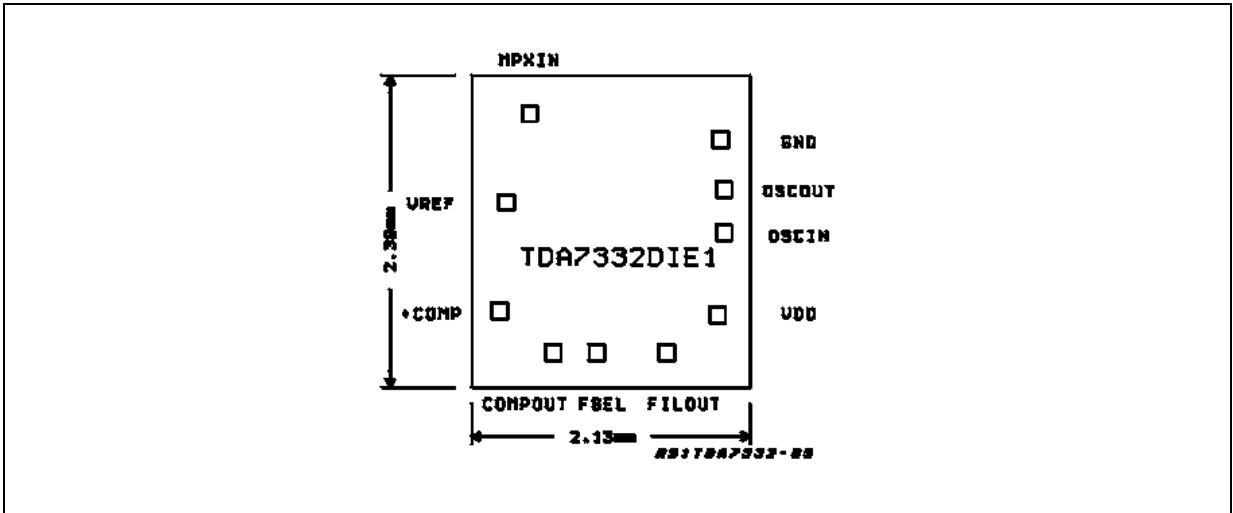


Table 3. Electrical Characteristics (V_{CC} = 5V, T_{amb} = 25°C; f_{osc} = 4.332MHz; V_{IN} = 20mV_{rms} unless

otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY SECTION						
V_{CC}	Supply Voltage		4.5	5	5.5	V
I_S	Supply Current		6	9	14	mA
FILTER						
F_C	Center Frequency		56.5	57	57.5	KHz
BW	3dB Bandwidth		2.5	3	3.5	KHz
G	Gain	$f = 57\text{KHz}$	18	20	22	dB
A	Attenuation	$\Delta f = \pm 4\text{KHz}$	18	22		dB
		$f = 38\text{KHz}; V_i = 500\text{mVrms}$	50	80		dB
		$f = 67\text{KHz}; V_i = 250\text{mVrms}$	35	50		dB
ΔPh	Phase non linearity	A (see note1)		0.5	5	DEG
		B (see note1)		1	7.5	DEG
		C (see note1)		2	10	DEG
R_i	Input Impedance		100	160	200	K Ω
S/N	Signal to Noise Ratio	$V_i = 3\text{mVrms}$	30	40		dB
V_i	Input Signal	$f = 19\text{KHz}; T_3 < -40\text{dB}$ (see note2)			1	Vrms
		$f = 57\text{KHz}$ (RDS + ARI)			50	mVrms
R_L	Load Impedance	Pin 12	100			K Ω
LIMITER						
RA	Resistance pin 8-12		15	21	28	K Ω
V_{OL}	Comp. Output LOW	$I_O = +0.5\text{mA}$			1	V
V_{OH}	Comp. Output HIGH	$I_O = -0.5\text{mA}$	4			V
	Duty Cycle	$V_i = 1\text{mVrms}$		50		%
OSCILLATOR						
F_{OSC}	Oscillator Frequency	$F_{SEL} = \text{Open}$		4.332		MHz
		$F_{SEL} = \text{Closed to Ground}$		8.664		MHz
	Output Amplitude			4.5		V_{PP}
V_{CLL}	Clock Input Level LOW				1	V
V_{OLH}	Clock Input Level HIGH		4			V

CRYSTAL TYPE = EURO QUARTZ

Note (1):

The phase non linearity is defined as: $DPh = |-2ff2 + ff1 + ff3|$ where ffx is the input-output phase difference at the frequency fx ($x = 1,2,3$)

Table 4.

Measure	f1 (KHz)	f2 (KHz)	f3 (KHz)	$\Delta\text{Ph max}$
A	56.5	57	57.5	$<5^\circ$
B	56	57	58	$<7.5^\circ$
C	55.5	57	58.5	$<10^\circ$

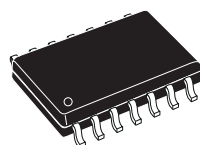
Note (2): The 3th harmonic (57KHz) at the output (pin12) must be less than -40dB in respect to the input signal plus gain.

Figure 5. SO14 Mechanical Data & Package Dimensions

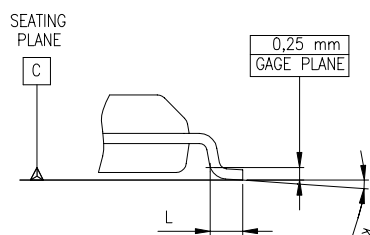
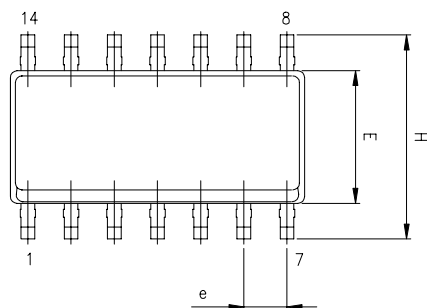
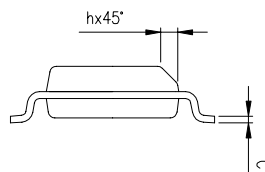
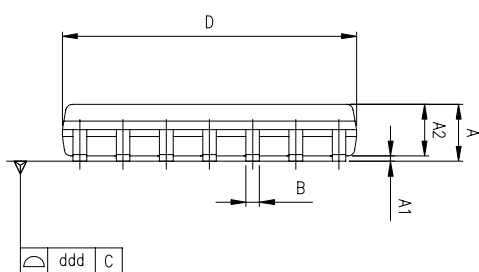
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.30	0.004		0.012
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.01
D (1)	8.55		8.75	0.337		0.344
E	3.80		4.0	0.150		0.157
e		1.27			0.050	
H	5.8		6.20	0.228		0.244
h	0.25		0.50	0.01		0.02
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA



SO14



0016019 D

Table 5. Revision History

Date	Revision	Description of Changes
September 2003	1	First Issue
September 2004	2	Deleted DIP 14 package and part number TDA7332. Aligned the graphic style to be compliant with the new "Corporate Technical Publications Design Guide"

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