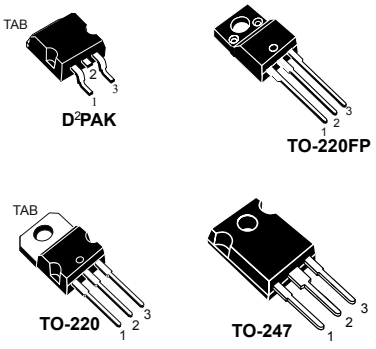
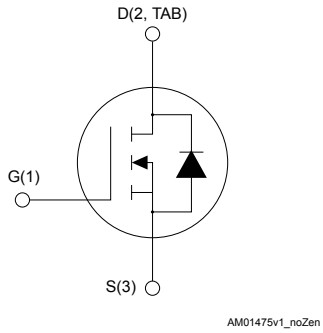
STB31N65M5, STF31N65M5
STP31N65M5, STW31N65M5

Datasheet

N-channel 650 V, 124 mΩ typ., 22 A, MDmesh M5 Power MOSFETs in D²PAK, TO-220FP, TO-220 and TO-247 packages





Features

Order code	V_{DS} @ T_{JMAX}	$R_{DS(on)}$ max.	I_D	Package
STB31N65M5	710 V	148 mΩ	22 A	D²PAK
STF31N65M5				TO-220FP
STP31N65M5				TO-220
STW31N65M5				TO-247

- 100% avalanche tested
- Excellent switching performance
- Extremely low $R_{DS(on)}$
- Low gate charge and input capacitance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

STPOWER

Product status link
STB31N65M5
STF31N65M5
STP31N65M5
STW31N65M5

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D²PAK, TO-220, TO-247	TO-220FP	
V_{GS}	Gate-source voltage	±25		V
I_D	Drain current (continuous) at T_C = 25 °C	22	22 (1)	A
I_D	Drain current (continuous) at T_C = 100 °C	13.9	13.9 (1)	A
I_{DM} (2)	Drain current (pulsed)	88	88 (1)	A
P_{TOT}	Total power dissipation at T_C = 25 °C	150	30	W
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat-sink (t = 1 s, T_C = 25 °C)		2.5	kV
dv/dt (3)	Peak diode recovery voltage slope	15		V/ns
dv/dt (4)	MOSFET dv/dt ruggedness	50		
T_J	Operating junction temperature range	-55 to 150		°C
T_{stg}	Storage temperature range			

1. *Limited by package.*
2. *Limited by maximum junction temperature.*
3. *I_{SD} ≤ 22 A, di/dt ≤ 400 A/µs; V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 400 V.*
4. *V_{DS} ≤ 480 V.*

Table 2. Thermal data

Symbol	Parameter	Value				Unit
		D²PAK	TO-220	TO-220FP	TO-247	
R_{thJC}	Thermal resistance, junction-to-case	0.83		4.17	0.83	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	30(1)	62.5		50	°C/W

1. *When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	5	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	410	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C (1)			100	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 11 A		124	148	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	1865	-	pF
C_{oss}	Output capacitance		-	45	-	pF
C_{rss}	Reverse transfer capacitance		-	4.2	-	pF
$C_{o(tr)}$ (1)	Equivalent capacitance time related	V_{GS} = 0 V, V_{DS} = 0 to 520 V	-	146	-	pF
$C_{o(er)}$ (2)	Equivalent capacitance energy related		-	43	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz, I_B = 0 A	-	2.8	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 11 A V_{GS}= 0 to 10 V (see Figure 17. Test circuit for gate charge behavior)	-	45	-	nC
Q_{gs}	Gate-source charge		-	11.5	-	nC
Q_{gd}	Gate-drain charge		-	20	-	nC

1. *$C_{o(tr)}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*
2. *$C_{o(er)}$ is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	V_{DD}= 400 V, I_D = 14 A, R_G = 4.7 Ω V_{GS} = 10 V (see Figure 18. Test circuit for inductive load switching and diode recovery times and Figure 21. Switching time waveform)	-	46	-	ns
$t_{r(v)}$	Voltage rise time		-	8	-	ns
$t_{f(i)}$	Current fall time		-	8.5	-	ns
$t_{c(off)}$	Crossing time		-	11	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		22	A
I_{SDM} (1)	Source-drain current (pulsed)		-		88	A
V_{SD} (2)	Forward on voltage	I_{SD} = 22 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 22 A, di/dt = 100 A/µs, V_{DD} = 100 V (see Figure 18. Test circuit for inductive load switching and diode recovery times)	-	336		ns
Q_{rr}	Reverse recovery charge		-	5		µC
I_{RRM}	Reverse recovery current		-	30		A
t_{rr}	Reverse recovery time	I_{SD} = 22 A, di/dt = 100 A/µs, V_{DD}= 100 V, T_j= 150 °C (see Figure 18. Test circuit for inductive load switching and diode recovery times)	-	406		ns
Q_{rr}	Reverse recovery charge		-	6		µC
I_{RRM}	Reverse recovery current		-	31		A

1. *Pulse width limited by safe operating area*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for D²PAK, TO-220 and TO-247

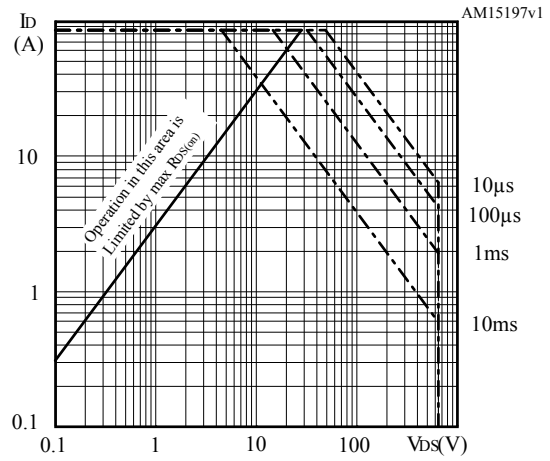


Figure 2. Thermal impedance for D²PAK, TO-220 and TO-247

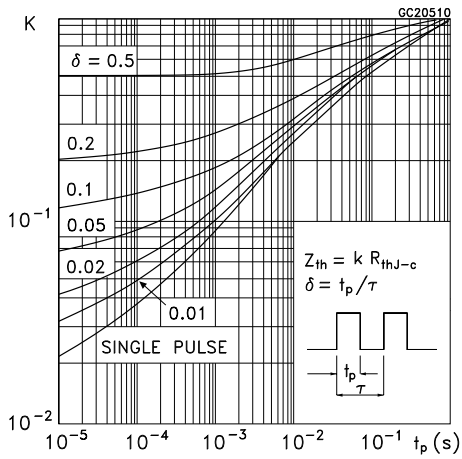


Figure 3. Safe operating area for TO-220FP

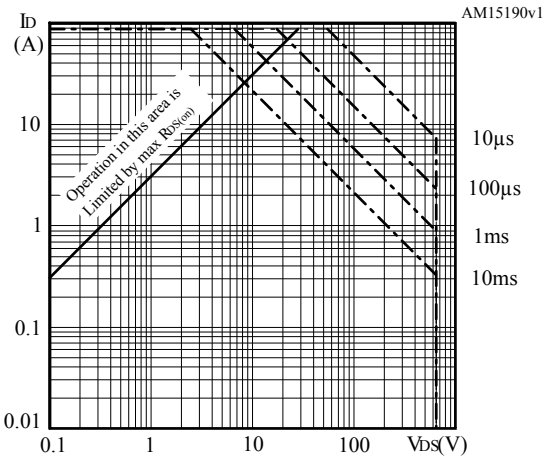


Figure 4. Thermal impedance for TO-220FP

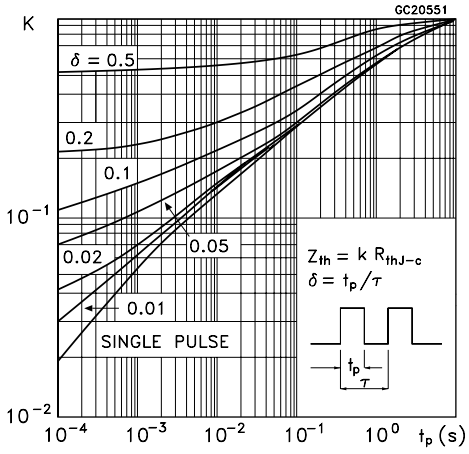


Figure 5. Output characteristics

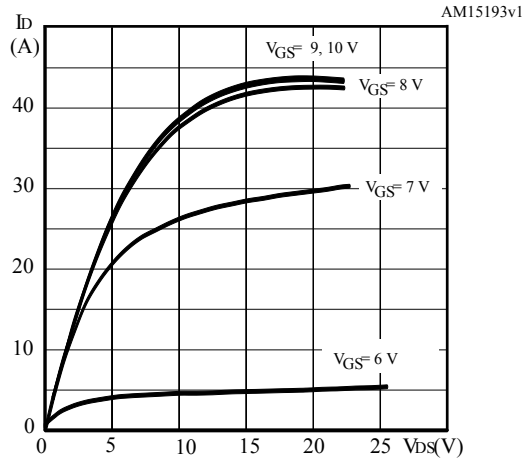


Figure 6. Transfer characteristics

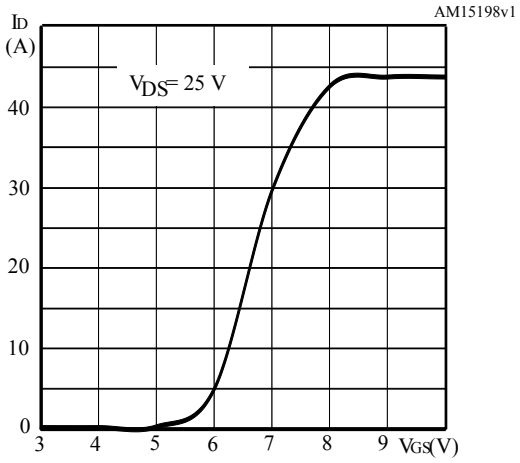


Figure 7. Gate charge vs gate-source voltage

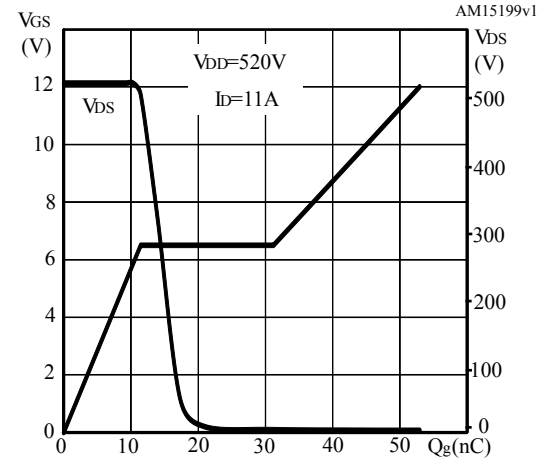


Figure 8. Static drain-source on-resistance

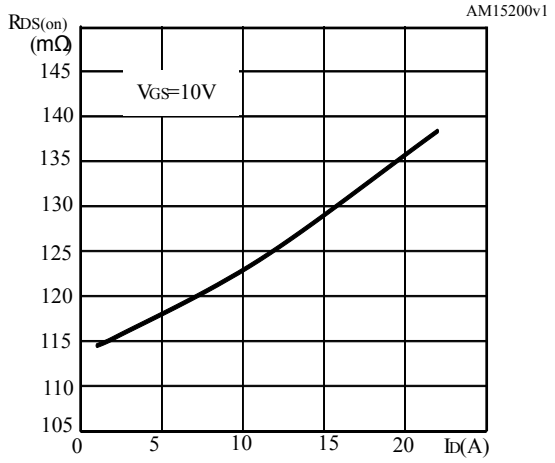


Figure 9. Capacitance variations

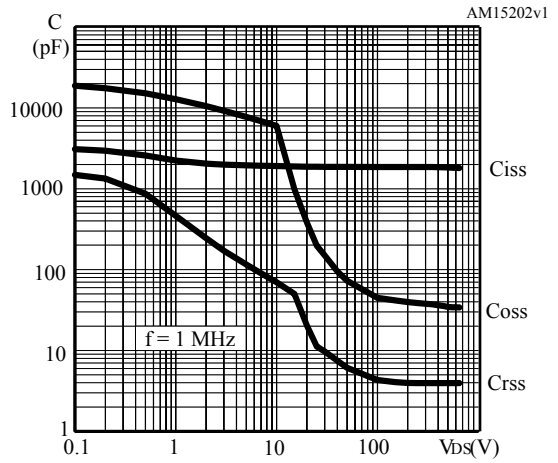


Figure 10. Output capacitance stored energy

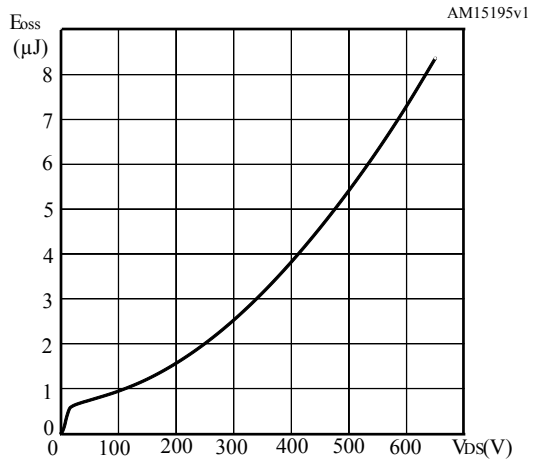


Figure 11. Normalized gate threshold voltage vs temperature

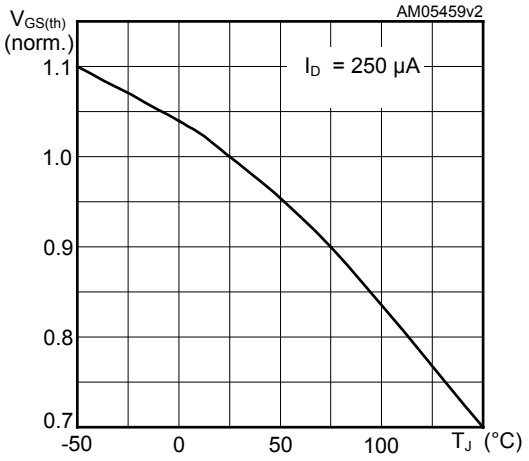


Figure 12. Normalized on-resistance vs temperature

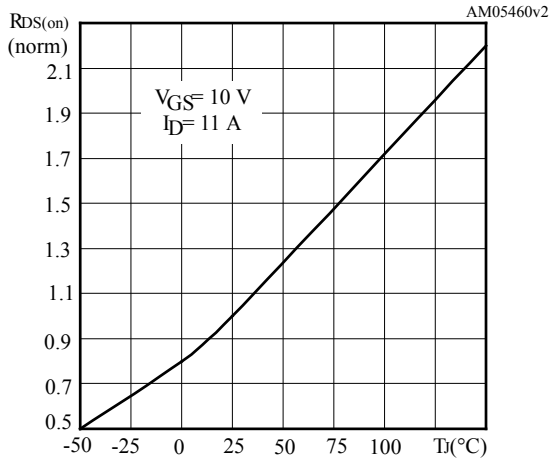


Figure 13. Source-drain diode forward characteristics

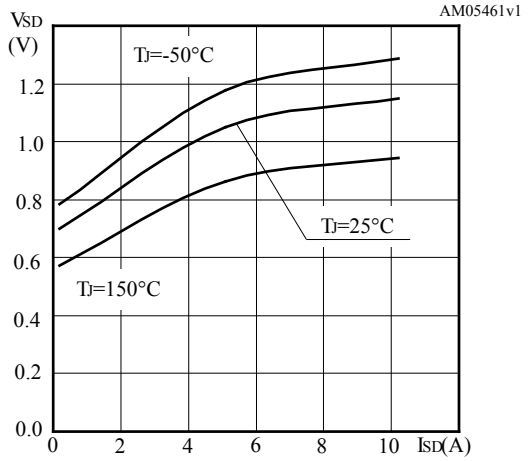


Figure 14. Normalized $V_{(BR)DSS}$ vs temperature

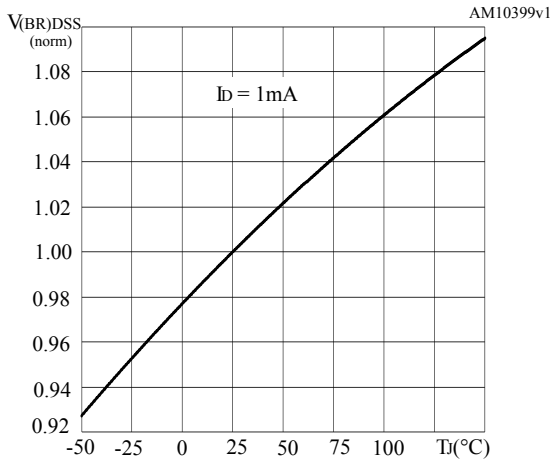
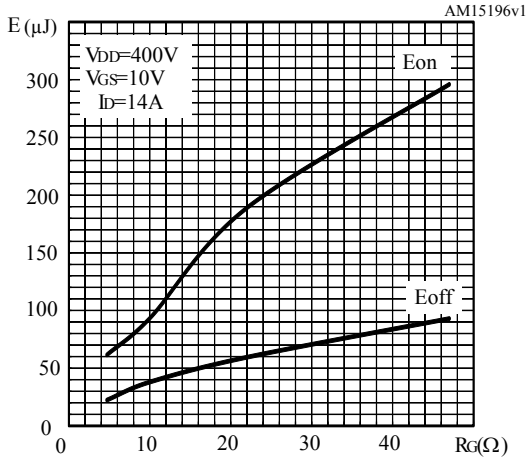


Figure 15. Switching energy vs gate resistance



Note: E_{on} including reverse recovery of a SiC diode.

3 Test circuits

Figure 16. Test circuit for resistive load switching times

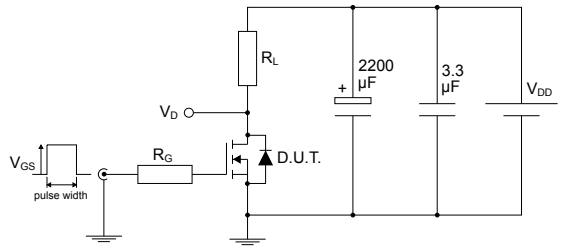


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Figure 17. Test circuit for gate charge behavior

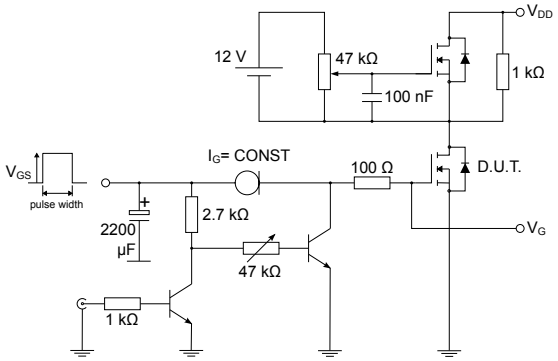

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Figure 18. Test circuit for inductive load switching and diode recovery times

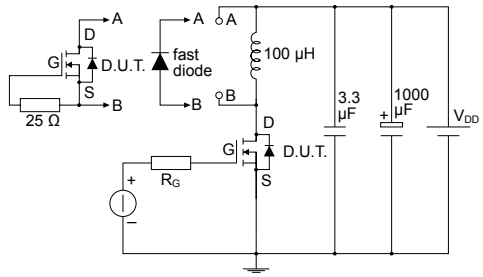

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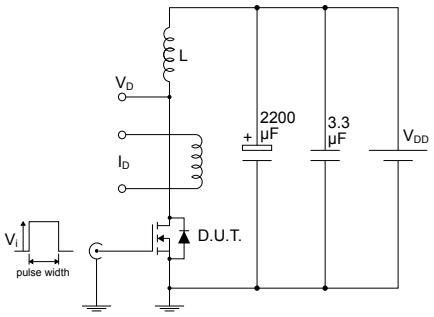
Figure 19. Unclamped inductive load test circuit



AM01471v1

Figure 20. Unclamped inductive waveform

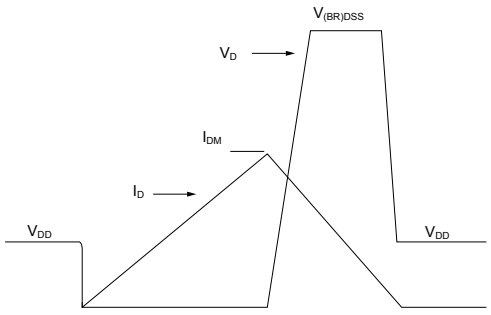


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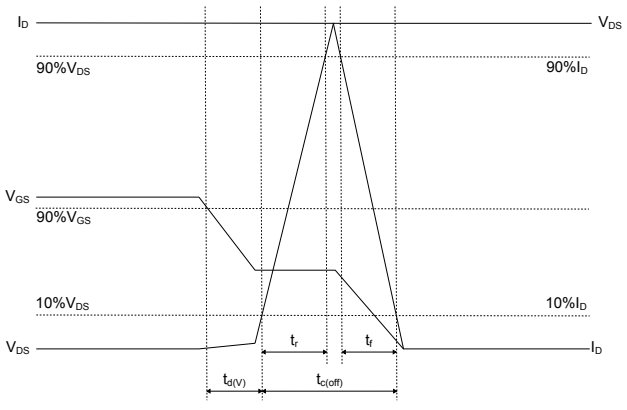
Figure 21. Switching time waveform



AM05540v2

4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 22. **D²PAK (TO-263) type A package outline**

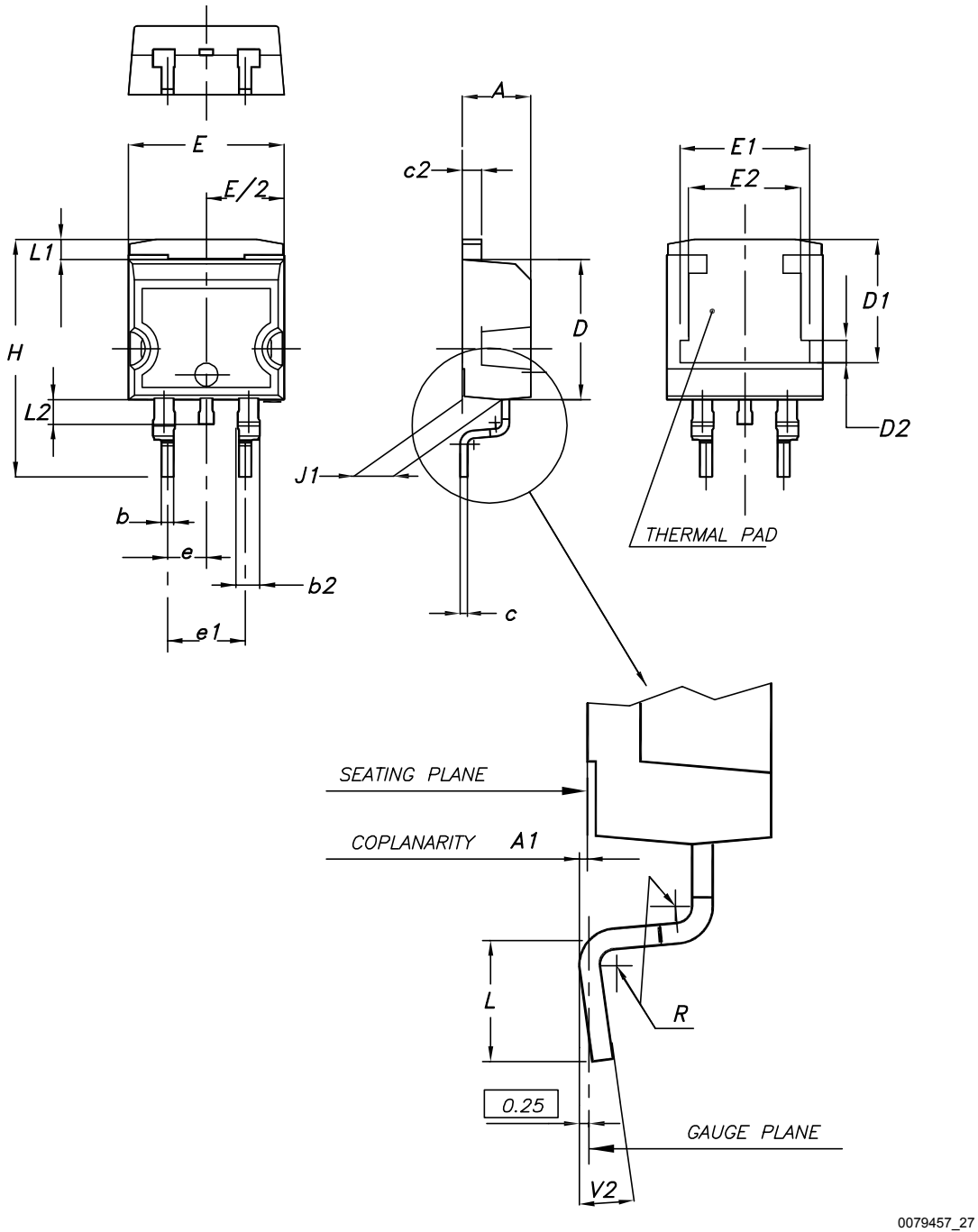


Table 8. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

4.2 D²PAK (TO-263) type B package information

Figure 23. **D²PAK (TO-263) type B package outline**

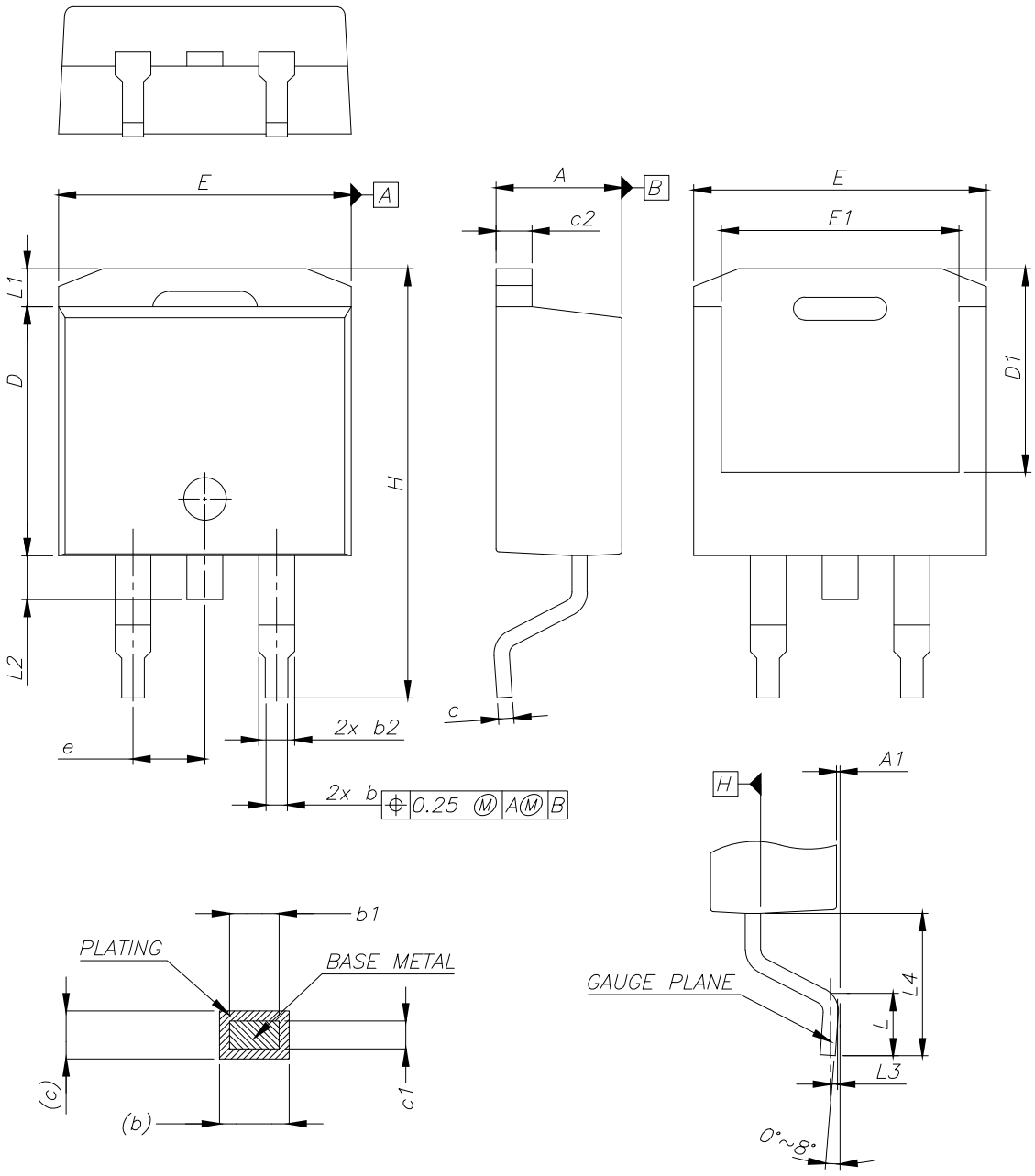


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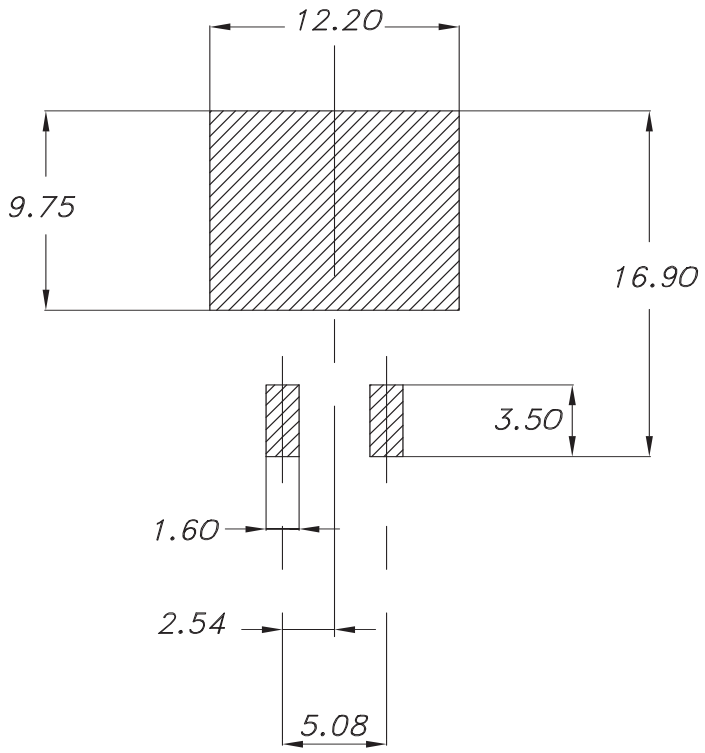
Table 9. **D²PAK (TO-263) type B mechanical data**

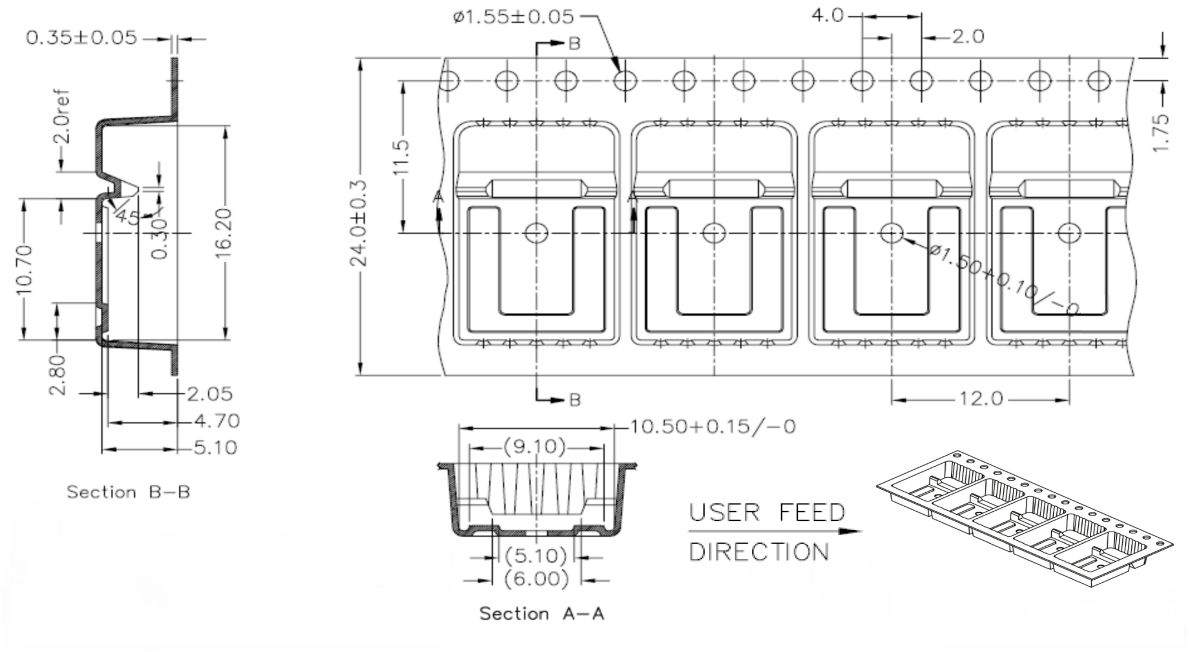
Dim.	mm		
	Min.	Typ.	Max.
A	4.36		4.56
A1	0.00		0.25
b	0.70		0.90
b1	0.51		0.89
b2	1.17		1.37
c	0.38		0.694
c1	0.38		0.534
c2	1.19		1.34
D	8.60		9.00
D1	6.90		7.50
E	10.15		10.55
E1	8.10		8.70
e	2.54 BSC		
H	15.00		15.60
L	1.90		2.50
L1			1.65
L2			1.78
L3		0.25	
L4	4.78		5.28

Figure 24. **D²PAK (TO-263) recommended footprint (dimensions are in mm)**



4.3 D²PAK packing information

Figure 25. **D²PAK tape drawing (dimensions are in mm)**



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4.4 TO-220FP type B package information

Figure 26. **TO-220FP type B package outline**

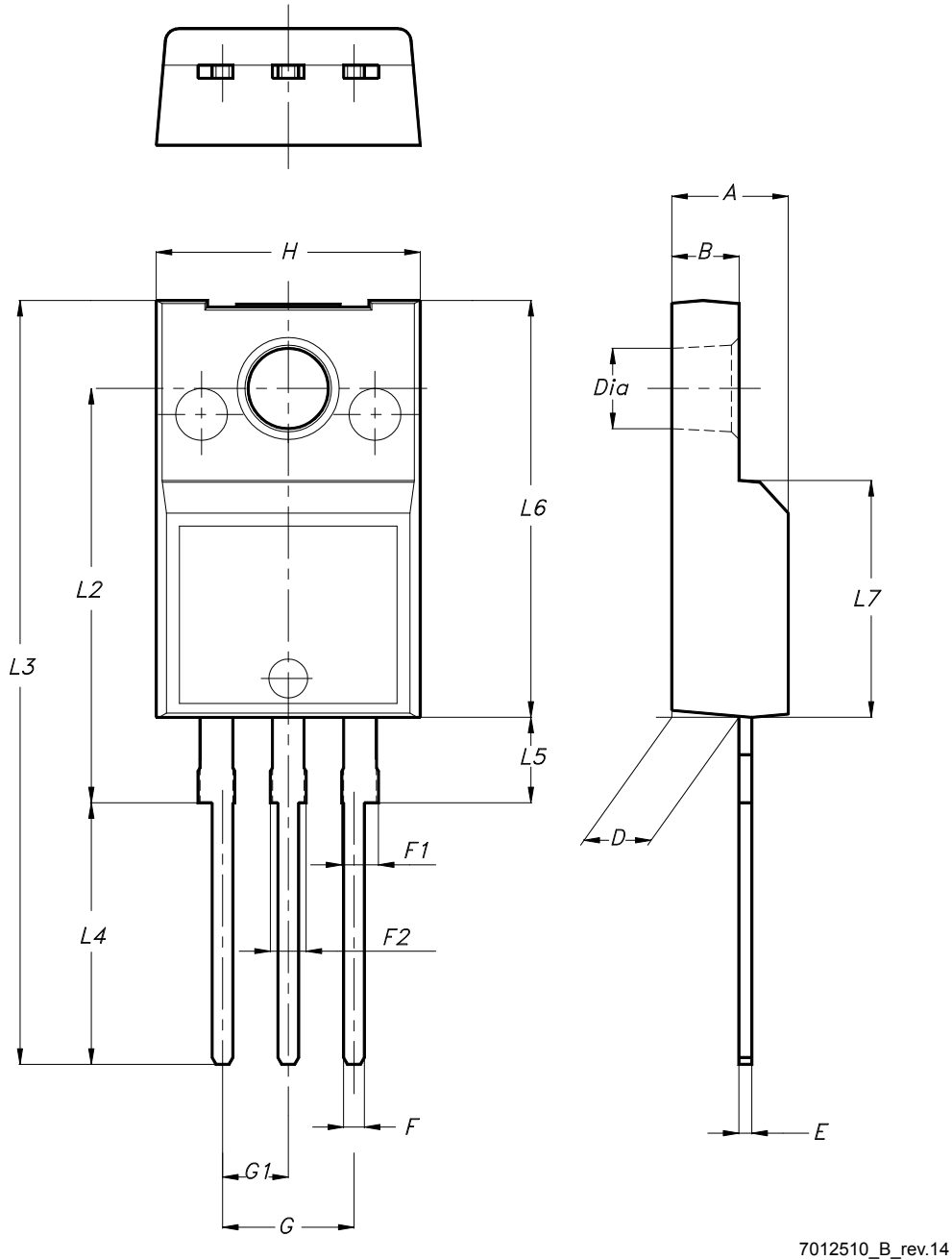

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Table 10. **TO-220FP type B package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

4.5 TO-220 type A package information

Figure 27. **TO-220 type A package outline**

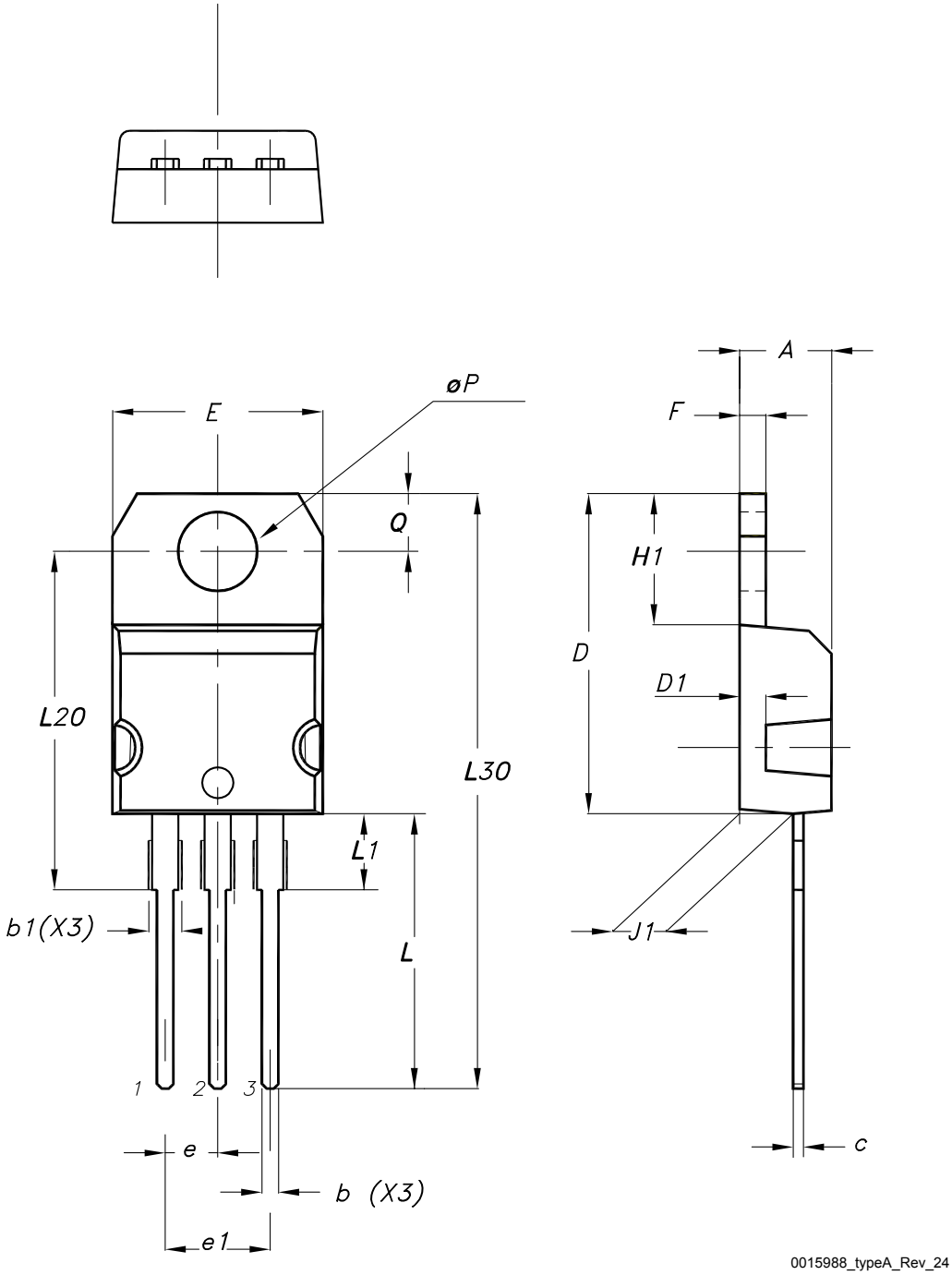
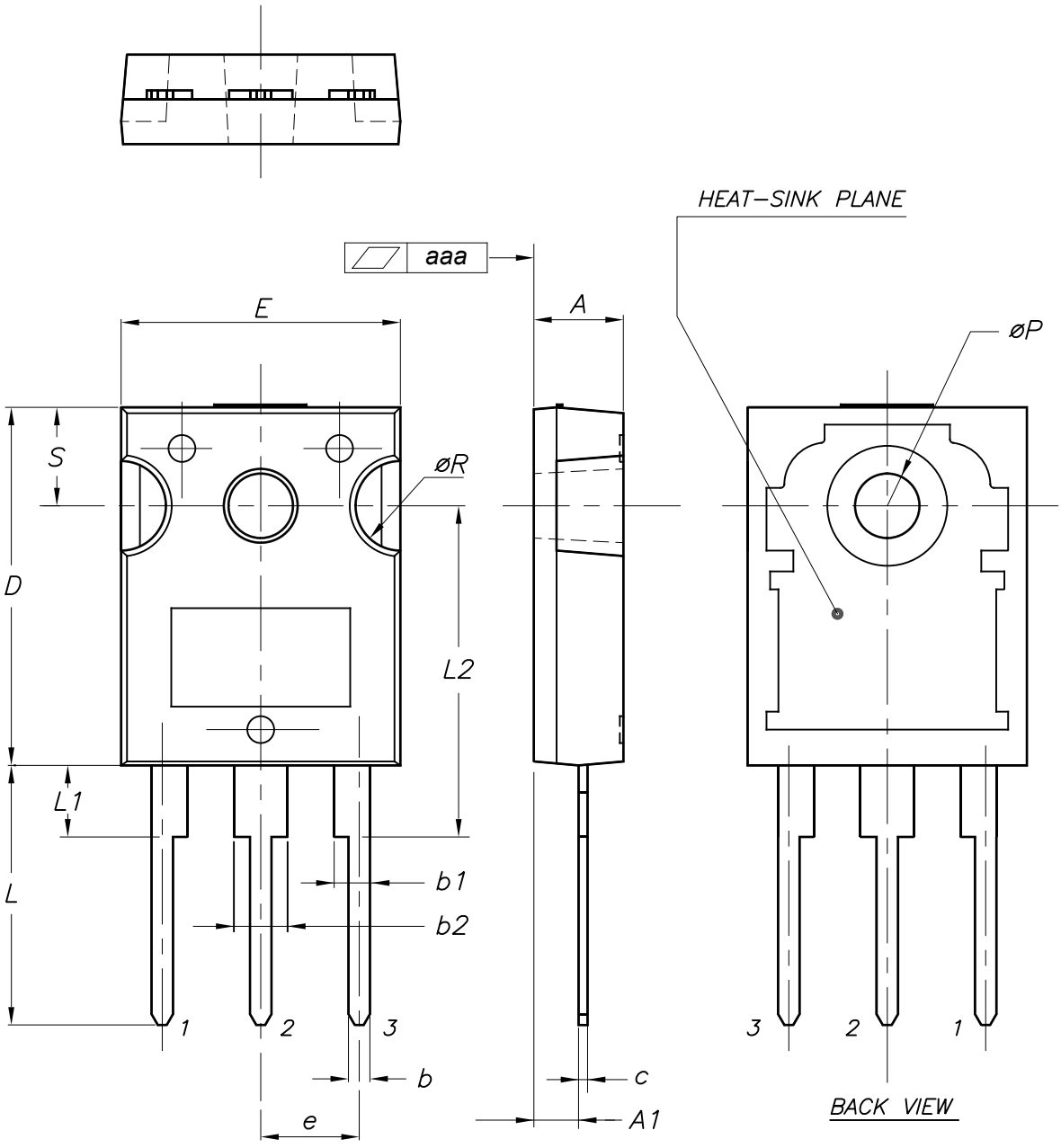


Table 11. **TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

4.6 TO-247 package information

Figure 28. **TO-247 package outline**



0075325_10

Table 12. **TO-247 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70
aaa		0.04	0.10

5 Ordering information

Table 13. **Order codes**

Order code	Marking	Package	Packing
STB31N65M5	31N65M5	D^2PAK	Tape e reel
STF31N65M5		TO-220FP	Tube
STP31N65M5		TO-220	
STW31N65M5		TO-247	

Revision history

Table 14. **Document revision history**

Date	Revision	Changes
23-Feb-2012	1	First release.
10-Sep-2012	2	– Modified *note 2* under the *Table 2*. – Updated typical values in Table 4, 5 and 6. – Added *Section 2.1*. – Minor text changes on the cover page.
05-Mar-2013	3	Added dv/dt value on *Table 2: Absolute maximum ratings*.
15-Apr-2019	4	The part number STFI31N65M5 has been moved to a separate datasheet. Removed maturity status indication from cover page. The document status is production data. Updated features and description in cover page. Updated *Section 4 Package information*. Added *Section 5 Ordering information.* Minor text changes.
21-Aug-2025	5	Updated Section 4: Package information. Minor text changes.

Contents

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