



# SOT23, Low-Power $\mu$ P Supervisory Circuits with Battery Backup and Chip-Enable Gating

## General Description

The MAX6365–MAX6368 supervisory circuits simplify power-supply monitoring, battery-backup control functions, and memory write protection in microprocessor ( $\mu$ P) systems. The circuits significantly improve the size, accuracy, and reliability of modern systems with an ultra-small integrated solution.

These devices perform four basic system functions:

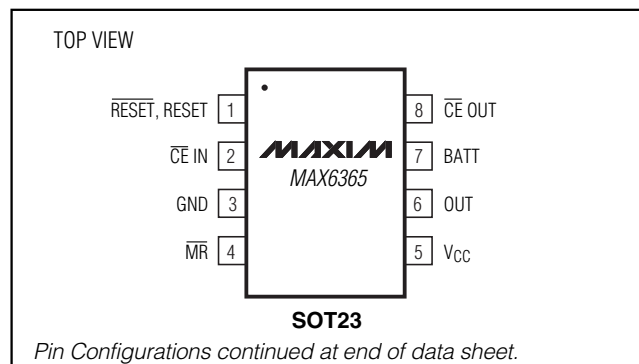
- 1) Provide a  $\mu$ P reset output during  $V_{CC}$  supply power-up, power-down, and brownout conditions.
- 2) Internally control  $V_{CC}$  to backup-battery switching to maintain data or low-power operation for CMOS RAM, CMOS  $\mu$ Ps, real-time clocks, and other digital logic when the main supply fails.
- 3) Provide memory write protection through internal chip-enable gating during supply or processor faults.
- 4) Include one of the following options: a manual reset input (MAX6365), a watchdog timer function (MAX6366), a battery-on output (MAX6367), or an auxiliary user-adjustable reset input (MAX6368).

The MAX6365–MAX6368 operate from  $V_{CC}$  supply voltages as low as 1.2V. The factory preset reset threshold voltages range from 2.32V to 4.63V (see *Ordering Information*). In addition, each part is offered in three reset output versions: push-pull active low, open-drain active low, or open-drain active high (see *Selector Guide*). The MAX6365–MAX6368 are available in miniature 8-pin SOT23 packages.

## Applications

Critical $\mu$ P/ $\mu$ C Power Monitoring	Portable/Battery-Powered Equipment
Fax Machines	Set-Top Boxes
Industrial Control	POS Equipment
Computers/Controllers	

## Pin Configurations



## Features

- ◆ Low +1.2V Operating Supply Voltage ( $V_{CC}$  or  $V_{BATT}$ )
- ◆ Precision Monitoring of +5.0V, +3.3V, +3.0V, and +2.5V Power-Supply Voltages
- ◆ On-Board Gating of Chip-Enable Signals, 1.5ns Propagation Delay
- ◆ Debounced Manual Reset Input (MAX6365)
- ◆ Watchdog Timer, 1.6s Timeout (MAX6366)
- ◆ Battery-On Output Indicator (MAX6367)
- ◆ Auxiliary User-Adjustable RESET IN (MAX6368)
- ◆ Low 10 $\mu$ A Quiescent Supply Current
- ◆ Three Available Output Structures
  - Push-Pull  $\overline{\text{RESET}}$
  - Open-Drain  $\overline{\text{RESET}}$
  - Open-Drain RESET
- ◆ RESET/ $\overline{\text{RESET}}$  Valid Down to 1.2V Guaranteed ( $V_{CC}$  or  $V_{BATT}$ )
- ◆ Power-Supply Transient Immunity
- ◆ 150ms min Reset Timeout Period
- ◆ Miniature 8-Pin SOT23 Package

## Ordering Information

PART*	TEMP. RANGE	PIN-PACKAGE
MAX6365LKA__-T	-40°C to +85°C	8 SOT23-8
MAX6365PKA__-T	-40°C to +85°C	8 SOT23-8
MAX6365HKA__-T	-40°C to +85°C	8 SOT23-8
MAX6366LKA__-T	-40°C to +85°C	8 SOT23-8
MAX6366PKA__-T	-40°C to +85°C	8 SOT23-8
MAX6366HKA__-T	-40°C to +85°C	8 SOT23-8
MAX6367LKA__-T	-40°C to +85°C	8 SOT23-8
MAX6367PKA__-T	-40°C to +85°C	8 SOT23-8
MAX6367HKA__-T	-40°C to +85°C	8 SOT23-8
MAX6368LKA__-T	-40°C to +85°C	8 SOT23-8
MAX6368PKA__-T	-40°C to +85°C	8 SOT23-8
MAX6368HKA__-T	-40°C to +85°C	8 SOT23-8

\*These parts offer a choice of reset threshold voltages. From the Reset Threshold Ranges table, insert the desired threshold voltage code in the blank to complete the part number. SOT parts come in tape-and-reel only and must be ordered in 2500-piece increments. See Device Marking Codes for a complete parts list, including SOT top marks and standard threshold versions. See Selector Guide for a listing of device features.

Typical Operating Circuit appears at end of data sheet.



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## ABSOLUTE MAXIMUM RATINGS

Terminal Voltages (with respect to GND)

$V_{CC}$ , BATT, OUT ..... -0.3V to +6V

RESET (open drain), RESET (open drain) ..... -0.3V to +6V

BATT ON, RESET (push-pull), RESET IN,

WDI,  $\overline{CE}$  IN,  $\overline{CE}$  OUT ..... -0.3V to ( $V_{OUT} + 0.3V$ )

MR ..... -0.3V to ( $V_{CC} + 0.3V$ )

Input Current

$V_{CC}$  Peak ..... 1A

$V_{CC}$  Continuous ..... 250mA

BATT Peak ..... 250mA

BATT Continuous ..... 40mA

GND ..... 75mA

Output Current

OUT ..... Short-Circuit Protected for up to 10s

RESET, RESET, BATT ON,  $\overline{CE}$  OUT ..... 20mA

Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ )

8-Pin SOT23 (derate 8.75mW/ $^\circ\text{C}$  above  $+70^\circ\text{C}$ ) ..... 700mW

Operating Temperature Range .....  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$

Storage Temperature Range .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$

Junction Temperature .....  $+150^\circ\text{C}$

Lead Temperature (soldering, 10s) .....  $+300^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

( $V_{CC} = +2.4V$  to  $+5.5V$ ,  $V_{BATT} = +3.0V$ ,  $\overline{CE}$  IN =  $V_{CC}$ , reset not asserted,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ . Typical values are at  $T_A = +25^\circ\text{C}$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range (Note 2)	$V_{CC}$ , $V_{BATT}$	No load		0		5.5	V
Supply Current (Excluding $I_{OUT}$ )	$I_{CC}$	No load, $V_{CC} > V_{TH}$	$V_{CC} = 2.8V$		10	30	$\mu\text{A}$
			$V_{CC} = 3.6V$		12	35	
			$V_{CC} = 5.5V$		15	50	
Supply Current in Battery-Backup Mode (Excluding $I_{OUT}$ )	$I_{BACK}$	$V_{BATT} = 2.8V$ , $V_{CC} = 0$	$T_A = +25^\circ\text{C}$			1	$\mu\text{A}$
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			3	
BATT Standby Current	$I_{BATT}$	$5.5V > V_{CC} > (V_{BATT} + 0.2V)$	$T_A = +25^\circ\text{C}$	-0.1		0.02	$\mu\text{A}$
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	-1.0		0.02	
$V_{CC}$ to OUT On-Resistance	$R_{ON}$	$V_{CC} = 4.75V$ , $I_{OUT} = 150\text{mA}$				3.1	$\Omega$
		$V_{CC} = 3.15V$ , $I_{OUT} = 65\text{mA}$				3.7	
		$V_{CC} = 2.38V$ , $I_{OUT} = 25\text{mA}$				4.6	
Output Voltage in Battery-Backup Mode	$V_{OUT}$	$V_{BATT} = 4.5V$ , $I_{OUT} = 20\text{mA}$		$V_{BATT} - 0.2$			V
		$V_{BATT} = 3.0V$ , $I_{OUT} = 10\text{mA}$		$V_{BATT} - 0.15$			
		$V_{BATT} = 2.25V$ , $I_{OUT} = 5\text{mA}$		$V_{BATT} - 0.15$			
Battery-Switchover Threshold ( $V_{CC} - V_{BATT}$ )	$V_{SW}$	$V_{CC} < V_{TH}$	Power-up		20		mV
			Power-down		-20		
Reset Threshold	$V_{TH}$	MAX636__KA46		4.50	4.63	4.75	V
		MAX636__KA44		4.25	4.38	4.50	
		MAX636__KA31		3.00	3.08	3.15	
		MAX636__KA29		2.85	2.93	3.00	
		MAX636__KA26		2.55	2.63	2.70	
		MAX636__KA23		2.25	2.32	2.38	
$V_{CC}$ Falling Reset Delay	$t_{RD}$	$V_{CC}$ falling at 10V/ms			20		$\mu\text{s}$

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MAX6365-MAX6368

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC}$  = +2.4V to +5.5V,  $V_{BATT}$  = +3.0V,  $\overline{CE}$  IN =  $V_{CC}$ , reset not asserted,  $T_A$  = -40°C to +85°C. Typical values are at  $T_A$  = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Reset Active Timeout Period	t <sub>RP</sub>			150		280	ms
$\overline{\text{RESET}}$ Output Voltage	V <sub>OL</sub>	Reset asserted, V <sub>BATT</sub> = 0	I <sub>SINK</sub> = 1.6mA, V <sub>CC</sub> ≥ 2.1V			0.3	V
			I <sub>SINK</sub> = 100μA, V <sub>CC</sub> ≥ 1.2V			0.4	
	V <sub>OH</sub>	Reset not asserted (MAX636_L only)	I <sub>SOURCE</sub> = 500μA, V <sub>CC</sub> ≥ V <sub>TH</sub> (MAX)	0.8 × V <sub>CC</sub>			
RESET Output Voltage	V <sub>OL</sub>	Reset not asserted	I <sub>SINK</sub> = 1.6mA, V <sub>CC</sub> ≥ V <sub>TH</sub> (MAX)			0.3	V
	V <sub>OH</sub>	Reset not asserted, V <sub>BATT</sub> = 0 (MAX636_H only) (Note 3)	I <sub>SOURCE</sub> = 1mA, V <sub>CC</sub> ≥ 1.8V	0.7 × V <sub>CC</sub>			
			I <sub>SOURCE</sub> = 200μA, V <sub>CC</sub> ≥ 1.2V	0.8 × V <sub>CC</sub>			
$\overline{\text{RESET}}$ Output Leakage Current	I <sub>LKG</sub>	MAX636_P and MAX636_H only				1	μA
MANUAL RESET (MAX6365 only)							
$\overline{\text{MR}}$ Input Voltage	V <sub>IL</sub>					0.3 × V <sub>CC</sub>	V
	V <sub>IH</sub>			0.7 × V <sub>CC</sub>			
Pullup Resistance				20			kΩ
Minimum Pulse Width				1			μs
Glitch Immunity		V <sub>CC</sub> = 3.3V		100			ns
$\overline{\text{MR}}$ to Reset Delay		V <sub>CC</sub> = 3.3V		120			ns
WATCHDOG (MAX6366 only)							
Watchdog Timeout Period	t <sub>WD</sub>			1.00	1.65	2.25	s
Minimum WDI Input Pulse Width	t <sub>WDI</sub>			100			ns
WDI Input Voltage	V <sub>IL</sub>					0.3 × V <sub>CC</sub>	V
	V <sub>IH</sub>			0.7 × V <sub>CC</sub>			
WDI Input Current				-1.0		1.0	μA
BATT ON (MAX6367 only)							
Output Voltage	V <sub>OL</sub>	I <sub>SINK</sub> = 3.2mA, V <sub>BATT</sub> = 2.1V				0.4	V
Output Short-Circuit Current		Sink current, V <sub>CC</sub> = 5V		60			mA
		Source current, V <sub>BATT</sub> ≥ 2V		10	30	100	μA

# SOT23, Low-Power $\mu$ P Supervisory Circuits with Battery Backup and Chip-Enable Gating

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = +2.4V$  to  $+5.5V$ ,  $V_{BATT} = +3.0V$ ,  $\overline{CE}$  IN =  $V_{CC}$ , reset not asserted,  $T_A = -40^\circ C$  to  $+85^\circ C$ . Typical values are at  $T_A = +25^\circ C$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RESET IN (MAX6368 only)							
RESET IN Threshold	V <sub>RTH</sub>			1.185	1.235	1.285	V
RESET IN Leakage Current				±0.01		±25	nA
RESET IN to Reset Delay		V <sub>OD</sub> = 50mV, RESET IN falling		1.5			µs
CHIP-ENABLE GATING							
CE IN Leakage Current		Reset asserted		±1			µA
CE IN to CE OUT Resistance		Reset not asserted (Note 4)		20		100	Ω
CE OUT Short-Circuit Current		Reset asserted, CE OUT = 0		0.75		2.0	mA
CE IN to CE OUT Propagation Delay		50Ω source, C <sub>LOAD</sub> = 50pF	V <sub>CC</sub> = 4.75V	1.5		7	ns
			V <sub>CC</sub> = 3.15V	2		9	
CE OUT Output Voltage High		V <sub>CC</sub> = 5V, V <sub>CC</sub> ≥ V <sub>BATT</sub> , I <sub>SOURCE</sub> = 100µA		0.8 × V <sub>CC</sub>			V
		V <sub>CC</sub> = 0, V <sub>BATT</sub> ≥ 2.2V, I <sub>SOURCE</sub> = 1µA		V <sub>BATT</sub> - 0.1			
Reset-to-CE OUT Delay				12			µs

**Note 1:** All devices are 100% production tested at  $T_A = +25^\circ C$ . Limits over temperature are guaranteed by design.

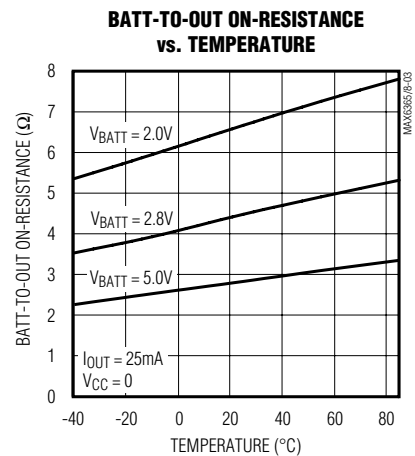
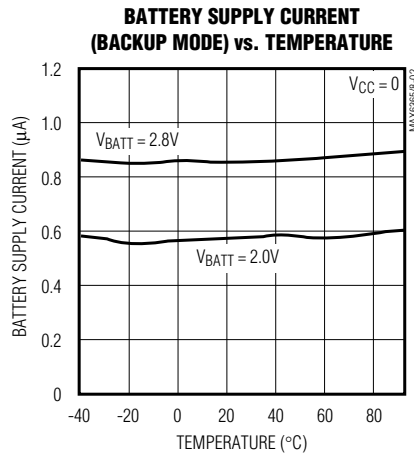
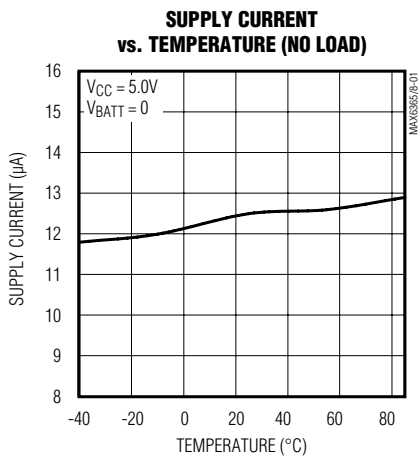
**Note 2:**  $V_{BATT}$  can be 0 anytime, or  $V_{CC}$  can go down to 0 if  $V_{BATT}$  is active (except at startup).

**Note 3:** RESET is pulled up to OUT. Specifications apply for OUT =  $V_{CC}$  or OUT = BATT.

**Note 4:** The chip-enable resistance is tested with  $V_{CC} = V_{TH(MAX)}$  and  $\overline{CE}$  IN =  $V_{CC}/2$ .

## Typical Operating Characteristics

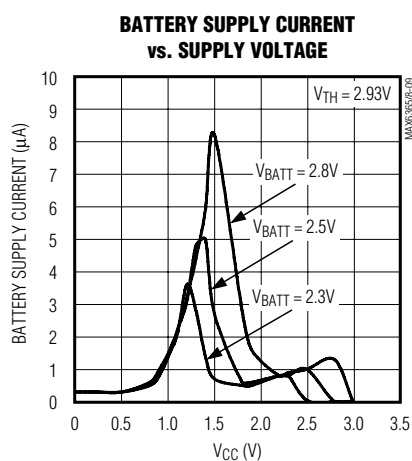
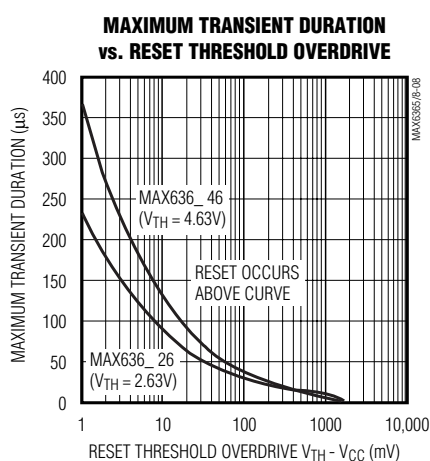
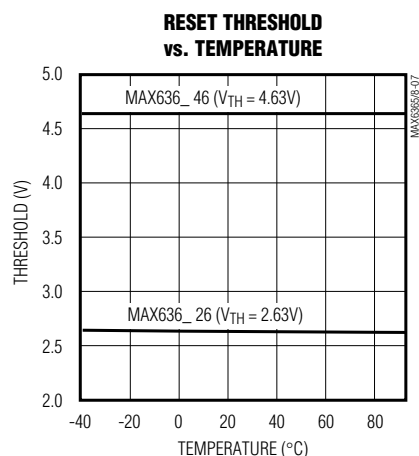
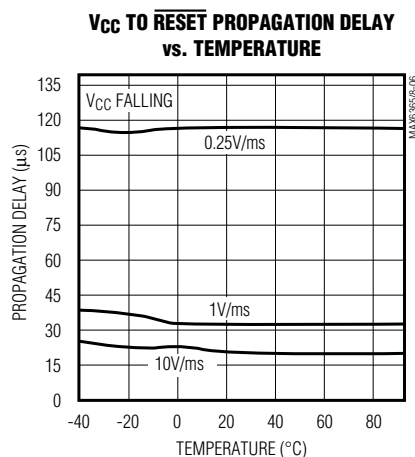
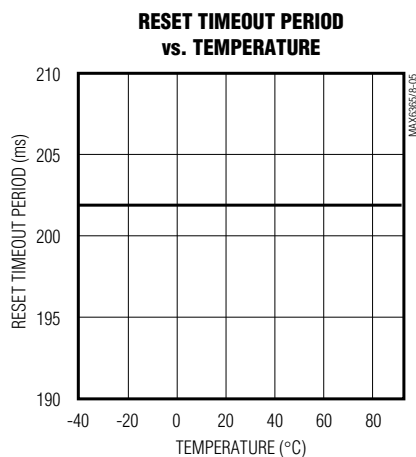
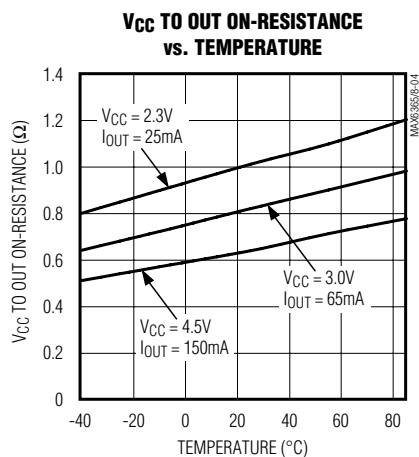
( $T_A = +25^\circ C$ , unless otherwise noted.)



# SOT23, Low-Power $\mu$ P Supervisory Circuits with Battery Backup and Chip-Enable Gating

## Typical Operating Characteristics (continued)

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

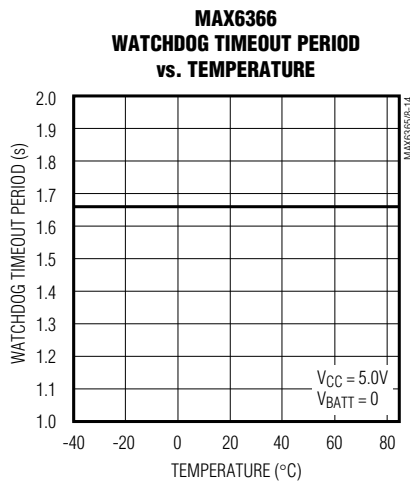
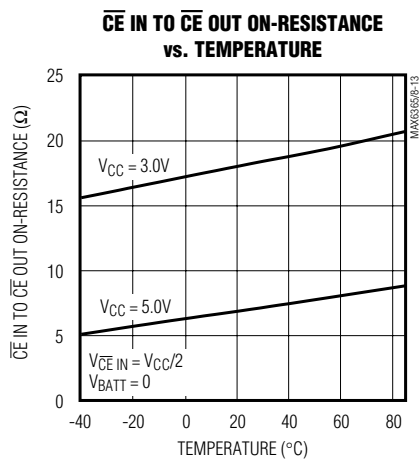
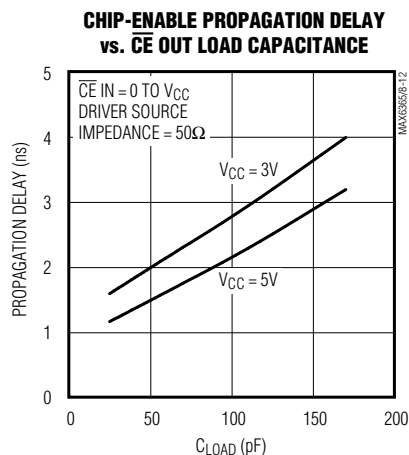
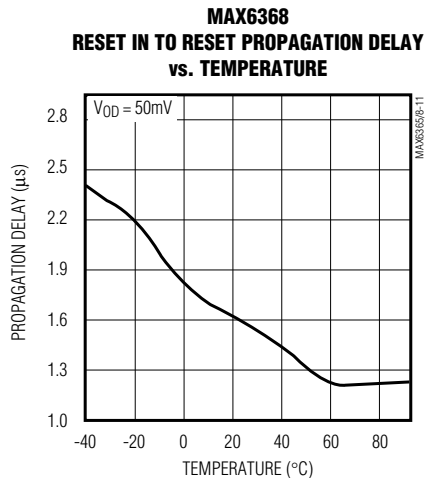
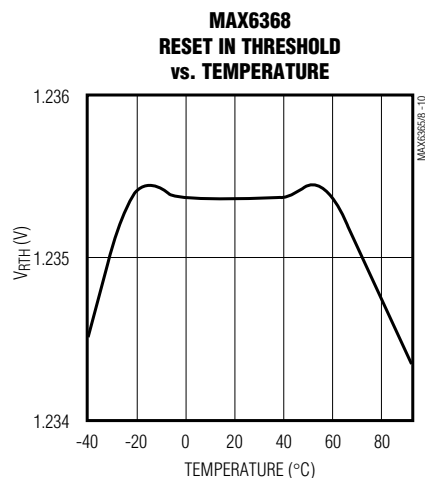


MAX6365-MAX6368

# SOT23, Low-Power $\mu$ P Supervisory Circuits with Battery Backup and Chip-Enable Gating

## Typical Operating Characteristics (continued)

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



# SOT23, Low-Power $\mu$ P Supervisory Circuits with Battery Backup and Chip-Enable Gating

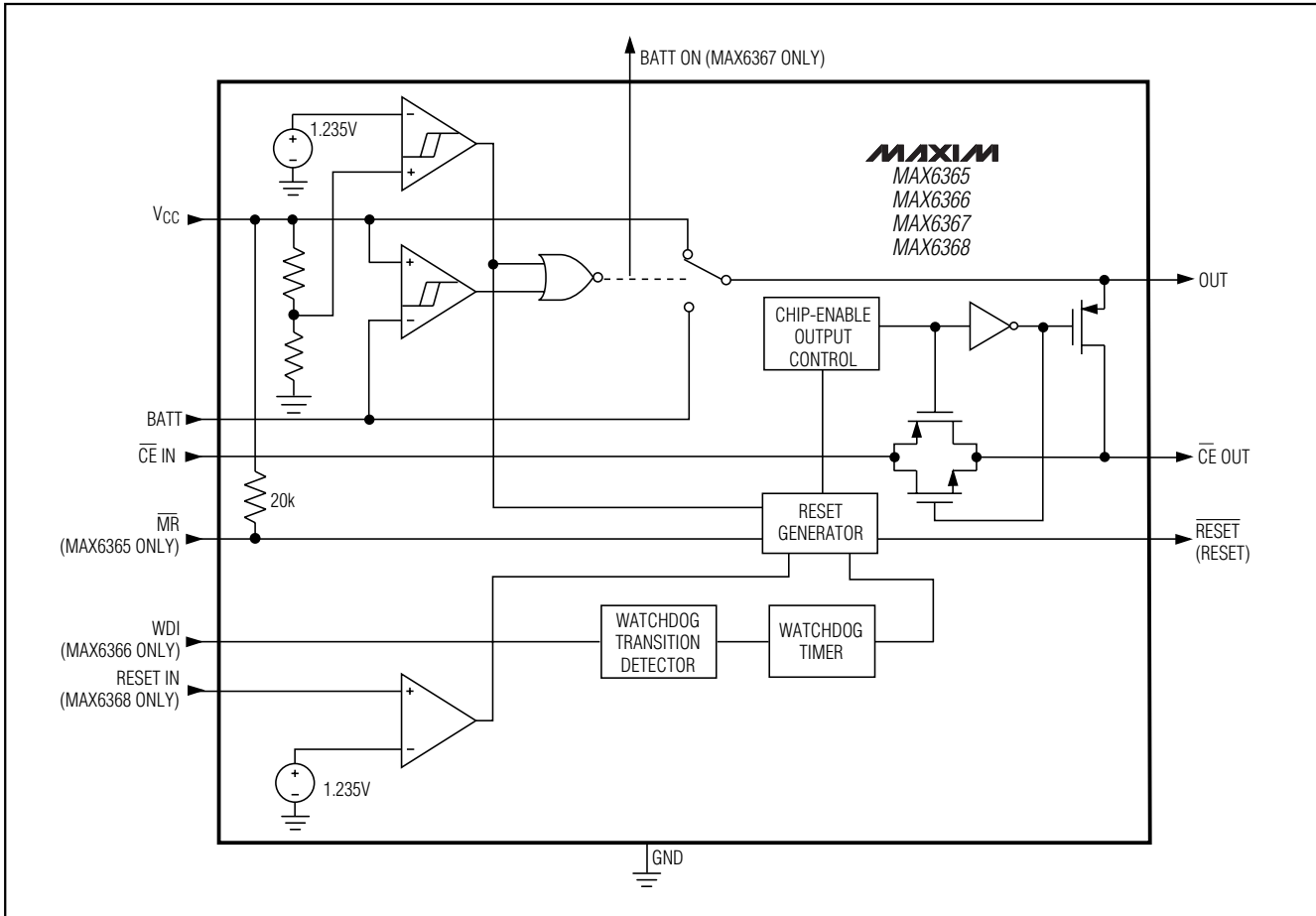
## Pin Description

MAX6365-MAX6368

PIN	NAME	FUNCTION
1	RESET	Active-High Reset Output. RESET asserts high continuously when $V_{CC}$ is below the reset threshold ( $V_{TH}$ ), $\overline{MR}$ is low, or RESET IN is low. It asserts in pulses when the internal watchdog times out. RESET remains asserted for the reset timeout period ( $t_{RP}$ ) after $V_{CC}$ rises above the reset threshold, after the manual reset input goes from low to high, after RESET IN goes high, or after the watchdog triggers a reset event. RESET is an open-drain active-high reset output.
	$\overline{RESET}$	Active-Low Reset Output. $\overline{RESET}$ asserts low continuously when $V_{CC}$ is below the reset threshold ( $V_{TH}$ ), the manual reset input is low, or RESET IN is low. It asserts low in pulses when the internal watchdog times out. $\overline{RESET}$ remains asserted low for the reset timeout period ( $t_{RP}$ ) after $V_{CC}$ rises above the reset threshold, after the manual reset input goes from low to high, after RESET IN goes high, or after the watchdog triggers a reset event. The MAX636_L is an active-low push-pull output, while the MAX636_P is an active-low open-drain output.
2	$\overline{CE}$ IN	Chip-Enable Input. The input to chip-enable gating circuitry. Connect to GND or OUT if not used.
3	GND	Ground
4	$\overline{MR}$	<b>MAX6365</b> Manual-Reset Input. Maintaining logic low on $\overline{MR}$ asserts a reset. Reset output remains asserted as long as $\overline{MR}$ is low and for the reset timeout period ( $t_{RP}$ ) after $\overline{MR}$ transitions from low to high. Leave unconnected, or connect to $V_{CC}$ if not used. $\overline{MR}$ has an internal 20k $\Omega$ pullup to $V_{CC}$ .
	WDI	<b>MAX6366</b> Watchdog Input. If WDI remains high or low for longer than the watchdog timeout period ( $t_{WD}$ ), the internal watchdog timer runs out and a reset pulse is triggered for the reset timeout period ( $t_{RP}$ ). The internal watchdog clears whenever reset asserts or whenever WDI sees a rising or falling edge (Figure 2).
	BATT ON	<b>MAX6367</b> Battery-On Output. BATT ON goes high when in battery backup mode.
	RESET IN	<b>MAX6368</b> Reset Input. When RESET IN falls below 1.235V, reset asserts. Reset output remains asserted as long as RESET IN is low and for at least $t_{RP}$ after RESET IN goes high.
5	$V_{CC}$	Supply Voltage, 1.2V to 5.5V. Reset asserts when $V_{CC}$ drops below the reset threshold voltage ( $V_{TH}$ ). Reset remains asserted until $V_{CC}$ rises above $V_{TH}$ and for at least $t_{RP}$ after $V_{CC}$ rises above $V_{TH}$ .
6	OUT	Output. OUT sources from $V_{CC}$ when not in reset and from the greater of $V_{CC}$ or BATT when $V_{CC}$ is below the reset threshold.
7	BATT	Backup-Battery Input. When $V_{CC}$ falls below the reset threshold, OUT switches to BATT if $V_{BATT}$ is 20mV greater than $V_{CC}$ . When $V_{CC}$ rises 20mV above $V_{BATT}$ , OUT switches to $V_{CC}$ . The 40mV hysteresis prevents repeated switching if $V_{CC}$ falls slowly.
8	$\overline{CE}$ OUT	Chip-Enable Output. $\overline{CE}$ OUT goes low only when $\overline{CE}$ IN is low and reset is not asserted. If $\overline{CE}$ IN is low when reset is asserted, $\overline{CE}$ OUT will stay low for 12 $\mu$ s (typ) or until $\overline{CE}$ IN goes high, whichever occurs first.

# SOT23, Low-Power $\mu$ P Supervisory Circuits with Battery Backup and Chip-Enable Gating

## Functional Diagram



## Detailed Description

The *Typical Operating Circuit* shows a typical connection for the MAX6365–MAX6368. OUT powers the static random-access memory (SRAM). If  $V_{CC}$  is greater than the reset threshold ( $V_{TH}$ ), or if  $V_{CC}$  is lower than  $V_{TH}$  but higher than  $V_{BATT}$ ,  $V_{CC}$  is connected to OUT. If  $V_{CC}$  is lower than  $V_{TH}$  and  $V_{CC}$  is less than  $V_{BATT}$ , BATT is connected to OUT. OUT supplies up to 150mA from  $V_{CC}$ . In battery-backup mode, an internal MOSFET connects the backup battery to OUT. The on-resistance of the MOSFET is a function of backup-battery voltage and is shown in the BATT-to-OUT On-Resistance vs. Temperature graph in the *Typical Operating Characteristics*.

### Chip-Enable Signal Gating

The MAX6365–MAX6368 provide internal gating of  $\overline{CE}$  signals to prevent erroneous data from being written to

CMOS RAM in the event of a power failure. During normal operation, the  $\overline{CE}$  gate is enabled and passes all  $\overline{CE}$  transitions. When reset asserts, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. All of these devices use a series transmission gate from  $\overline{CE}$  IN to  $\overline{CE}$  OUT. The 2ns propagation delay from  $\overline{CE}$  IN to  $\overline{CE}$  OUT allows the devices to be used with most  $\mu$ Ps and high-speed DSPs.

During normal operation,  $\overline{CE}$  IN is connected to  $\overline{CE}$  OUT through a low on-resistance transmission gate. This is valid when reset is not asserted. If  $\overline{CE}$  IN is high when reset is asserted,  $\overline{CE}$  OUT remains high regardless of any subsequent transitions on  $\overline{CE}$  IN during the reset event.

If  $\overline{CE}$  IN is low when reset is asserted,  $\overline{CE}$  OUT is held low for 12 $\mu$ s to allow completion of the read/write operation (Figure 1). After the 12 $\mu$ s delay expires, the  $\overline{CE}$



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OUT goes high and stays high regardless of any subsequent transitions on  $\overline{\text{CE}}$  IN during the reset event. When  $\overline{\text{CE}}$  OUT is disconnected from  $\overline{\text{CE}}$  IN,  $\overline{\text{CE}}$  OUT is actively pulled up to OUT.

The propagation delay through the chip-enable circuitry depends on both the source impedance of the drive to  $\overline{\text{CE}}$  IN and the capacitive loading at  $\overline{\text{CE}}$  OUT. The chip-enable propagation delay is production tested from the 50% point of  $\overline{\text{CE}}$  IN to the 50% point of  $\overline{\text{CE}}$  OUT, using a 50 $\Omega$  driver and 50pF load capacitance. Minimize the capacitive load at  $\overline{\text{CE}}$  OUT to minimize propagation delay, and use a low-output-impedance driver.

## Backup-Battery Switchover

In a brownout or power failure, it may be necessary to preserve the contents of the RAM. With a backup battery installed at BATT, the MAX6365-MAX6368 automatically switch the RAM to backup power when  $V_{\text{CC}}$  falls. The MAX6367 has a BATT ON output that goes high in battery-backup mode. These devices require two conditions before switching to battery-backup mode:

- 1)  $V_{\text{CC}}$  must be below the reset threshold.
- 2)  $V_{\text{CC}}$  must be below  $V_{\text{BATT}}$ .

Table 1 lists the status of the inputs and outputs in battery-backup mode. The devices do not power up if the only voltage source is on BATT. OUT only powers up from  $V_{\text{CC}}$  at startup.

**Table 1. Input and Output Status in Battery-Backup Mode**

PIN	STATUS
$V_{\text{CC}}$	Disconnected from OUT
OUT	Connected to BATT
BATT	Connected to OUT. Current drawn from the battery is less than 1 $\mu$ A (at $V_{\text{BATT}} = 2.8\text{V}$ , excluding $I_{\text{OUT}}$ ) when $V_{\text{CC}} = 0$ .
RESET/RESET	Asserted
BATT ON	High state
$\overline{\text{MR}}$ , RESET IN, $\overline{\text{CE}}$ IN, WDI	Inputs ignored
$\overline{\text{CE}}$ OUT	Connected to OUT

## Manual Reset Input (MAX6365 Only)

Many  $\mu$ P-based products require manual reset capability, allowing the user or external logic circuitry to initiate a reset. For the MAX6365, a logic low on  $\overline{\text{MR}}$  asserts reset. Reset remains asserted while  $\overline{\text{MR}}$  is low and for a minimum of 150ms ( $t_{\text{RP}}$ ) after it returns high.  $\overline{\text{MR}}$  has an internal 20k $\Omega$  pullup resistor to  $V_{\text{CC}}$ . This input can be driven with TTL/CMOS logic levels or with open-drain/collector outputs. Connect a normally open momentary switch from  $\overline{\text{MR}}$  to GND to create a manual reset function; external debounce circuitry is not required. If  $\overline{\text{MR}}$  is driven from long cables or the device is used in a noisy environment, connect a 0.1 $\mu$ F capacitor from  $\overline{\text{MR}}$  to GND to provide additional noise immunity.

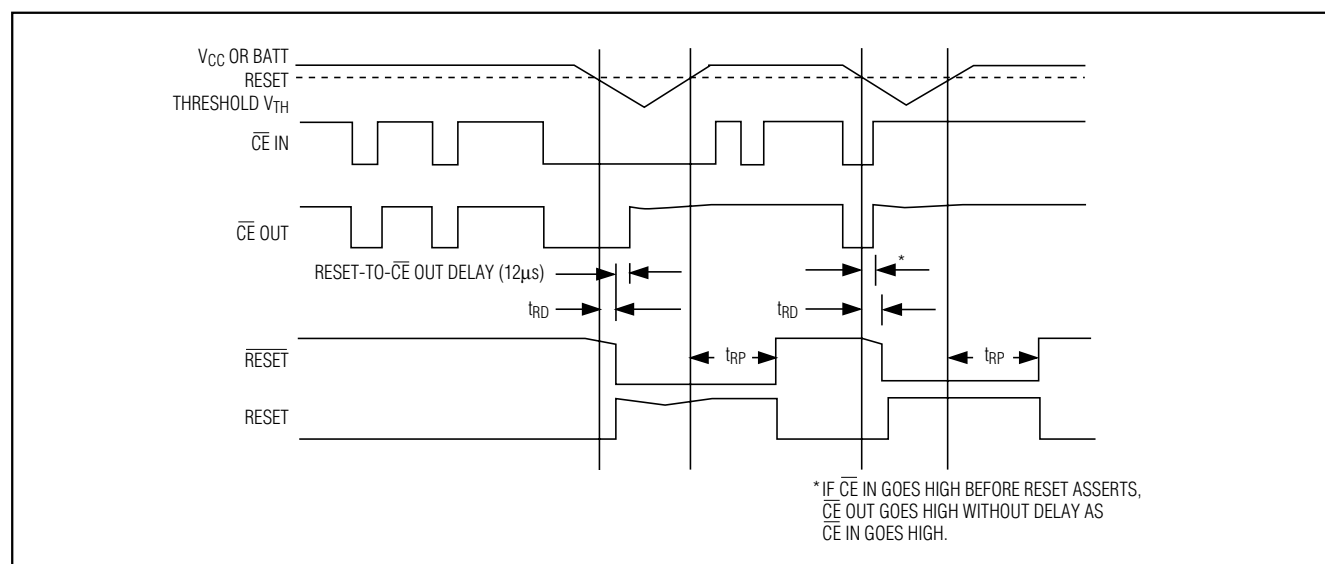


Figure 1. Reset and Chip-Enable Timing

# SOT23, Low-Power $\mu$ P Supervisory Circuits with Battery Backup and Chip-Enable Gating

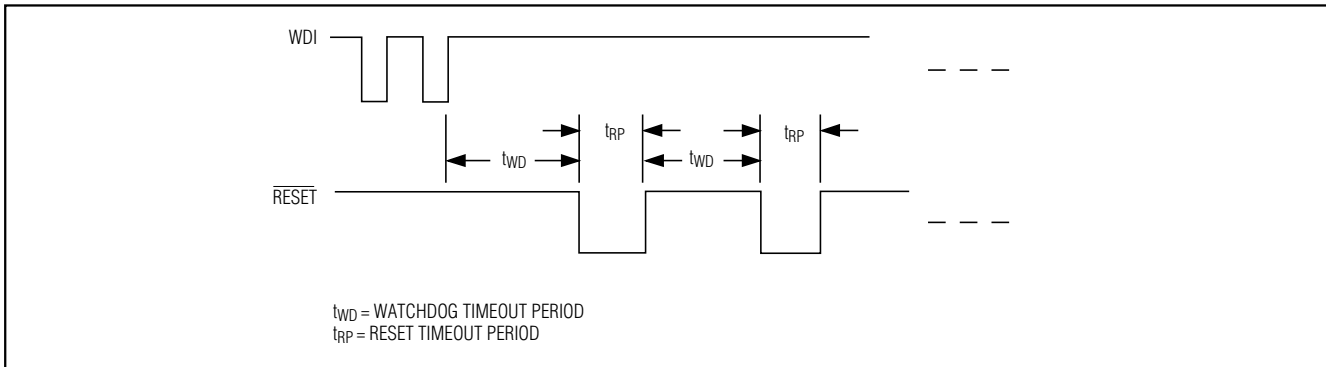


Figure 2. MAX6366 Watchdog Timeout Period and Reset Active Time

## Watchdog Input (MAX6366 Only)

The watchdog monitors  $\mu$ P activity through the watchdog input (WDI). If the  $\mu$ P becomes inactive, reset asserts. To use the watchdog function, connect WDI to a bus line or  $\mu$ P I/O line. A change of state (high to low, low to high, or a minimum 100ns pulse) resets the watchdog timer. If WDI remains high or low for longer than the watchdog timeout period ( $t_{WD}$ ), the internal watchdog timer runs out and a reset pulse is triggered for the reset timeout period ( $t_{RP}$ ). The internal watchdog timer clears whenever reset asserts or whenever WDI sees a rising or falling edge. If WDI remains in either a high or low state, a reset pulse asserts periodically after every  $t_{WD}$  (Figure 2). Leave WDI unconnected to disable the watchdog function.

## BATT ON Indicator (MAX6367 Only)

BATT ON is a push-pull output that drives high when in battery-backup mode. BATT ON typically sinks 3.2mA at 0.1V saturation voltage. In battery-backup mode, this terminal sources approximately 10 $\mu$ A from OUT. Use BATT ON to indicate battery-switchover status or to supply base drive to an external pass transistor for higher current applications (Figure 3).

## RESET IN Comparator (MAX6368 Only)

RESET IN is compared to an internal 1.235V reference. If the voltage at RESET IN is less than 1.235V, reset asserts. Use the RESET IN comparator as an undervoltage detector to signal a failing power supply or as a secondary power-supply reset monitor.

To program the reset threshold ( $V_{RTH}$ ) of the secondary power supply, use the following (see *Typical Operating Circuit*):

$$V_{RTH} = V_{REF} (R1 / R2 + 1)$$

where  $V_{REF} = 1.235V$ . To simplify the resistor selection, choose a value for R2 and calculate R1:

$$R1 = R2 [(V_{RTH} / V_{REF}) - 1]$$

Since the input current at RESET IN is 25nA (max), large values (up to 1M $\Omega$ ) can be used for R2 with no significant loss in accuracy. For example, in the *Typical Operating Circuit*, the MAX6368 monitors two supply voltages. To monitor the secondary 5V logic or analog supply with a 4.60V nominal programmed reset threshold, choose R2 = 100k $\Omega$ , and calculate R1 = 273k $\Omega$ .

## Reset Output

A  $\mu$ P's reset input starts the  $\mu$ P in a known state. The MAX6365-MAX6368  $\mu$ P supervisory circuits assert a reset to prevent code-execution errors during power-up, power-down, and brownout conditions. RESET is guaranteed to be a logic low or logic high, depending on the device chosen (see *Ordering Information*). RESET or  $\overline{\text{RESET}}$  asserts when  $V_{CC}$  is below the reset threshold and for at least 150ms ( $t_{RP}$ ) after  $V_{CC}$  rises above the reset threshold. RESET or  $\overline{\text{RESET}}$  also asserts when  $\overline{\text{MR}}$  is low (MAX6365) and when RESET IN is less than 1.235V (MAX6368). The MAX6366 watchdog function will cause RESET (or  $\overline{\text{RESET}}$ ) to assert in pulses following a watchdog timeout (Figure 2).

## Applications Information

### Operation Without a Backup Power Source

The MAX6365-MAX6368 provide battery-backup functions. If a backup power source is not used, connect BATT to GND and OUT to  $V_{CC}$ .

### Watchdog Software Considerations

One way to help the watchdog timer monitor the software execution more closely is to set and reset the watchdog at different points in the program rather than pulsing the watchdog input periodically. Figure 4 shows a flow diagram in which the I/O driving the

## SOT23, Low-Power $\mu$ P Supervisory Circuits with Battery Backup and Chip-Enable Gating

watchdog is set low in the beginning of the program, set high at the beginning of every subroutine or loop, and set low again when the program returns to the beginning. If the program should hang in any subroutine, the problem would be quickly corrected.

### Replacing the Backup Battery

When  $V_{CC}$  is above  $V_{TH}$ , the backup power source can be removed without danger of triggering a reset pulse. The device does not enter battery-backup mode when  $V_{CC}$  stays above the reset threshold voltage.

### Negative-Going $V_{CC}$ Transients

These supervisors are relatively immune to short-duration, negative-going  $V_{CC}$  transients. Resetting the  $\mu$ P when  $V_{CC}$  experiences only small glitches is usually not desirable.

The *Typical Operating Characteristics* section has a Maximum Transient Duration vs. Reset Threshold Overdrive graph for which reset is not asserted. The graph was produced using negative-going  $V_{CC}$  pulses,

starting at  $V_{CC}$  and ending below the reset threshold by the magnitude indicated (reset threshold overdrive). The graph shows the maximum pulse width that a negative-going  $V_{CC}$  transient can typically have without triggering a reset pulse. As the amplitude of the transient increases (i.e., goes further below the reset threshold), the maximum allowable pulse width decreases. Typically, a  $V_{CC}$  transient that goes 100mV below the reset threshold and lasts for 30 $\mu$ s will not trigger a reset pulse.

A 0.1 $\mu$ F bypass capacitor mounted close to the  $V_{CC}$  pin provides additional transient immunity.

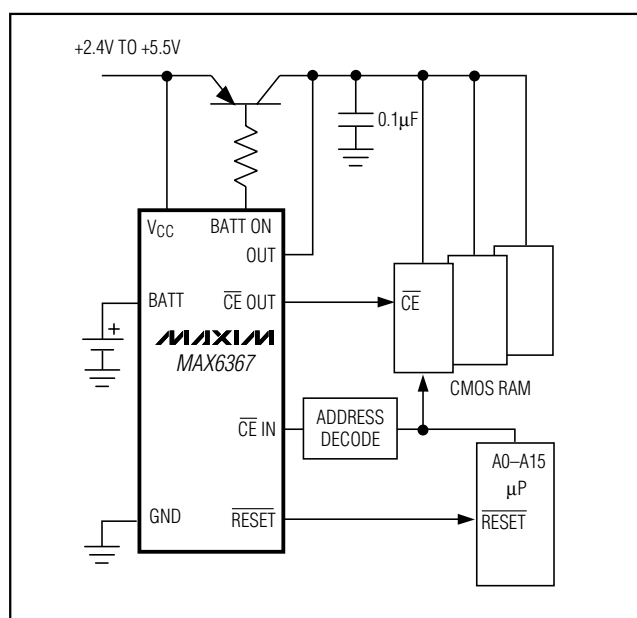


Figure 3. MAX6367 BATT ON Driving an External Pass Transistor

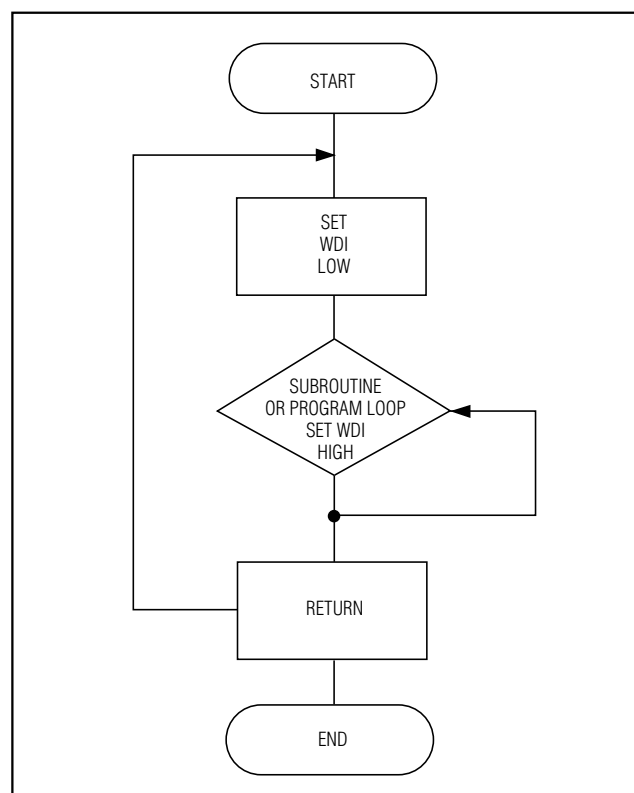


Figure 4. Watchdog Flow Diagram

# SOT23, Low-Power $\mu$ P Supervisory Circuits with Battery Backup and Chip-Enable Gating

## Reset Threshold Ranges

SUFFIX	RESET THRESHOLD RANGES (V)		
	MIN	TYP	MAX
46	4.50	4.63	4.75
44	4.25	4.38	4.50
31	3.00	3.08	3.15
29	2.85	2.93	3.00
26	2.55	2.63	2.70
23	2.25	2.32	2.38

## Device Marking Codes

PART	TOP MARK	PART	TOP MARK	PART	TOP MARK
MAX6365LKA23	AAAM	MAX6366PKA23	AABK	MAX6367HKA23	AACI
MAX6365LKA26	AAAL	MAX6366PKA26	AABJ	MAX6367HKA26	AACH
MAX6365LKA29*	AAAK	MAX6366PKA29*	AABI	MAX6367HKA29	AACG
MAX6365LKA31	AAAJ	MAX6366PKA31	AABH	MAX6367HKA31	AACF
MAX6365LKA44	AAAI	MAX6366PKA44	AABG	MAX6367HKA44	AACE
MAX6365LKA46*	AAAH	MAX6366PKA46*	AABF	MAX6367HKA46*	AACD
MAX6365PKA23	AAAS	MAX6366HKA23	AABQ	MAX6368LKA23	AACO
MAX6365PKA26	AAAR	MAX6366HKA26	AABP	MAX6368LKA26	AACN
MAX6365PKA29*	AAAQ	MAX6366HKA29	AABO	MAX6368LKA29*	AACM
MAX6365PKA31	AAAP	MAX6366HKA31	AABN	MAX6368LKA31	AACL
MAX6365PKA44	AAAO	MAX6366HKA44	AABM	MAX6368LKA44	AACK
MAX6365PKA46*	AAAN	MAX6366HKA46*	AABL	MAX6368LKA46*	AACJ
MAX6365HKA23	AAAY	MAX6367LKA23	AABW	MAX6368PKA23	AACU
MAX6365HKA26	AAAX	MAX6367LKA26	AABV	MAX6368PKA26	AACT
MAX6365HKA29	AAAW	MAX6367LKA29*	AABU	MAX6368PKA29*	AACS
MAX6365HKA31	AAAV	MAX6367LKA31	AABT	MAX6368PKA31	AACR
MAX6365HKA44	AAAU	MAX6367LKA44	AABS	MAX6368PKA44	AACQ
MAX6365HKA46*	AAAT	MAX6367LKA46*	AABR	MAX6368PKA46*	AACP
MAX6366LKA23	AABE	MAX6367PKA23	AACC	MAX6368HKA23	AADA
MAX6366LKA26	AABD	MAX6367PKA26	AACB	MAX6368HKA26	AACZ
MAX6366LKA29*	AABC	MAX6367PKA29*	AACA	MAX6368HKA29	AACY
MAX6366LKA31	AABB	MAX6367PKA31	AABZ	MAX6368HKA31	AACX
MAX6366LKA44	AABA	MAX6367PKA44	AABY	MAX6368HKA44	AACW
MAX6366LKA46*	AAAZ	MAX6367PKA46*	AABX	MAX6368HKA46*	AACV

\*These standard versions are available in small quantities through Maxim Distribution. Sample stock is generally held on standard versions only. Contact factory for availability of nonstandard versions.

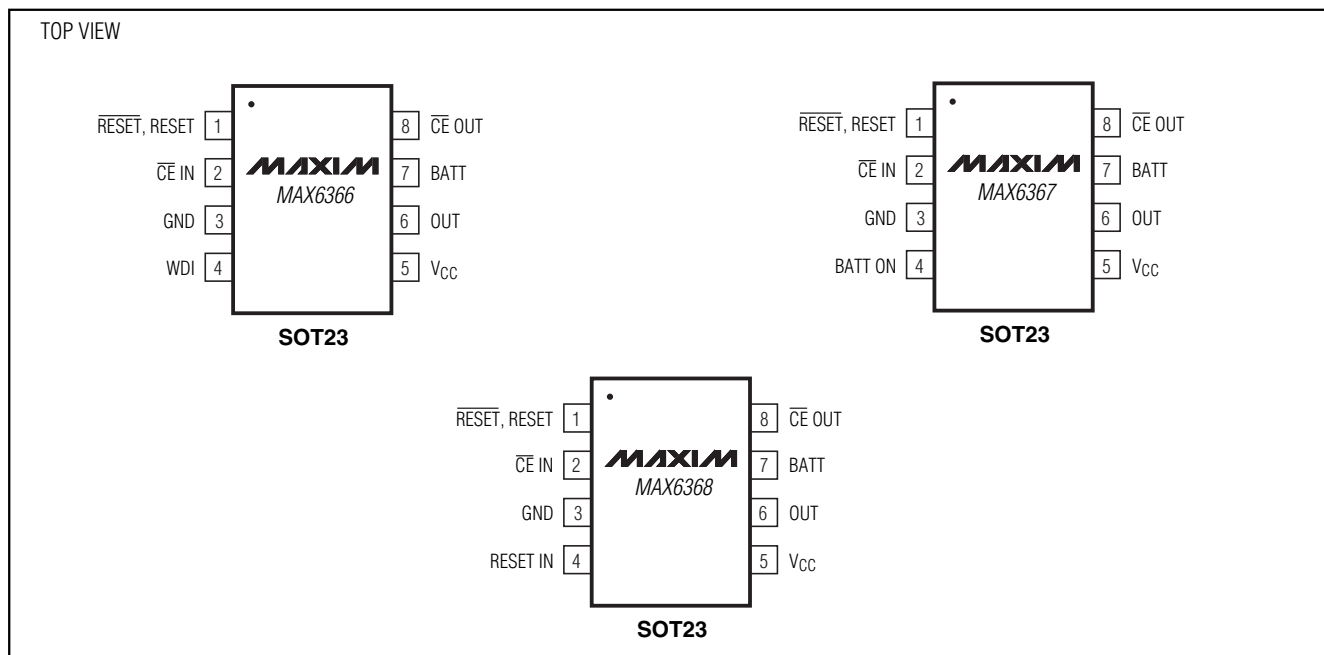
# SOT23, Low-Power $\mu$ P Supervisory Circuits with Battery Backup and Chip-Enable Gating

## Selector Guide

PART	MANUAL RESET INPUT	WATCH- DOG INPUT	BATT ON	RESET IN	RESET PUSH- PULL	RESET OPEN- DRAIN	RESET OPEN- DRAIN	CHIP- ENABLE GATING
MAX6365LKA__	✓				✓			✓
MAX6365PKA__	✓					✓		✓
MAX6365HKA__	✓						✓	✓
MAX6366LKA__		✓			✓			✓
MAX6366PKA__		✓				✓		✓
MAX6366HKA__		✓					✓	✓
MAX6367LKA__			✓		✓			✓
MAX6367PKA__			✓			✓		✓
MAX6367HKA__			✓				✓	✓
MAX6368LKA__				✓	✓			✓
MAX6368PKA__				✓		✓		✓
MAX6368HKA__				✓			✓	✓

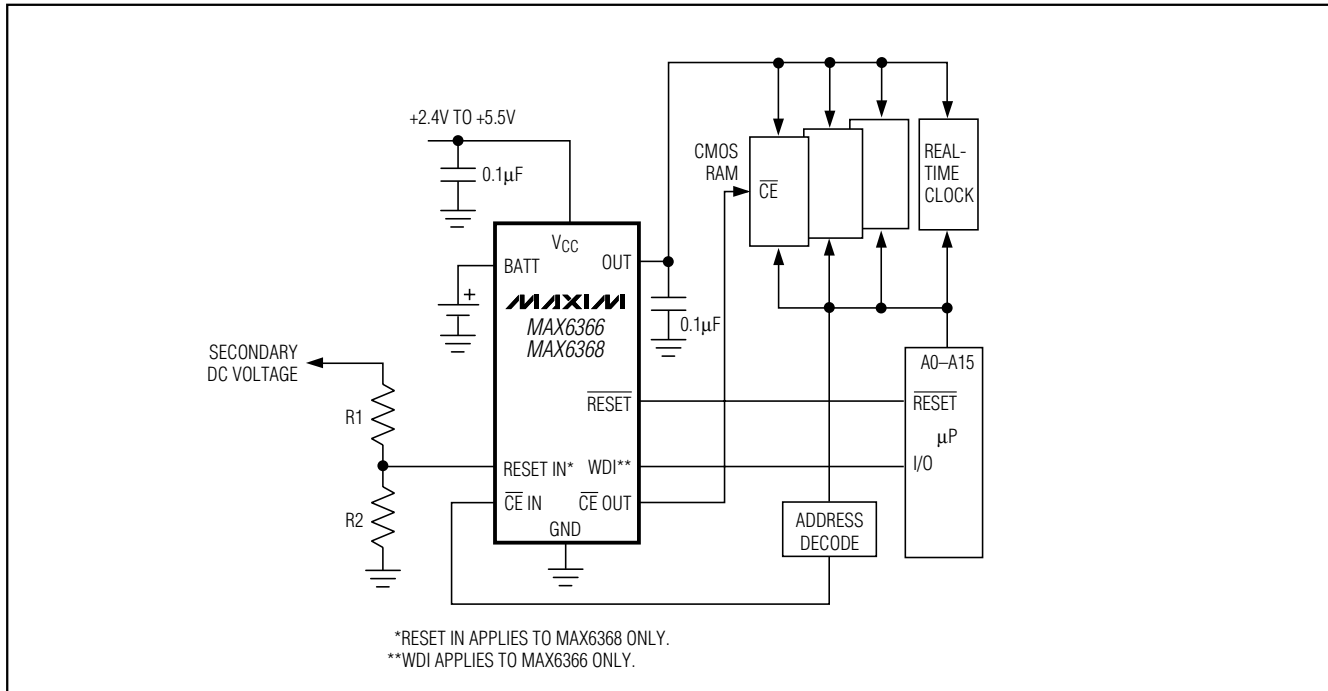
MAX6365-MAX6368

## Pin Configurations (continued)



# SOT23, Low-Power $\mu$ P Supervisory Circuits with Battery Backup and Chip-Enable Gating

## Typical Operating Circuit



## Chip Information

TRANSISTOR COUNT: 729

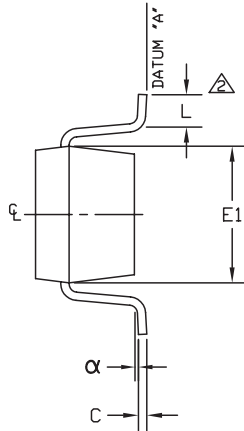
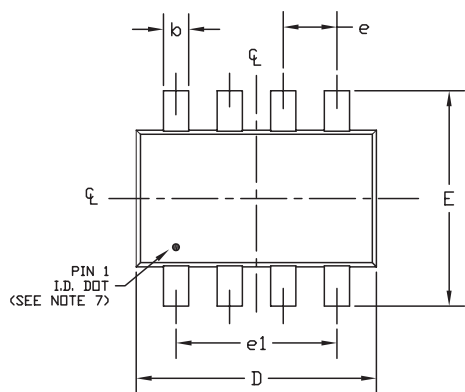
PROCESS: CMOS

# SOT23, Low-Power $\mu$ P Supervisory Circuits with Battery Backup and Chip-Enable Gating

## Package Information

MAX6365-MAX6368

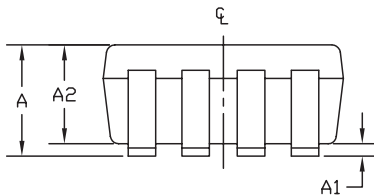
SOT23, 8LEPS



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.28	0.45
C	0.09	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.10	0.60
e	0.65 ref	
e1	1.95 ref	
$\alpha$	0°	10°

### NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2.  $\Delta$  FOOT LENGTH MEASURED REFERENCE TO FLAT FOOT SURFACE PARALLEL TO DATUM "A".
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. EIAJ REF. NUMBER SC-74 (6 LEAD VERSION)
6. COPLANARITY 4 MILS. MAX.
7. PIN 1 I.D. DOT IS 0.3 MM  $\phi$  MIN. LOCATED ABOVE PIN 1.
8. MEETS JEDEC MQ178.



<b>MAXIM</b>			
PROPRIETARY INFORMATION			
TITLE: PACKAGE OUTLINE, SOT-23, 8L			
APPROVAL	DOCUMENT CONTROL NO. 21-0078	REV C	1/1

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