

## FEATURES

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

## DESCRIPTION

This 16-bit registered transceiver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

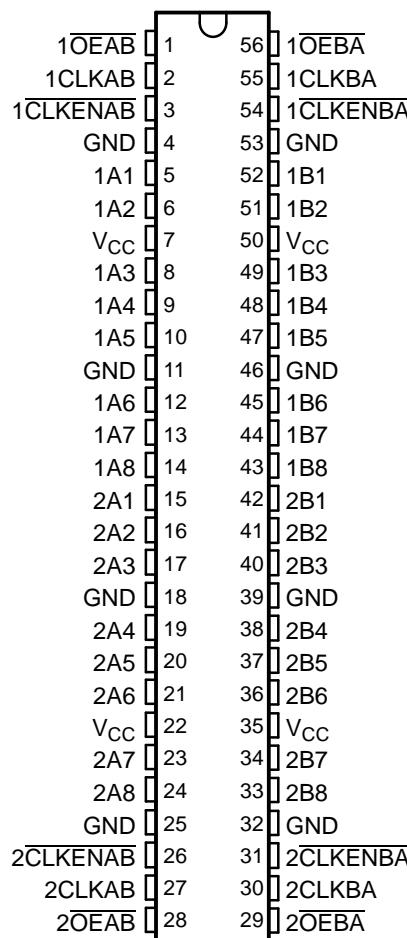
The SN74ALVCH16952 contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. This device can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input, provided that the clock-enable (CLKENAB or CLKENBA) input is low. Taking the output-enable ( $\overline{OEAB}$  or  $\overline{OEBA}$ ) input low accesses the data on either port.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16952 is characterized for operation from -40°C to 85°C.

### DGG, DGV, OR DL PACKAGE (TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus, EPIC are trademarks of Texas Instruments.

**SN74ALVCH16952**  
**16-BIT REGISTERED TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

SCES011E–JULY 1995–REVISED SEPTEMBER 2004

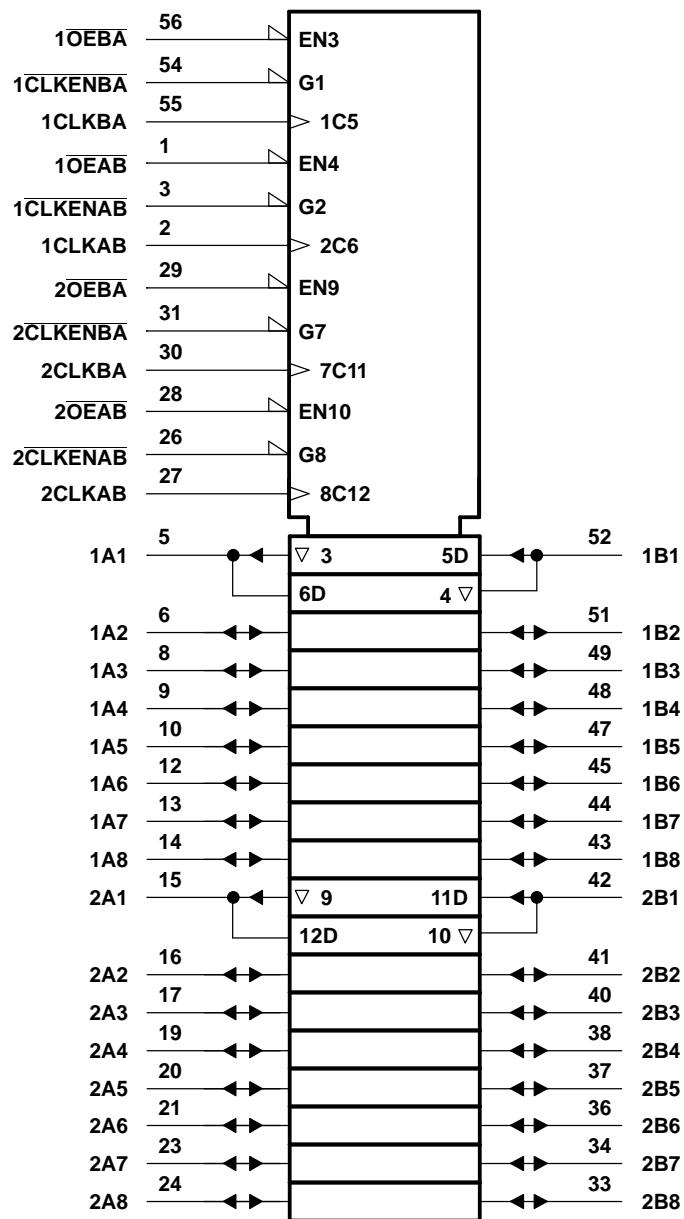


**FUNCTION TABLE<sup>(1)</sup>**

INPUTS				OUTPUT B
<b>CLKENAB</b>	<b>CLKAB</b>	<b>OEAB</b>	<b>A</b>	
H	X	L	X	$B_0^{(2)}$
X	L	L	X	$B_0^{(2)}$
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

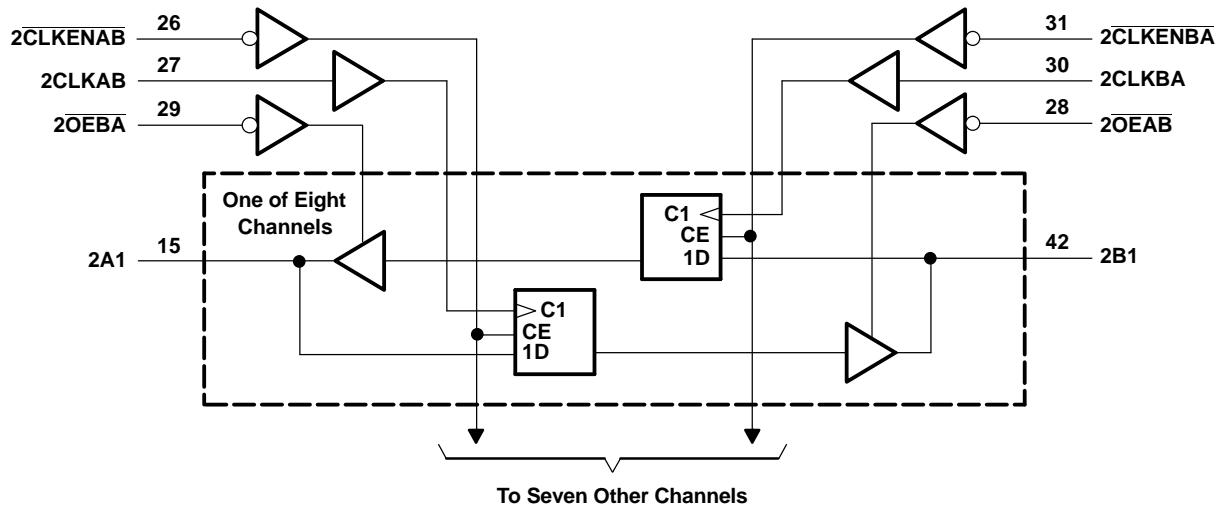
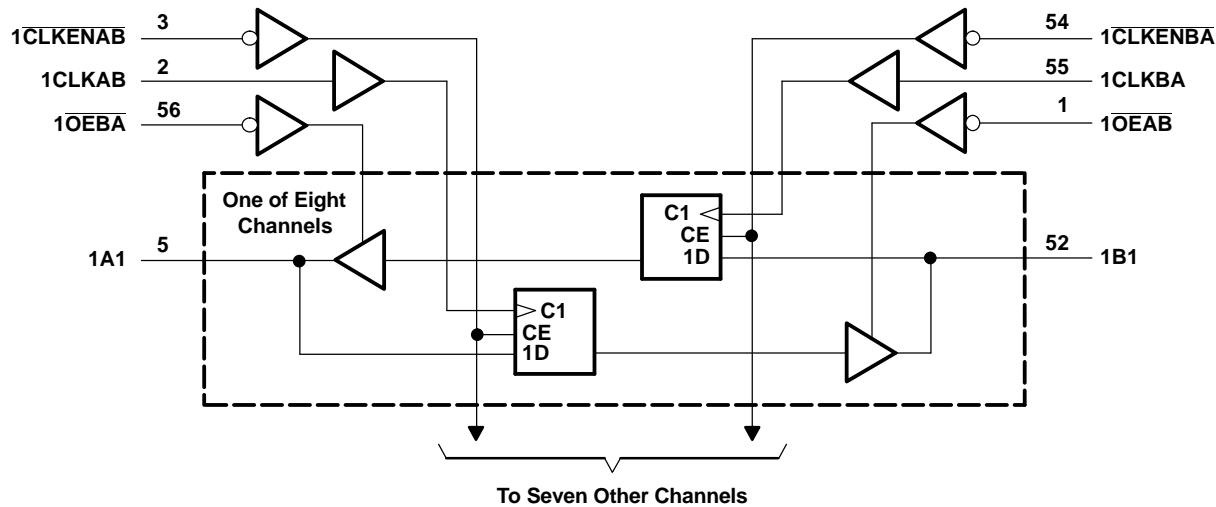
(1) A-to-B data flow is shown; B-to-A data flow is similar, but uses  $\overline{\text{CLKENBA}}$ ,  $\text{CLKBA}$ , and  $\overline{\text{OEBA}}$ .  
(2) Level of B before the indicated steady-state input conditions were established

**LOGIC SYMBOL<sup>(1)</sup>**



(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**LOGIC DIAGRAM (POSITIVE LOGIC)**



**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	4.6	V
$V_I$	Input voltage range	Except I/O ports <sup>(2)</sup>	-0.5	4.6
		I/O ports <sup>(2)(3)</sup>	-0.5	$V_{CC} + 0.5$
$V_O$	Output voltage range <sup>(2)(3)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	$I_{IK} < 0$		-50	mA
$I_{OK}$	$I_{OK} < 0$		-50	mA
$I_O$	Continuous output current		$\pm 50$	mA
	Continuous current through each $V_{CC}$ or GND		$\pm 100$	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DGG package	81	°C/W
		DGV package	86	
		DL package	74	
$T_{stg}$	Storage temperature range	-65	150	°C

- Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- This value is limited to 4.6 V maximum.
- The package thermal impedance is calculated in accordance with JESD 51.

**RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	1.65	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	1.7	
		$V_{CC} = 2.7$ V to 3.6 V	2	
$V_{IL}$	Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	0.7	
		$V_{CC} = 2.7$ V to 3.6 V	0.8	
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 1.65$ V	-4	mA
		$V_{CC} = 2.3$ V	-12	
		$V_{CC} = 2.7$ V	-12	
		$V_{CC} = 3$ V	-24	
$I_{OL}$	Low-level output current	$V_{CC} = 1.65$ V	4	mA
		$V_{CC} = 2.3$ V	12	
		$V_{CC} = 2.7$ V	12	
		$V_{CC} = 3$ V	24	
$\Delta t/\Delta v$	Input transition rise or fall rate		10	ns/V
$T_A$	Operating free-air temperature	-40	85	°C

- All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**SN74ALVCH16952**  
**16-BIT REGISTERED TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

SCES011E–JULY 1995–REVISED SEPTEMBER 2004

 **TEXAS**  
**INSTRUMENTS**  
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**ELECTRICAL CHARACTERISTICS**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = -100 $\mu$ A	1.65 V to 3.6 V	V <sub>CC</sub>	- 0.2		V
	I <sub>OH</sub> = -4 mA	1.65 V		1.2		
	I <sub>OH</sub> = -6 mA	2.3 V		2		
	I <sub>OH</sub> = -12 mA	2.3 V		1.7		
		2.7 V		2.2		
		3 V		2.4		
V <sub>OL</sub>	I <sub>OL</sub> = -24 mA	3 V		2		V
	I <sub>OL</sub> = 100 $\mu$ A	1.65 V to 3.6 V		0.2		
	I <sub>OL</sub> = 4 mA	1.65 V		0.45		
	I <sub>OL</sub> = 6 mA	2.3 V		0.4		
	I <sub>OL</sub> = 12 mA	2.3 V		0.7		
		2.7 V		0.4		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V		$\pm$ 5	$\mu$ A	
I <sub>I(hold)</sub>	V <sub>I</sub> = 0.58 V	1.65 V		25		$\mu$ A
	V <sub>I</sub> = 1.07 V	1.65 V		-25		
	V <sub>I</sub> = 0.7 V	2.3 V		45		
	V <sub>I</sub> = 1.7 V	2.3 V		-45		
	V <sub>I</sub> = 0.8 V	3 V		75		
	V <sub>I</sub> = 2 V	3 V		-75		
I <sub>OZ</sub> <sup>(3)</sup>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V		$\pm$ 10	$\mu$ A	
	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V		40	$\mu$ A	
$\Delta$ I <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V		750	$\mu$ A	
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		3.5	pF
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V		8.5	pF

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.  
 (2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.  
 (3) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

**TIMING REQUIREMENTS**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

		V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V $\pm$ 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V $\pm$ 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency			(1)	150	150	150	150	MHz
t <sub>w</sub>	Pulse duration	CLKEN high	(1)	3.3	3.3	3.3	3.3	3.3	ns
		CLK high or low	(1)	3.3	3.3	3.3	3.3	3.3	
t <sub>su</sub>	Setup time	Data before CLK	(1)	1.7	1.9	1.5	1.5	1.5	ns
		CLKEN before CLK	(1)	1.2	1	1	1	1	
t <sub>h</sub>	Hold time	Data after CLK	(1)	0.6	0.6	0.8	0.8	0.8	ns
		CLKEN after CLK	(1)	1.1	0.9	1.1	1.1	1.1	

(1) This information was not available at the time of publication.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT		
			MIN	TYP	MIN	MAX	MIN	MAX			
$f_{max}$			(1)		150		150		MHz		
$t_{pd}$	CLK	A or B	(1)		1	4.1		4.6	1	3.9	ns
$t_{en}$	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	(1)		1	5.4		5.3	1	4.4	ns
$t_{dis}$	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	(1)		1	5.3		4.4	1.1	4	ns

(1) This information was not available at the time of publication.

## OPERATING CHARACTERISTICS

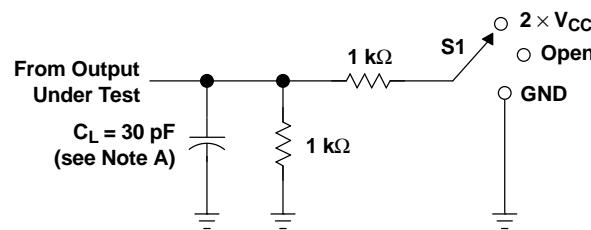
$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
		TYP	TYP	TYP	
$C_{pd}$ Power dissipation capacitance	Outputs enabled	$C_L = 0, f = 10\text{ MHz}$	(1)	53	pF
	Outputs disabled		(1)	34	
				40	

(1) This information was not available at the time of publication.

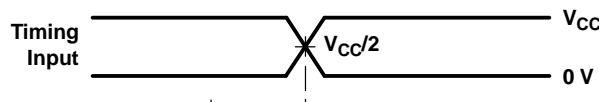
**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 1.8 \text{ V}$

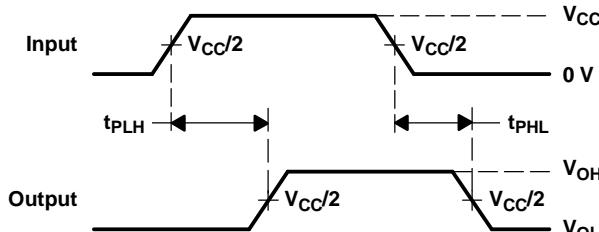


TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

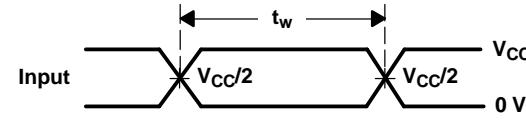
**LOAD CIRCUIT**



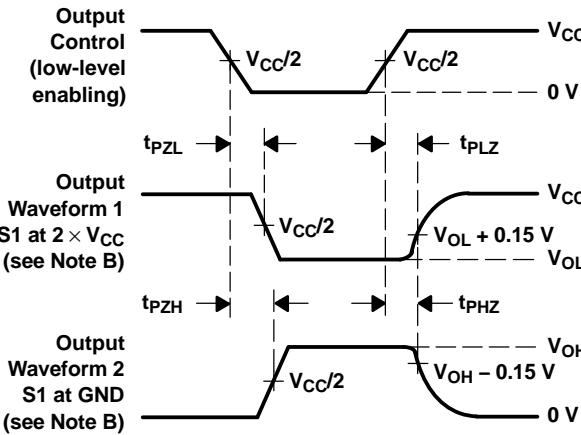
**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS  
PULSE DURATION**



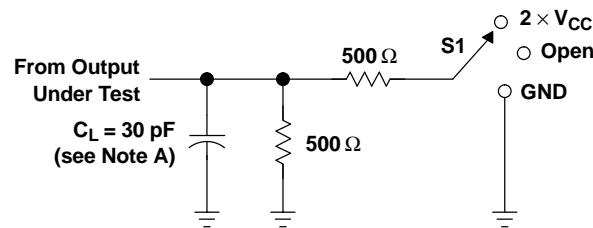
**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES**

NOTES:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
- The outputs are measured one at a time, with one transition per measurement.
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

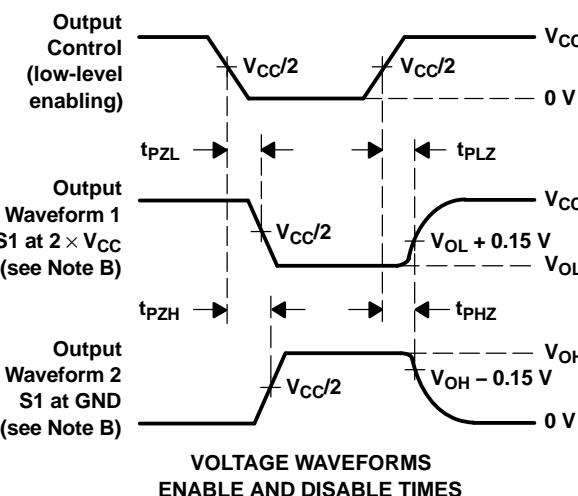
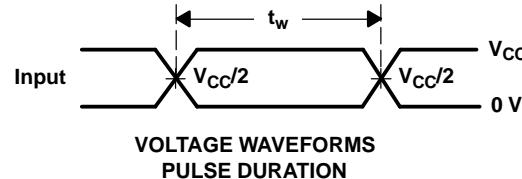
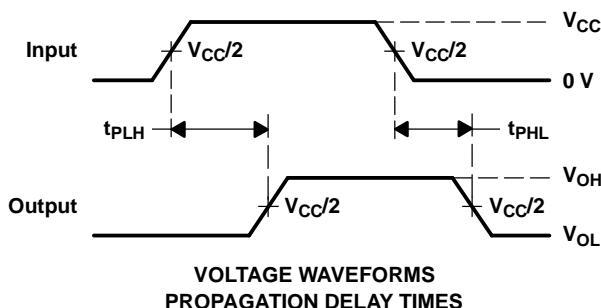
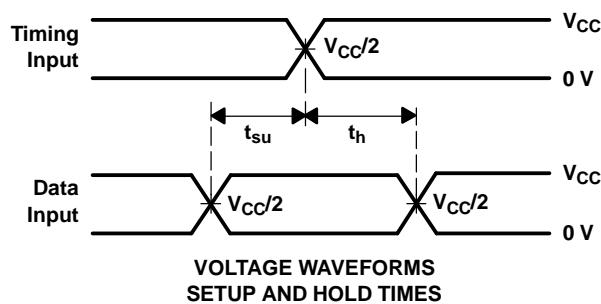
**Figure 1. Load Circuit and Voltage Waveforms**

**PARAMETER MEASUREMENT INFORMATION**  
 **$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$**



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times$ $V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

LOAD CIRCUIT



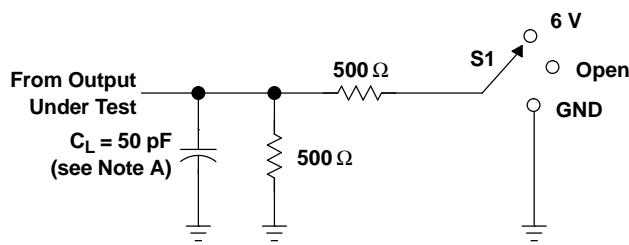
NOTES:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
- The outputs are measured one at a time, with one transition per measurement.
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

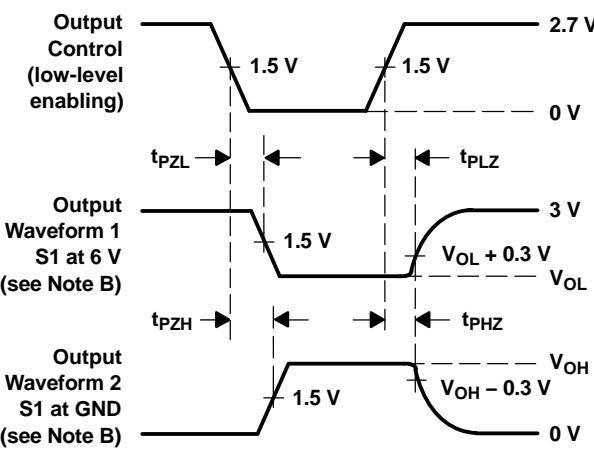
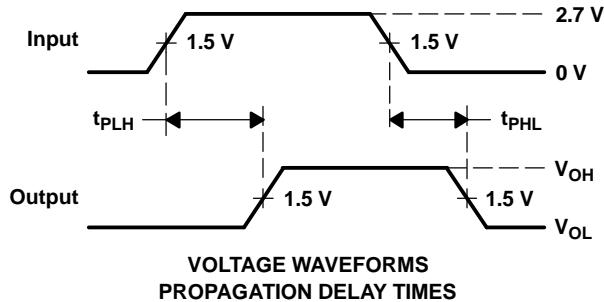
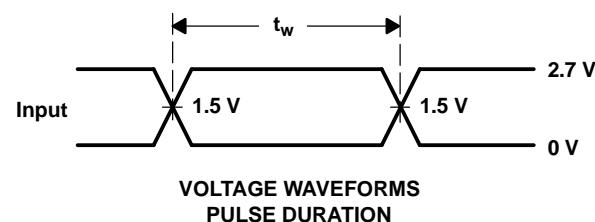
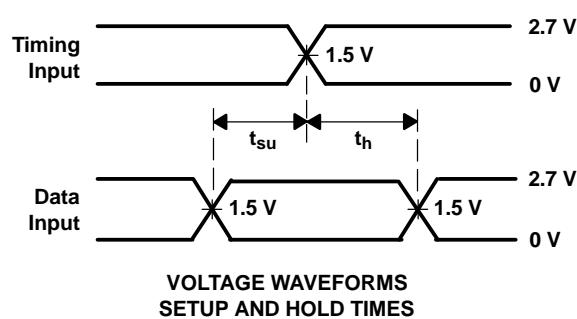
Figure 2. Load Circuit and Voltage Waveforms

**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V} \pm 0.3 \text{ V}$



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



NOTES:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- The outputs are measured one at a time, with one transition per measurement.
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 3. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ALVCH16952DGGR	Active	Production	TSSOP (DGG)   56	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16952
SN74ALVCH16952DGGR.B	Active	Production	TSSOP (DGG)   56	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16952

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

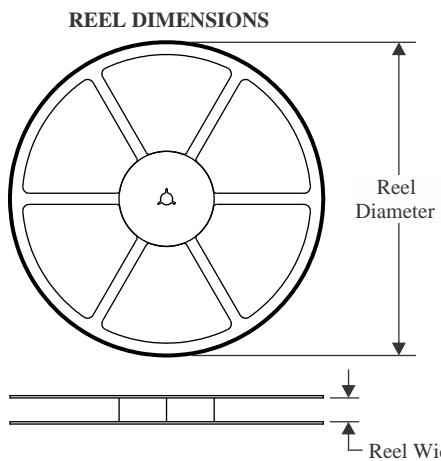
<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

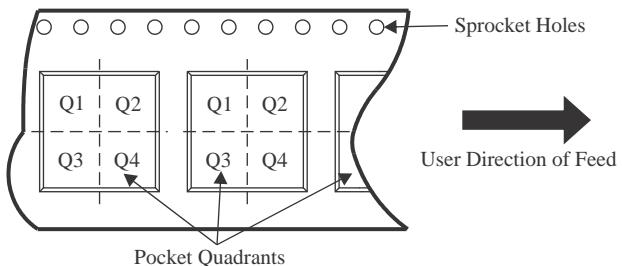
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

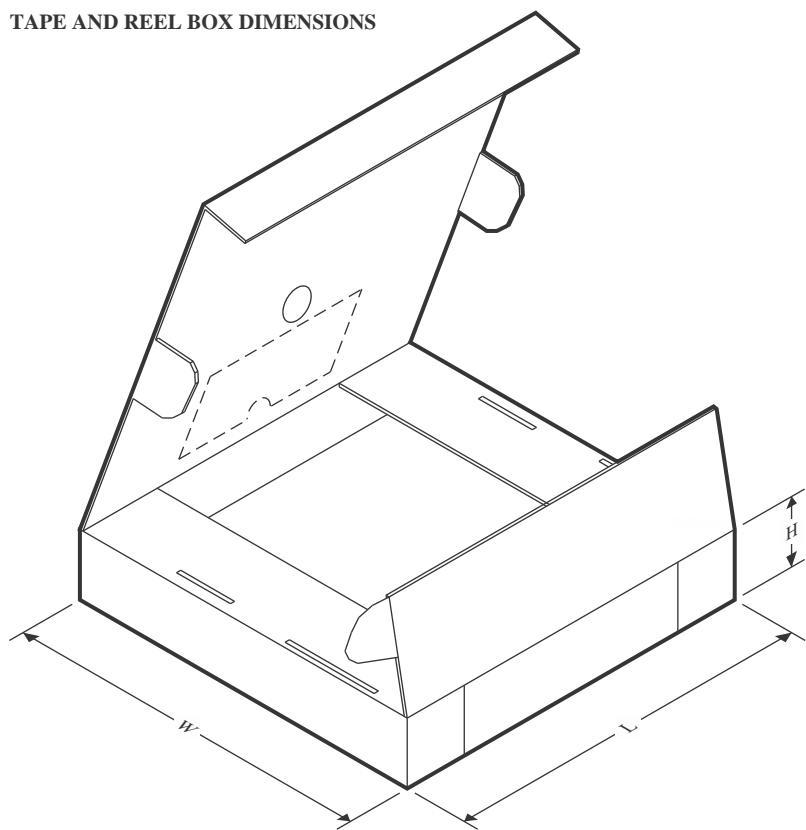
**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVCH16952DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVCH16952DGGR	TSSOP	DGG	56	2000	356.0	356.0	45.0

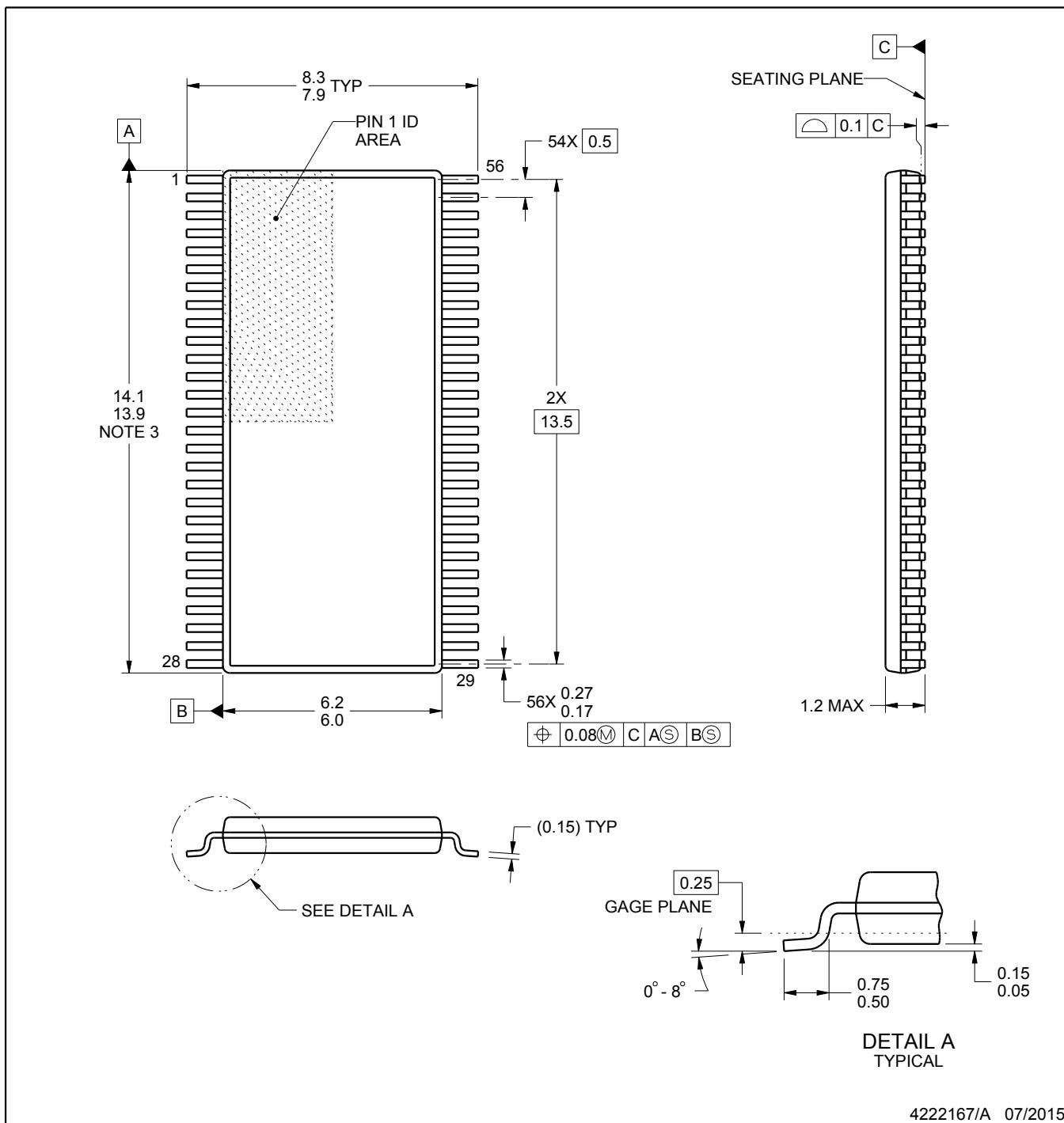
# PACKAGE OUTLINE

DGG0056A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

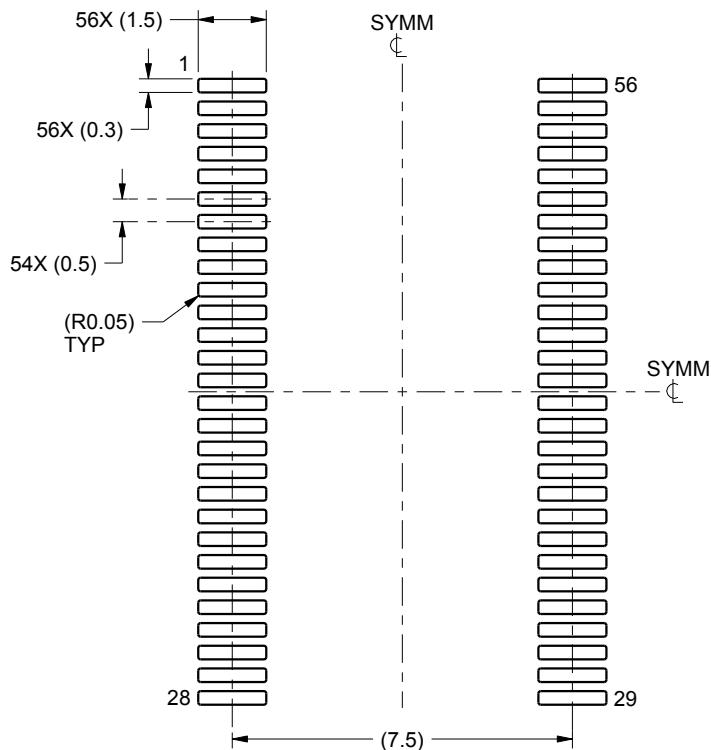
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

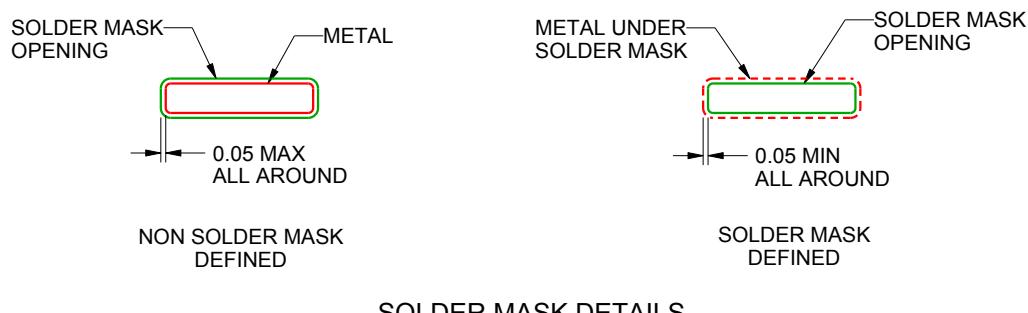
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

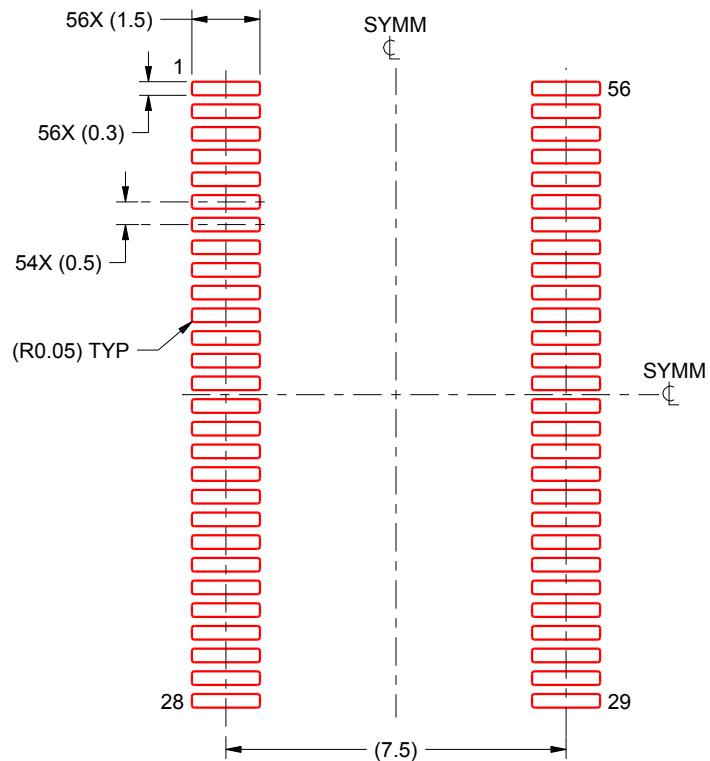
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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