

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ max}$	$I_D \text{ max}$ $T_A = +25^\circ\text{C}$
30V	73m Ω @ $V_{GS} = 10\text{V}$	3.3A
	110m Ω @ $V_{GS} = 4.5\text{V}$	2.7A

Description and Applications

This MOSFET has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- General Purpose Interfacing Switch
- Power Management Functions
- Boost Application
- Analog Switch

Features and Benefits

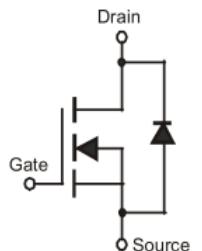
- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- Halogen and Antimony Free. "Green" Device (Note 3)**
- Qualified to AEC-Q101 standards for High Reliability**

Mechanical Data

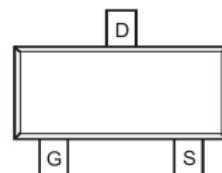
- Case: SOT-23
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See diagram
- Terminals: Finish — NiPdAu over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Weight: 0.027 grams (approximate)



TOP VIEW



Internal Schematic



TOP VIEW

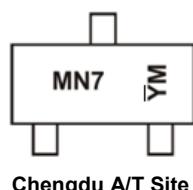
Ordering Information (Note 4)

Part Number	Case	Packaging
DMN3110S-7	SOT-23	3000/Tape & Reel

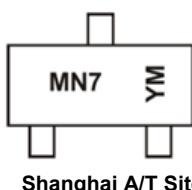
Notes:

- No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- For packaging details, go to our website at <http://www.diodes.com/products/packages.html>

Marking Information



Chengdu A/T Site



Shanghai A/T Site

MN7 = Product Type Marking Code

YM = Date Code Marking for SAT (Shanghai Assembly/ Test site)

YM = Date Code Marking for CAT (Chengdu Assembly/ Test site)

Y or YM = Year (ex: A = 2013)

M = Month (ex: 9 = September)

Date Code Key

Year	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	
Code	U	V	W	X	Y	Z	A	B	C	D	E	
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	30	V
Gate-Source Voltage			V_{GSS}	± 20	V
Continuous Drain Current (Note 5) $V_{GS} = 10\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	2.5 2.0	A
Continuous Drain Current (Note 6) $V_{GS} = 10\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	3.3 2.7	A
Continuous Drain Current (Note 6) $V_{GS} = 10\text{V}$	$t \leq 10\text{sec}$	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	3.8 3.1	A
Continuous Drain Current (Note 6) $V_{GS} = 4.5\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	2.7 2.1	A
Pulsed Drain Current (Note 7)			I_{DM}	25	A

 Thermal Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

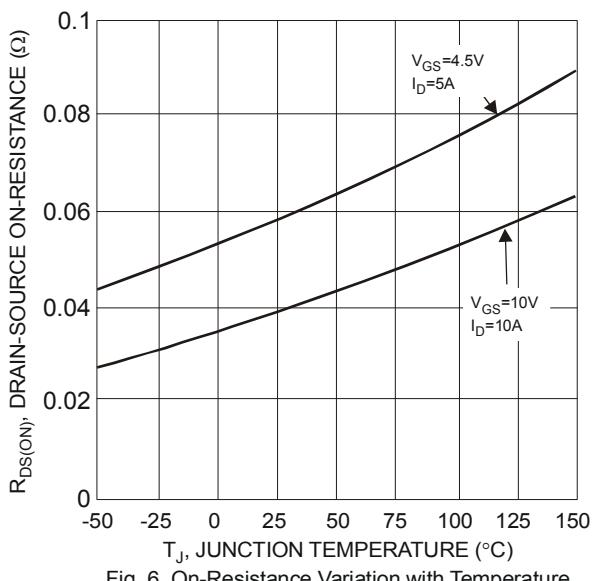
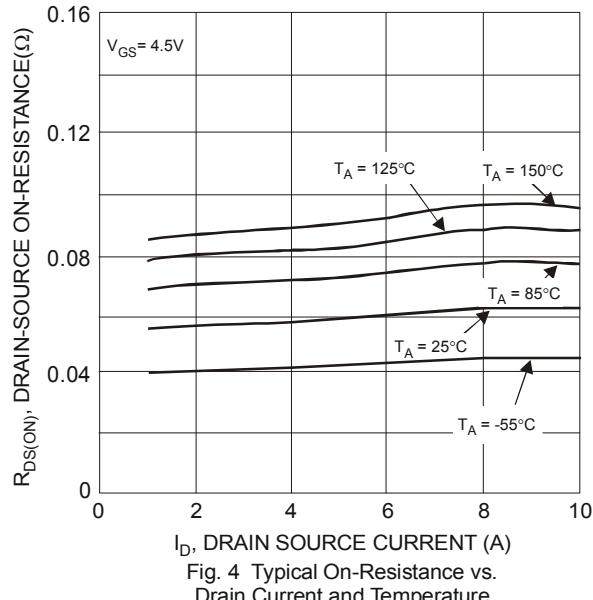
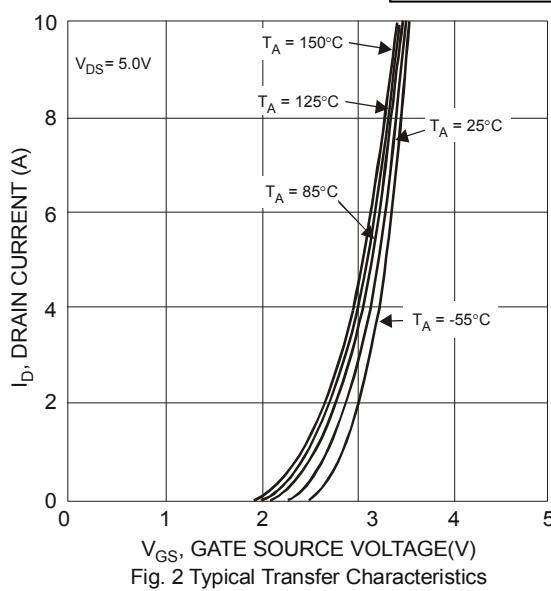
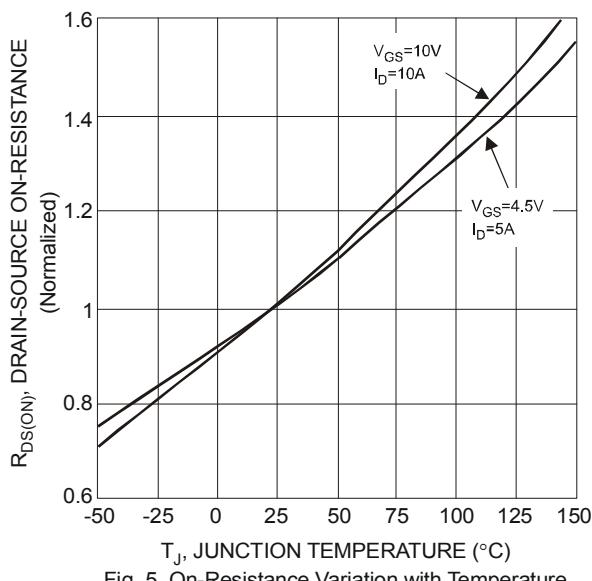
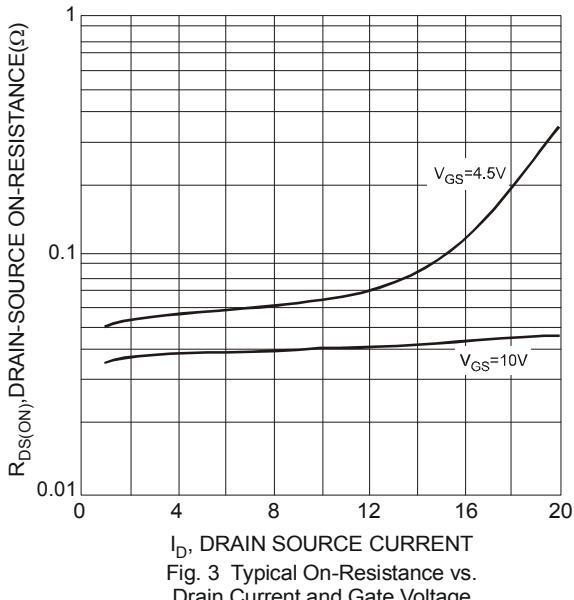
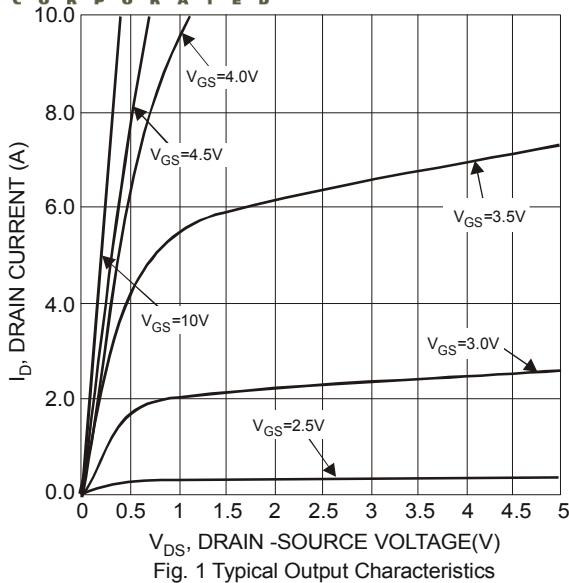
Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	P_D	0.74	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	173.4	°C/W
Total Power Dissipation (Note 6)	P_D	1.3	W
Thermal Resistance, Junction to Ambient (Note 6)	$R_{\theta JA}$	99.1	°C/W
Total Power Dissipation (Note 6) $t \leq 10\text{sec}$	P_D	1.8	W
Thermal Resistance, Junction to Ambient (Note 6) $t \leq 10\text{sec}$	$R_{\theta JA}$	72	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

 Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	-	-	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current @ $T_C = +25^\circ\text{C}$	I_{DSS}	-	-	1.0	μA	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	-	-	± 100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(th)}$	1.0	-	3.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(\text{ON})}$	-	54	73	$\text{m}\Omega$	$V_{GS} = 10\text{V}, I_D = 3.1\text{A}$
		-	88	110		$V_{GS} = 4.5\text{V}, I_D = 2\text{A}$
Forward Transfer Admittance	$ Y_{fs} $	-	4.8	-	mS	$V_{DS} = 10\text{V}, I_D = 3.1\text{A}$
Diode Forward Voltage (Note 6)	V_{SD}	-	0.75	1.0	V	$V_{GS} = 0\text{V}, I_S = 1\text{A}$
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	-	305.8	-	pF	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	-	39.9	-	pF	
Reverse Transfer Capacitance	C_{rss}	-	39.5	-	pF	
Gate Resistance	R_g	-	1.4	-	Ω	
Total Gate Charge ($V_{GS} = 4.5\text{V}$)	Q_g	-	4.1	-	nC	$V_{GS} = 10\text{V}, V_{DS} = 10\text{V}, I_D = 3\text{A}$
Total Gate Charge ($V_{GS} = 10\text{V}$)	Q_g	-	8.6	-	nC	
Gate-Source Charge	Q_{qs}	-	1.2	-	nC	
Gate-Drain Charge	Q_{qd}	-	1.5	-	nC	
Turn-On Delay Time	$t_{D(on)}$	-	2.6	-	ns	$V_{DD} = 15\text{V}, V_{GS} = 10\text{V}, R_L = 47\Omega, R_G = 3\Omega,$
Turn-On Rise Time	t_r	-	4.6	-	ns	
Turn-Off Delay Time	$t_{D(off)}$	-	13.1	-	ns	
Turn-Off Fall Time	t_f	-	2.5	-	ns	

Notes:

5. Device mounted on FR-4 PCB, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, on 1inch square copper plate
7. Device mounted on minimum recommended pad layout test board, 10 μs pulse duty cycle = 1%
8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to product testing.



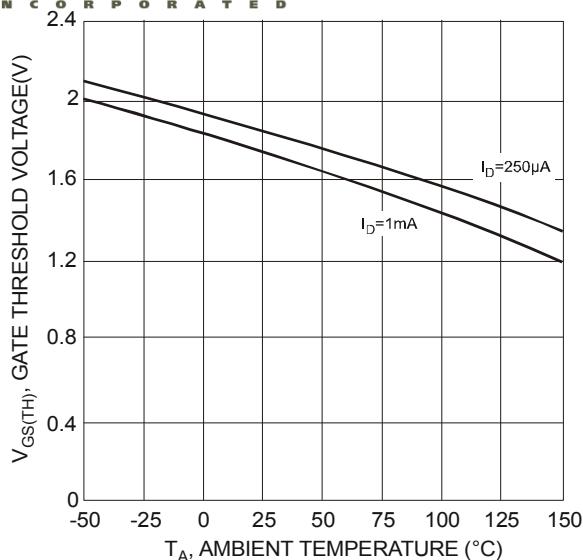


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

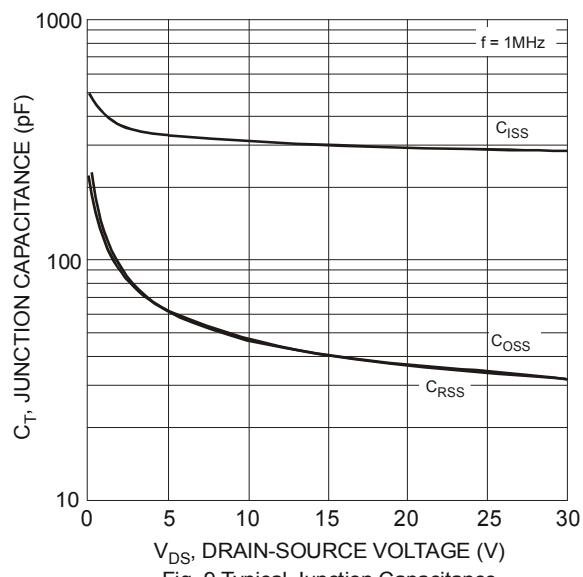


Fig. 9 Typical Junction Capacitance

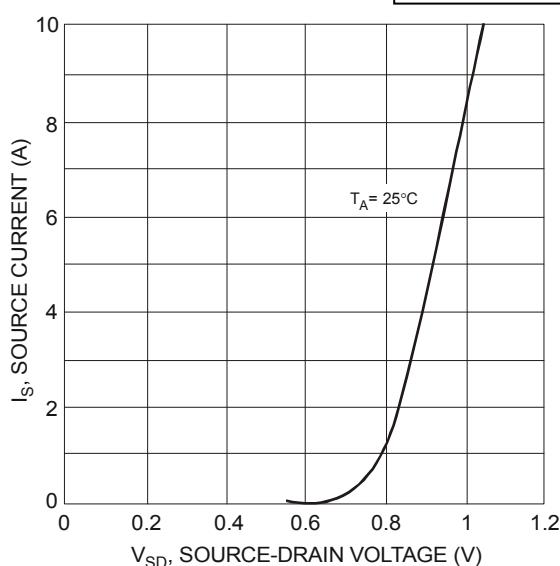


Fig. 8 Diode Forward Voltage vs. Current

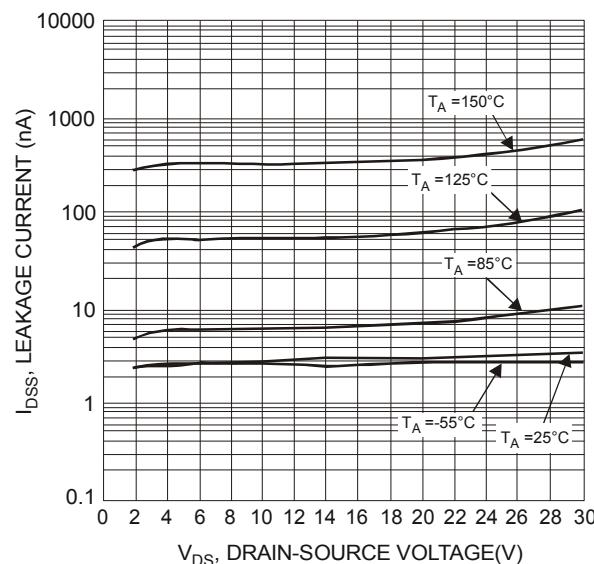


Fig. 10 Typical Drain-Source Leakage Current vs. Voltage

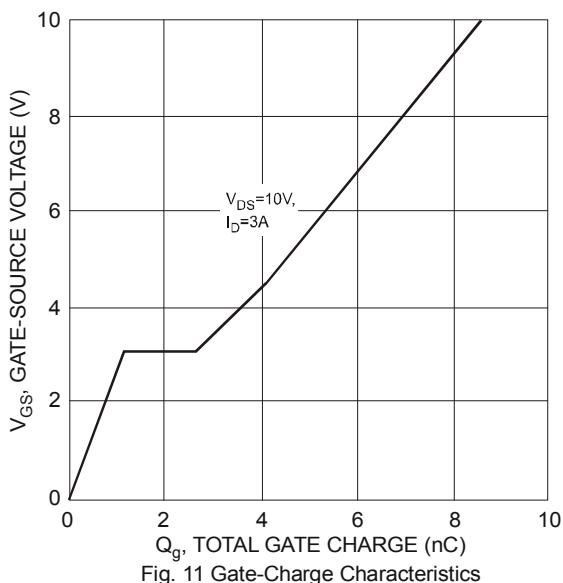
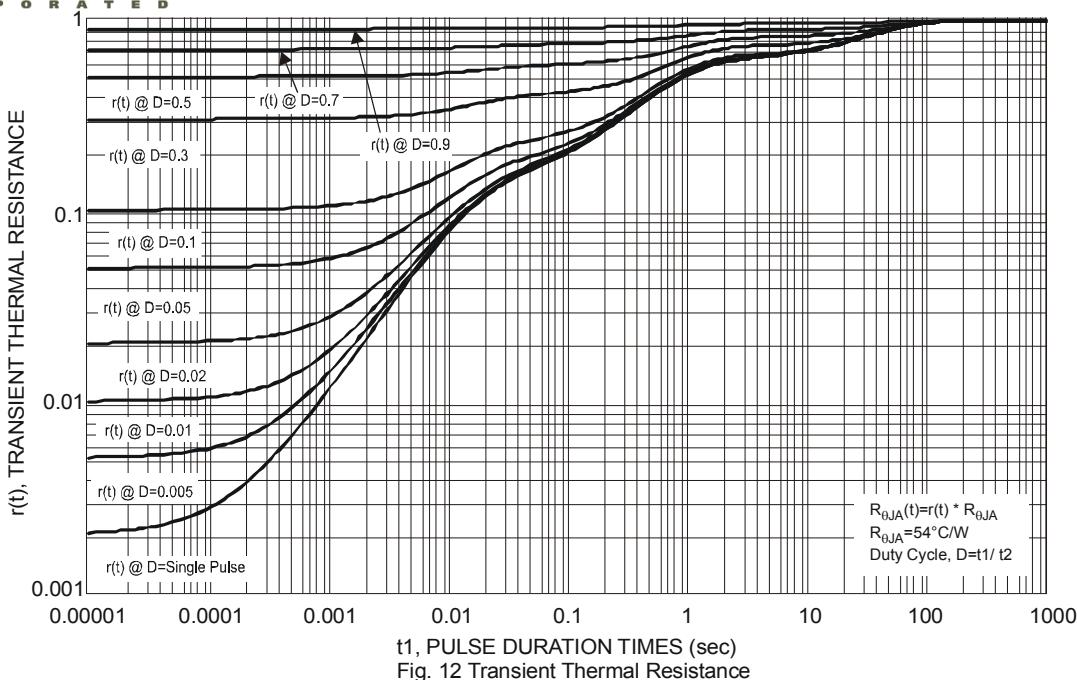


Fig. 11 Gate-Charge Characteristics

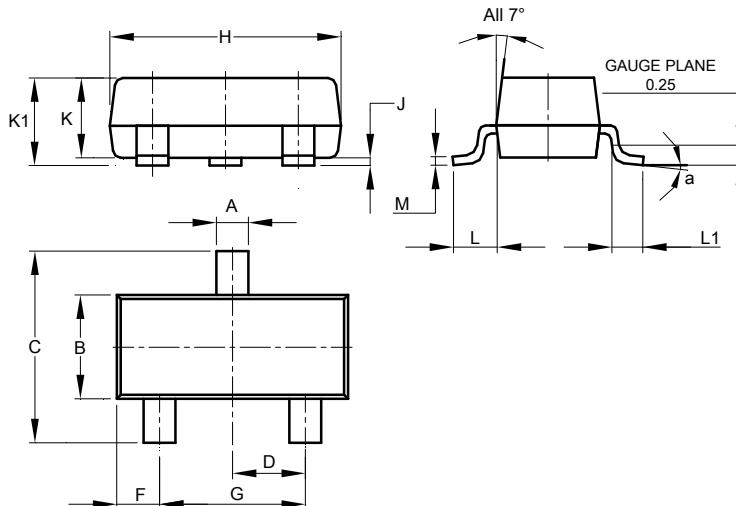


t₁, PULSE DURATION TIMES (sec)

Fig. 12 Transient Thermal Resistance

Package Outline Dimensions

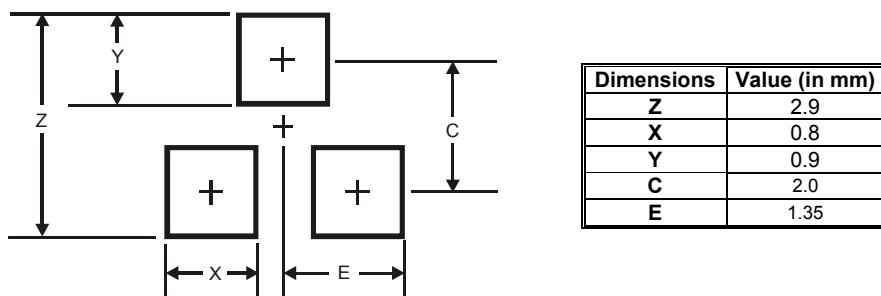
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



SOT23			
Dim	Min	Max	Typ
A	0.37	0.51	0.40
B	1.20	1.40	1.30
C	2.30	2.50	2.40
D	0.89	1.03	0.915
F	0.45	0.60	0.535
G	1.78	2.05	1.83
H	2.80	3.00	2.90
J	0.013	0.10	0.05
K	0.890	1.00	0.975
K1	0.903	1.10	1.025
L	0.45	0.61	0.55
L1	0.25	0.55	0.40
M	0.085	0.150	0.110
α	8°		
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



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