D2-4 Family Audio DSP

Intelligent Digital Amplifier PWM Controller and Audio Processor

FN6782
Rev.2.00
Mar 19, 2019

The D2-4 family (D2-2/D2-3 and D2-4/D2-5/D2-6/D2-6A/D2-6R) devices are complete System-on-Chip (SoC) Audio Processor and Class-D Amplifier Controllers that offer a powerful yet very cost-effective solution for a wide range of consumer audio products, including digital TV systems, PC/multimedia speakers, and portable device docking stations. This 4th generation Digital Audio Processor (DAP) family device combines extensive integrated DSP processing and proprietary audio signal processing algorithms for complete audio system control.

The D2-4 family devices offer the optimum balance of functionality and board-system-material cost, especially in an SoC system architecture with PA audio output. All audio processing and amplifier control is handled by the D2-4 family, and its ease of integration to the existing system processor handles all system control functions.

Related Literature

For a full list of related documents, visit our website:

- D2-4/D2-5 and D2-2/D2-3 device pages

Features

- 48 digital class-D amplifier controller with integrated Digital Signal Processor (DSP)
- Fully programmable audio signal path parameters
- Up to 3 channels of Digital Signal Processing (DSP)
- Includes equalizers, filters, mixers, and other common audio processing blocks
- Audio enhancement algorithms included
- 7.1 sound by PDM™ digital audio stereo inputs
- PC/host control port
- Integrated power-supply-side converters, sample rates from 32kHz up to 192kHz
- Supports 2.0, 2.1, or bramp amplifier outputs with discrete or integrated power stages

Applications

- PC multimedia speakers
- Digital TV audio systems
- Portable device docking stations
- Powered speaker systems


PWM
PWM
PWM

Table of Contents

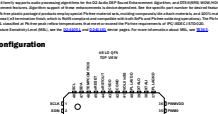
Ordering Information

PART NUMBER (Note 1, 2)	PART MARKING (Note 3)	PART DESCRIPTION	TEMP RANGE (°C)	TAPE & REEL (Units)	PACKAGE (RoHS Compliant)	PKG. DWG. #
D2-AD-DIO-LP	D2 Audio DSP Board Enhancement Algorithm	D2 Audio DSP Board Enhancement Algorithm	-40 to +85	-	48 ld QFN	L48.7x7
D2-AD-DIO-LP-TR	D2 Audio DSP Board Enhancement Algorithm	D2 Audio DSP Board Enhancement Algorithm	-40 to +85	2k	48 ld QFN	L48.7x7
D2-AD-DIO-LP	D2 Audio DSP Board Enhancement Algorithm STEREO/MONO WING KIT	D2 Audio DSP Board Enhancement Algorithm STEREO/MONO WING KIT	-40 to +85	-	48 ld QFN	L48.7x7
D2-AD-DIO-LP-TR (Note 2)	D2 Audio DSP Board Enhancement Algorithm STEREO/MONO WING KIT	D2 Audio DSP Board Enhancement Algorithm STEREO/MONO WING KIT	-40 to +85	2k	48 ld QFN	L48.7x7

NOTES:

1. See "Notes" for details about reel specifications.
2. These D2-Family supports audio processing algorithms for the D2 Audio DSP Board Enhancement Algorithm, and STEREO/MONO WING KIT audio enhancement features. Algorithm support of these enhancements is device-dependent. See the specific part number for desired feature support.
3. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). The Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020b.
4. For Moisture Sensitivity Level (MSL), see the D2-Family Device Selection Guide page. For more information about MSL, see TB363.

Pin Configuration



D2-4 Family Pin Descriptions

PIN	PIN NAME (Pin Number)	TYPE	TOLERANCE (5V, 3.3V, 2.5V, 1.8V)	DRIVE STRENGTH (mA)	DESCRIPTION
1	SCLK	I	3.3		PCM serial audio bit clock (SCLK) Input. Input bus hysteresis.
2	SDOUT	O	3.3		PCM serial audio data (SDO) Output. Input bus hysteresis.
3	LRCK	I	3.3		PCM serial audio left/right (LRCK) Input. Input bus hysteresis.
4	MCLK	I	3.3		PCM serial audio master clock output for external (MC-DAC) components, slave. Low net. Output is as driven. Bus hysteresis.
5, 42	CVDD	P	3.3		Core power. 1.8 (Typ.). Used for ultra-low-power DSP logic, and interfaces.
6, 42	CGND	P	0.0		Core ground
7, 40	RVDD	P	3.3		Digital analog ring. Internally connected to PWRDGND.
8, 39	RGND	P	0.0		Digital analog ring power. 3.3V. The 3.3V supply is used for all the digital I/O pad drivers and receivers, except for the analog pads. Both are required to be connected. Internally connected to PWRDGND.
9	TEMPMON/ SDA	I/O	3.3	4/8	Temperature monitor input. Bidirectional open drain/Input/Output. Bidirectional/Input/Output. Bidirectional open drain. Open-drain/Input/Output. Open-drain/Input/Output. Open-drain/Input/Output

D2-4 Family Pin Descriptions (Continued)

Pin	Pin Name (Notes 1, 2)	Type	Voltage Level (V)	Pull Type	Description
23	PWDN2	I	3.3	N/A	PWM protection input. Input to the powerness Protection monitoring functionality of these pins is controlled by an internal D2-4 family firmware, and dependent on which of the four amplifier configurations is enabled.
24	PWDN3	I/O	3.3	4	PWM output pin ground. Internally connected to PGND.
25	PWM7	I/O	3.3	8mA	PWM outputs. Output is 8mA or 24mA, depending on the output mode configuration setting. Pins float on reset.
26	PWM6	I/O	3.3	8mA	
27	PWM5	I/O	3.3	8mA	
28	PWM4	I/O	3.3	8mA	
29, 30	PWM1/2/3	P	3.3	N/A	PWM output pin power. This 3.3V supply is used for the PWM pad drivers. Internally connected to PVDD.
31	PWM3	I/O	3.3	8mA	PWM outputs. Output is 8mA or 24mA, depending on the output mode configuration setting. Pins float on reset.
32	PWM2	I/O	3.3	8mA	
33	PWM1	I/O	3.3	8mA	
34	PWM0	I/O	3.3	8mA	
37	PLLGND	P	1.8		PLL analog ground
38	XTAL1	P	1.8		Crystal oscillator analog input pin
39	XTAL2	O	1.8		Crystal oscillator analog output pin. This output drives the crystal and STALO state, not have a drive strength specification.
40	PLLVDD	P	1.8		PLL analog power
41	VDLC/ nSI	I/O	3.3	4	Volume control pulse input and SPI slave select. At demodulation of device reset, this pin operates as a SPI slave select input. Upon internal D2-4 family firmware execution, this pin becomes an input for monitoring up/down pulse pulses from volume control device (see volume control pin). Active low output. This pin drives low from the 3.3V transceiver detector or 1.8V transceiver detector when the 3.3V or 1.8V transceiver is active to indicate a system must be in the HIBERNATE power down mode (see Hibernate). Active low input. Internally pulled up. Used as an input to the 1.8V transceiver detector and as a system wake-up input. Pin can optionally be configured as a GPIO input. Equivalent to the wake-up function on the IRQ input pins, on the rising edge.
42	TEMPSOM/ nSOM	I/O	3.3	3.3	Temperature monitor comment (3.3 pin)
47	SDA	I/O	3.3	8 -20	Two-wire serial data, open-drain pin with Schmitt-trigger input. Bidirectional data line used by both the master and slave operations for data transport. Pin floats on reset.
48	SCL	I/O	3.3	8 -20	Two-wire serial clock pad, open-drain driver with Schmitt-drive strength. Bidirectional signal used by both the master and slave controllers for clock signaling. Pin floats on reset.

NOTES:

1. All pins are in tri-state or high, unless otherwise specified. Pins that are active low are "n" prefix, such as nRESET.
2. I/O means the pad has an open-drain driver.
3. All power and ground pins of the same name are must be tied together to all other pins of that same name (for example, for the PVDD pins together, PGND pin together, GGND pin together, CGND pin together, PWMGND pins together, and PWMGND pins together).

Absolute Maximum Ratings (Note 20)

Supply Voltage	
PVDD, PVSS	-0.3 to +4.6V
AVDD, AVSS	-0.3 to +4.6V
Input Voltage	
Any Input but 5.5VIn	-0.3V to PVDD + 0.3V
5.5VIn	-0.3V to PVDD + 0.3V
Input Current, any Pin but Supplies	±10mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W) θ_{JC} (°C/W)
36 Ball WLCSP (Note 4)	27 27
Storage Temperature Range	-65°C to +150°C
Maximum Storage Temperature	150°C to +150°C
Pb-Free Reflow Profile	see TB493

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See TB379.
5. Pin θ_{JC} the "case-to-pin" thermal resistance of the exposed metal pad on the package underside.
10. Absolute Maximum parameters are not tested in production.

Recommended Operating Conditions

T_A = -20°C (OSS = PLLOSS) = 1.8V (xIn, RXDD = PWRXDD) = 3.3V (xIn, All grounds at 0.0V, All voltages referenced to ground. PVDD = 2.5V±0.25V(Note 1) (±0.125V(Note, were running at 1.8V ±100mV with optical audio data traffic.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Core Supply Pins	VDDD	1.7	1.8	1.9	V
Active Current		-	500	-	mA
Power-Down Current (Note 2,3)		-	1	-	mA
Digital I/O and PWM Pad Ring Supply Pins	PVDD and PWRXDD	3.0	3.3	3.6	V
Active Current		-	50	-	mA
Power-Down Current (Note 2,3)		-	0.05	-	mA
Analog Supply Pins (Pin)	PLLDDD	1.7	1.8	1.9	V
Active Current		-	30	-	mA
Power-Down Current (Note 2,3)		-	4	-	mA

NOTE:

1. Power-Down is with device in reset and clocks stopped.

Electrical Specifications

T_A = -20°C, OSS = PLLOSS = 1.8V, xIn, RXDD = PWRXDD = 3.3 ±10%, All grounds at 0.0V, All voltages referenced to ground. PVDD = 2.5V±0.25V(Note 1) (±0.125V(Note, were running at 1.8V ±100mV with optical audio data traffic.

PARAMETER	SYMBOL	PIN	MIN	TYP	MAX	UNIT
Digital Input High Logic Level (Note 20)						
Digital Input Low Logic Level (Note 20)					0.8	V
Digital Input Low Logic Level (Note 20) V_{DD} = Pad Driver	V_{IH}	PWRD 0.4				V
Low Level Input Driver Voltage (Note 20) V_{DD} = Pad Driver	V_{IL}				0.4	V
High Level Input Driver Voltage (Note 20)	V_{IH}	0.7			PLLDDD	V
Low Level Input Driver Voltage (Note 20)	V_{IL}				0.3	V
Input Leakage Current (Note 20)	I_{IN}				±10	µA
Input Capacitance	C_{IN}			5		pF
Output Capacitance	C_{OUT}			5		pF
WRDET Pulse Width	T_{WD}			30		ns

Electrical Specifications T_a = +25°C, DVDD = PLLVDD = 1.8V ±5%, RVDD = PAVRVDD = 3.3V ±5%, all grounds at 0V, 50 voltages measured to ground, PLL at 24.576 MHz, PLL at 22.5896 MHz unless noting all LED DRIVING voltages with a resistor to VDD

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
GENERAL CHARACTERISTICS					
Crystal Frequency (Fundamental Mode Crystal)	fx	20	24.576	25	MHz
Duty Cycle	Dx	40	-	60	%
Rise/Up Time (Rise/Up Time to Oscillation stabilized (with Wait Supply) or Stable Oscillation)	Tx	-	-	20	ms
PLL					
VCO Frequency	Fvco	240	294.912	300	MHz
PLL Lock Time from set-input Divisor	Tpll	-	-	2	ms
I/O POWER CHARACTERISTICS					
Reset Enabled Voltage Level	Vlen	0.95	1.10	1.30	V
PDM Minimum Output Pulse Width	Tdlx	-	8	-	ns
I/O CHARACTERISTICS					
Schmitt Level		1.4	1.6	1.7	V
Pulse Width Rejection	Tfswl1	-	100	-	ns
Minimum Output Pulse Width	Tx3	-	20	-	ns
I2C DATA/CLOCK CHARACTERISTICS					
Schmitt Level		2.4	2.7	2.9	V
Pulse Width Rejection	Tfswl2	-	100	-	ns
Minimum Output Pulse Width	Tx3	-	20	-	ns

NOTES:
1.1. All input pins except XTI2.
1.2. All output output pins. Since strength for each digital pin is in the "D2-4 Family Pin Descriptions" on page 3.
1.4. Input leakage applies to all pins except XTI2/x3.

Serial Audio Interface Port Timing T_a = +25 °C, DVDD = PLLVDD = 1.8V ±5%, RVDD = PAVRVDD = 3.3V ±5%, CL = 25pF 100kHz, MSB Justified, Fs = 48 (Fsample as 256, 512 and higher ratio exceeds the given specification)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
SCLK Frequency (SCLK)	$1/t_{SCLK}$	-	-	12.5	MHz
SCLK Pulse Width (HIGH and LOW) (SCLK)	t_{SCLKH}	40	-	-	ns
LRCKR Set-Up to SCLK Rising (LRCK)	t_{LRCKS}	20	-	-	ns
LRCKR Hold from SCLK Rising (LRCK)	t_{LRCKH}	20	-	-	ns
SDIN Set-Up to SCLK Rising (SDIN)	t_{SDI}	20	-	-	ns
SDIN Hold from SCLK Rising (SDIN)	t_{SDIH}	20	-	-	ns

FIGURE 2. SERIAL AUDIO INTERFACE PORT TIMING

Two-Wire (I^2C) Interface Port Timing V_{DD} = 2.6V (C_0000 = PLL000 = 1.8V ±5%, RIO0 = PWIN000 = 3.3V ±10%, All grounds at 0.0V, All voltages referenced to ground)

DESCRIPTION	SYMBOL	MIN	TYP	MAX	UNIT
SCL Frequency	f_{SCL}			100	kHz
Bus Free Time Between Transmissions	t_{BUF}	4.7			µs
SCL Clock Low	t_{LOW},$t_{SCL1,4}$	4.7			µs
SCL Clock High	t_{HIGH},$t_{SCL1,4}$	4.0			µs
Start Or Repeat Start Setup Time	$t_{SU;STA}$	4.7			µs
Start Condition Hold Time	$t_{HD;STA}$	4.0			µs
SDA Hold Time SCL Falling (See Note 19)	$t_{HD;DAT}$			3	ns/nS
SDA Setup Time to SCL Rising	$t_{SU;DAT}$	250			ns
SDA Output Delay Time From SCL Falling	$t_{SDA1,4}$			0.9	µs
Rise Time of Both SDA and SCL Bus (See Note 18)	t_r			1	µs
Fall Time of Both SDA and SCL Bus (See Note 18)	t_f			300	ns
Start Or Stop Condition	$t_{SU;STO}$	4.7			µs

NOTES:

18. Data is clocked in on valid rise edge SCL1,4 rising edge after SCL goes low.
19. Limits established by characterization and not production tested.

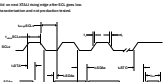


FIGURE 3. I^2C INTERFACE TIMING

SPI™ Master Mode Interface Port Timing T_A = -20°C, DGND = PGND = 1.8V, AVD, RVDD = PMRVDD = 3.3V ±5%, all grounds at 0.0V, all voltages referenced to ground.

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_{CYC}	MOSI Serial Port Clock Step	8	∞	ns
t_{SU}	MISO Setup to Clock Edge	1.0		ns
t_{HD}	MISO Hold from Clock Edge			
t_{SS}	nSS Minimum Width	2 system clocks + 2ns		

SPI™ Slave Mode Interface Port Timing T_A = -20°C, DGND = PGND = 1.8V ±5%, RVDD = PMRVDD = 3.3V ±5%, all grounds at 0.0V, all voltages referenced to ground.

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_{CYC}	MOSI Serial Port Clock Step	2 system clocks + 2ns		
t_{SU}	MOSI Setup to Clock Edge	1.0		ns
t_{HD}	MOSI Hold from Clock Edge			
t_{SS}	nSS Minimum Width	2 system clocks + 2ns		

FIGURE 5. SPI TIMING

Overview

The D2-4 family devices are integrated System-on-Chip (SoC) audio processors and Class D amplifier PWM controllers. They combine a DSP core with peripherals, memory and a Class D complete audio processing, and selectable PWM output options for driving multi-output power stage configurations. Stereo PBTL output, Stereo BTL output, Mono BTL output, and Mono single-ended interface enable integration compatibility with existing system architectures and solutions. The audio path includes a stereo Sample Rate Converter (SRC) plus device-specific audio enhancement processing algorithms.

Output Configurations

A 3-channel PWM engine with applications-selected configuration settings provides output paths for combinations of output channels. Application-dependent configurations include stereo Bridge-Tied Load (BTL) output, Stereo Single-Ended (SE) and Stereo Bridge Single-Ended (BSE), as well as Stereo Line, Headphone Outputs, or Subwoofer Line Outputs. Depending on configuration settings, Half-Bridge, Half-Bridge and Bridge-Tied Load (BTL) output stage topologies, with either discrete or integrated output stages are supported.

Programmable Audio Processing

Programmable parameter settings for audio processing include volume control, path routing and mixing, high/low pass filtering, multiband equalizers, compressors, and loudness. These parameters can be adjusted using the D2 Audio Customization GUI software during design and development, or can be set through the device's control interface within production amplifier products.

Typical Performance

Most system performance is largely determined by the amplifier output stage, power supply, output filter, speaker components, and overall system design. Typical performance capability of amplifier power outputs ranges from less than 20W to systems over 1kW. System audio quality metrics include 20Hz to 20kHz frequency response, SNR of greater than 100dB, and THD+N performance typically below 0.1%.

Audio Enhancement Processing

The D2-4 family devices include D2-Audio DSP Sound Enhancement Technology (SET) such as Dynamic Bass Boost (DBB), DRC, WOW, SPDIF Audio Jitter Reduction (JR) and other enhancement algorithms. These functions are integrated within the firmware of each device and are part of the standard audio signal flow.

Functional Description

Figure Accompanying Text shows a block diagram of the D2-4 family Audio processors as a reference for many of the items in the following descriptions.

Serial Audio Digital Input

The D2-4 family devices include Serial Audio Interface (SAI) port accommodating two channels of digital audio input. The SAI port supports I2S, LJ, RJ, TDM and PCM formats with sample rates up to 192 kHz SPDIF Audio rates. The SAI input port supports in slave mode only. The digital audio input from the SAI input port routes directly through the Sample Rate Converters (SRC). Either TDM/I2S digital input or the S/PDIF digital input can be selected as the audio input source.

S/PDIF Digital Audio I/O

The D2-4 family contains one IEC60958 compliant S/ PDIF Digital receiver input and one IEC60958 compatible S/PDIF Digital transmitter output.

The S/PDIF receiver input includes an input transition detector, PLL, and error detection and correction circuitry for digital audio data. The receiver meets the jitter tolerance specified in IEC60958-4.

The S/PDIF transmitter complies with the consumer applications defined in IEC60958-3. The transmitter supports 24-bit audio data, but does not support user data and channel status.

Compressed digital formats are not decoded within the D2-4 family. However, a bitstream pass-through mode is supported from the SPDIFIN1 input to the SPDIFTX output, which allows for the transmission of Dolby Digital and other formats of compressed audio input bitstream to make available at the product's S/PDIF output.

Sample Rate Converter

The D2-4 family devices include a 2-channel asynchronous Sample Rate Converter (SRC). The SRC converts audio data input sampled at one input sample rate to a fixed 48kHz output sample rate that aligns synchronous input audio streams to a single rate for system processing. With an input sample rate within the SRC lock range, the SRC automatically locks to the clock from either the SAI or S/ PDIF input sources. In addition to converting the input sample rate to the output sample rate, input clock jitter and sampling jitter are attenuated by the SRC.

DSP

A 24-bit fixed point Digital Signal Processor (DSP) controls the audio signal flow and implements system control functions within the D2-4 family devices.

Audio path signal routing, programmable parameter processing blocks, and control logic are defined within the device's internal firmware. Signal flows through the devices are buffered and parameset through interface specific fast-box blocks, such as the SCI.

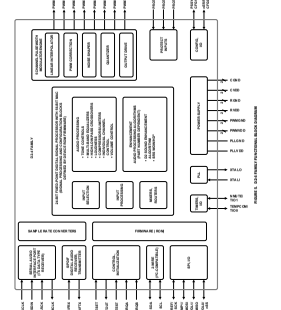
Audio Processing And Signal Flow

The audio processing within the D2-4 family devices is defined by the internal ROM firmware and executed by the DSP. This firmware defines the audio flow architecture and the processing blocks that are available to the application. Figure shows the signal flow for the D2-4 family devices. Standard audio processing has lines within this architecture include:

- Mixers/matrixes
- Routers
- Compressors and limiters
- Tone controls
- Multiband equalizers (fully parametric and shelving)
- Digitrim and fast gain crossover filters
- Volume and level controls
- Loudness compensation
- Input signal selection

Signal flow and total system definition is defined by the internal firmware. Signal processing blocks in programmable, which allows for adjustment of all of the internal parameters.

Signal flow and details of each of these audio processing blocks are shown in Figure 2.


D2-4 FAMILY
DUAL CORE ARM CORTEX-M3 PROCESSOR WITH FLASH AND SRAM MEMORY, DMA, CRC, MPU, DEBUG, TRACE, AND ADVANCED POWER MANAGEMENT
ARM CORTEX-M3 CPU
MPU
DEBUG
TRACE
MEMORY
- 128KB FLASH
- 16KB SRAM
- 2 CYCLE FLASH ACCESS
- 1 CYCLE SRAM ACCESS
- 2 CYCLE FLASH ACCESS WITH PREFETCH
- 1 CYCLE SRAM ACCESS WITH PARITY
- 1 CYCLE FLASH ACCESS WITH PREFETCH
- 1 CYCLE SRAM ACCESS WITH PARITY
- 1 CYCLE FLASH ACCESS WITH PREFETCH
- 1 CYCLE SRAM ACCESS WITH PARITY
- 1 CYCLE FLASH ACCESS WITH PREFETCH
- 1 CYCLE SRAM ACCESS WITH PARITY
MEMORY
- 128KB FLASH
- 16KB SRAM
- 2 CYCLE FLASH ACCESS
- 1 CYCLE SRAM ACCESS
- 2

Audio Enhancement Feature Processing

Additional enhancement audio processing algorithms are available in the D2-4 family of audio processors. The D2-4 family includes the following enhancement algorithms:

- D-Control DSP Sound Enhancement Algorithm (with the D2-4C/D2-4E/D2-4F)
- 3-channel stereo spatialization
- Bass enhancement
- Control configurations 62 presets
- Improved sound clarity
- Automatic volume control, equalization, optimization
- Automatic loudspeaker setup, equalization/correction

STEREOMIX REQUIRES THE D2-4C/D2-4E/D2-4F.

Each of these enhancements are unique to the particular part number, and each enhancement has its own set of programmable parameters to control operation. The location of these enhancements within the signal flow is shown in Figure 1 on page 3.

PWM Audio Outputs

The D2-4 family device incorporates five PWM output channels that are designed for high-fidelity output pins. Each of the PWM channels and their pins are used for driving output power stages, such as Class-D amplifiers, depending on the selected configuration.

The outputs support multiple PWM amplifier output topologies. These supported topologies include full-bridge 16-V to 5-V and full-bridge 16-V to 3V-rail-to-rail 2-level modulation with 2 or 4 equalizer curves. Each channel and pin supports 2 equalizer and eight output pins as well as the dedicated output topology is shown in Figure 2 on page 4 and Figure 3 on page 5. See Section Audio Configuration on page 12 for a detailed pin and section of linear output configurations, and their associated mapping of the PWM outputs.

Using a simple passive filter, the PWM outputs drive linear-level outputs at a nominal $2V_{RMS}$ headphone outputs or linear-level outputs that require a $2V_{RMS}$ or higher output level are implemented using an active filter.

I/O Control Pins

Several device pins are used as specific function inputs and outputs to control amplifier and device operations. Some pins are used as inputs to control the device and other pins are used as outputs to show operating states. Functions of these pins are defined in "D2-4 Family Pin Descriptions" on page 6, and additional descriptions are included in the functional block descriptions elsewhere in this document. These pins are implemented with 5-V tolerant bidirectional I/O buffers with pull-ups. These, however, have ground, as not programmable, and the specific function is defined by the D2-4 family internal firmware.

Timers

Two independent timers are used for device and system control. Timer 0 is used for the watchdog timer function. Timer 1 is used for the temperature sensing control. Two I/O pins are associated with the timers, and their pin functions are defined by the device firmware. Timer 0 is used for the temperature sensing and temperature monitoring algorithm. Its pin (TEXO) is used as an output to control the temperature sensing circuitry. Timer 1 is used for internal functions of the device. Its pin (TEXI) is not used for this timing operation, and is defined by device firmware as the nRESET I/O pin. Timer operation is established internally by firmware and, not programmable.

I²C-Write Control Interface

The D2-4 family devices include a 2-Wire I²C compatible interface for communication with an external controller.

This interface is usable with either an external microcontroller interface, or an communication EEPROM, or other compatible peripheral chips. The I²C interface is multimaster capable, supports standard and fast mode operation, and supports serial read and write operations.

Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) is an alternate serial input port for communication with an external microcontroller, or an communication EEPROM or other compatible peripheral chips.

The four SPI interface pins are all shared. This interface functions only as an input port for external serial communication, not operate as an interactive control port. During a reset condition, the latching of the strapping pins, five pins (SDA/MOSI, SCL/TEMP2, MISO/A0, SS/A1, and CS/A2) sample as the SPI port. The SPI port is not operational during reset, and the strapping pins sampling for firmware program. These pins are no longer used for SPI functions, and operate as assigned by the firmware.

Control Register Summary

The control register interface is used for an external controller to adjust the amplifier's programmable settings and adjustments. The control register interface is implemented in the digital processing blocks are accessed through a register programming interface, and each parameter is defined with its specific register address and bit-field. The I²C, signal or SPI register read and write operations, PWM amplifier modulation and fault outputs, and S-PDIF interaction, are controlled through the control registers.

All of these control register functions are defined in the Application Programming Interface (API) specification.

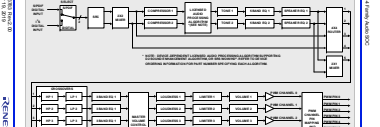


FIGURE 6. 59-2 Family AUDIO DSEN BLF FLOW

Temperature Sensing

The temperature sensing algorithm uses external hardware on the board to measure the temperature of the board. The external hardware includes a Negative Temperature Coefficient (NTC) resistor located physically on the design in areas that require monitoring.

This operation uses three of the I/O pins (TSENPRST, SCSI, TSENP), TSENS, and TSENPCONTROL. These pins have shared functions. Each pin has a multiplexer. These pins operate as part of the multiplexer. The multiplexer is controlled by the software. All functionality (turn off and turn on) of these pins are dedicated to the temperature monitoring function.

Overcurrent Protection

The device operates in conjunction with current limitation detection connected to the power supply, used at each power stage output of the amplifier design.

This detection circuit is to generate a pulse or logic level upon detection of high current, where this logic level is connected to one of the three protection inputs (PWPROTECT[0:2]).

These protection input pins are optional (intended for protecting the PWM power transistors). They are active-low and have a pull-up weak level drive on the pins. Firmware within the D2-4 family devices can monitor these inputs and can use the PWM hardware functions to disable the PWM output pins, depending on the conditions mentioned on these protection input pins.

The number of overcurrent protection is a design-dependent on which one of the four configurations is defined. The configuration settings, established during power-on reset through the configuration pins, also determine which protection inputs are used.

Power Supply Synchronization

The PWSYNC CFG1 pin provides a power-supply synchronization signal for switching power stages. Firmware uploading this pin to the frequency and duty cycle needed by the system switching power stage. The synchronization signal is used to synchronize the switch the device's internal power switching frequency to avoid interference signals that could occur if the switching power supply is not locked to the internal switching frequency.

This PWSYNC CFG1 pin is a shared pin. During device reset and initialization, the pin is used as one of two configuration strapping pins, where its high or low logic state is used to set the amplifier output mode. After the initial initialization of reset and the device firmware begins operating, this pin becomes the PWSYNC output.

Error Pin

The amplifier error internal overcurrent (ovc or O) pin (OVERRCURRENT), is an output to signal a detected shutdown and sensitive to an external system controller. This output can be used to turn on a cooling fan or alarm.

The error output is also used to signal an external microcontroller that the PCM is in sleep. The error output is used in some low-cost system installations, the PCM is busy as a monitor device.

The error output is also used to signal a system reset, as an output after the device firmware initializes and begins running. This same pin is shared on an input. During a reset condition, this pin operates as an input and is used as a strapping pin that are used to define the configuration mode. A vector pull-up or pull-down on this pin establishes the configuration mode of operation. After the initialization sequence completes, these resistors do not affect the error output operation.

Power Sequencing

The D2SS and D2SS including PWRSEQ power supplies should be brought up together to avoid high current transients that could damage the power supplies. The power supplies can be brought up separately. The best practice is for all supplies to feed from regulators using a common power source. Typically this can be achieved by using a single 5V power source and regulating the 3.3V and 2.8V supplies from that 5V source. As noted in Note 2 of the Pin Table, these notes must be held higher at 3V operation.

Clock and PLL

The clock is generated one frequency a fundamental-mode crystal connected between XTAL1 and XTAL2 pins. The PLL multiplier output is a designated frequency. Other clocks are derived directly by any other circuit. XTAL2 is an input that connects to the other side of the crystal.

The clock generation contains a low jitter PLL critical for low noise PWM output and low noise ADC operation. Firmware controls clock rate conversion and the audio processing data paths. The clock generation provides the clock for the PWM and ADC modules, the processor core, the DMA controller, the Serial Communication Port (SCP) transceiver, and the PWM engine.

Clock and PLL Operation is controlled by the internal clock-or firmware. They are not programmable and are optimized for device and system operation.

Reset and Device Initialization

The D2-4 family devices, must be reset to initialize and begin operation. Reset can be initiated by a hardware reset signal (pin) or by the ARSTSFTWARE bit. Extend hardware reset or a condition within the amplifier system design must provide this reset signal to the device. The reset signal must be held low for a minimum duration. Some hardware designs offer the ARSTSFT pin is released from its low-state idle.

The chip contains power-on detectors and brownout detectors for the 3.3V and 1.8V power supplies. A loss or drop of power from either of these power supplies triggers these brownout detectors. The asserts the ARSTSFT pin, drop it low. Connect the ARSTSFT pin to the hardware reset signal. Firmware can also monitor these and ensure a proper reset occurs if the power supply voltage drops below their designed specifications.

At the deassertion of ARSTSFT, the chip reads the status of the boot mode selection pins (PBQA and PBQB) and begins the boot process, determining if the boot mode is defined by these pins/ logic state. These device pins are strapped either high or low to define the boot mode. The boot mode can also be defined by the state of the boot mode selection bits. See "Boot Mode" on page 53 section for related descriptions.

Boot Modes

The D2-4 family devices contain internal firmware to operate the DSP, PWM, and other peripherals. Firmware is loaded into memory by the programmable serial port, can be written to the device after it is operational and running. Parameter data can be revised later, which allows customer-specific firmware settings to be used in processing. The device is designed to load in one of four possible modes. Firmware and parameter data to be provided from three boot sources.

- I^2C slave (to external microcontroller)
- I^2C EEPROM
- Internal device ROM only
- SPI slave

The specific boot mode is selected based on the state of the IRQ0/and IRQ1 input pins at the time of reset de-assertion. Boot modes are shown in Table 2.

TABLE 2. BOOT OPTIONS

BOOT MODE	IRQ0 PIN	IRQ1 PIN	SOURCE	DESCRIPTION
0	0	0	I^2C Slave	Operates as I^2C slave, boot at address 0x60. An external Master I^2C controller provides boot data.
1	0	1	I^2C Master	Operates as I^2C Master, boot from external EEPROM. Boot data is located under boot ROM, set to I^2C port.
2	1	0	Internal ROM	Boot from ROM. Boot configuration
3	1	1	SPI Slave	SPI slave. External SPI master provides boot code.

The device initializes on all three of its boot mode. However, it gets its configuration and parameter data from the boot device. The boot device can be an external microcontroller, an I^2C EEPROM, if a system uses both an external controller and an EEPROM, the EEPROM loads first. During this time, the controller must remain off the I^2C bus.

Output Mode Configurations

The D2-4 family devices support four amplifier output configuration modes of powered output and line output combinations. These four modes are shown in Table 3.

TABLE 3. DEVICE OUTPUT CONFIGURATION MODES

MODE	PWM OUTPUTS	DESCRIPTION
0	2.0L/R Powered	Powered Left and Right Speakers with 2-channel Line Outputs. Full Bridge Drive.
1	2.0L/R Powered	Powered Left and Right Speakers with 2-channel Line Outputs. Half Bridge Drive.
2	2.1L/R Sub L/R Out	Powered Left and Right Speakers with 2-channel Line Outputs. Single-Ended Stereo Left + Right Line-Level Subwoofer. Dual Ended Subwoofer Line-Level Output
3	2.2L/R L/R Out	Powered Left and Right Speakers, with 2-channel Line Outputs. Full Bridge Drive. Single-Ended Stereo Left + Right Line-Level Subwoofer. Crossover Filtering Added to Signal Flow.
3	2.2L/R Sub L/R Out	Powered Left and Right Speakers with 2-channel Line Outputs. Crossover Filtering Applied to Signal Flow.

These configuration modes use different combinations of the four PWM output channels, and the PWM channels are assigned DSP pins in their appropriate PWM channel pairs. This channel connection and mapping of the pins is shown in Table 4 on page 6. Of the total eight PWM pins, not all pins are used with every configuration mode. The unused PWM pins are disabled by the boot firmware and automatically programmed to be non-active and tri-state their pins are connected to their designated output stages.

In Mode 2 and 3, the PWM channel 3 is used for the subwoofer and is applied to the audio signal flow path, enabling the appropriate digital or low pass filters to be properly inserted into the PWM output channels.

The paired pin inputs are mapped to the PWM channels that are used for the powered outputs. This paired pin mapping assignment is shown in Table 4 on page 6 for the four configurations.

Configuration Mode Assignment

The configuration mode is assigned when the D2-4 family device exits its reset state. At that time, the logic states of the IRQ0/and IRQ1 pins are sampled and latched into the internal device registers. During this initialization time, these pins operate as logic inputs. After completion of the initialization and the internal firmware begins executing, these pins are reassigned as outputs for their shared functions. The internal latched logic states are used by the boot firmware to determine how the device is powered down or reset again. Each mode requires a specific amplifier design hardware connection, and the configuration pin logic levels are defined through pullup or pulldown resistors indicate as that design is used. These modes are fixed for each design and are not intended to be changed for each hardware design.

TABLE. PIN GROUPS, ASSIGNMENT AND CONFIGURATION SIGNALS

GROUP NUMBER	GROUP NAME	GROUP ASSIGNED PIN FOR LOW LEVEL	GROUP ASSIGNED PIN FOR HIGH LEVEL	PIN NUMBER	PIN NAME	PIN NUMBER	PIN NAME	PERMITTED PIN ASSIGNMENT	SUPPORTED GROUP SUPPORTED	PIN FUNCTION
0	2.5 L/R 4 Quadrant	0	1	0	L-Right	0.5	0	4 Quadrant, Full Bridge	0	Powered Left
				1	R-Left	4.7	1	4 Quadrant, Full Bridge	1	Powered Right
				2	-	-	-	-	-	-
				3	-	-	-	-	-	-
				4	-	-	-	-	-	-
1	2.2 L/R L/R Sub Line	0	1	0	L-Right	0.1	0	4 Quadrant, Full Bridge	0	Powered Left
				1	R-Left	2.3	1	4 Quadrant, Full Bridge	1	Powered Right
				2	L-Line	6	-	Line Level	-	Line; Headphone Left
				3	R-Line	7	-	Line Level	-	Line; Headphone Right
				4	Sub	4.6	-	Line Level	-	Line Level Sub
2	2.2 L/R Sub + L/R Line	1	0	0	L-Right	0.1	0	Half Bridge	-	Powered Left
				1	R-Right	2.3	1	Half Bridge	-	Powered Right
				2	L-Line	6	-	Line Level	-	Line; Headphone Left
				3	R-Line	7	-	Line Level	-	Line; Headphone Right
				4	Sub	4.6	2	2 Quadrant, Full Bridge	-	Powered Sub
3	2.2 Bi-Amp	1	1	0	L-InLeq	0.1	-	Half Bridge	-	Powered Left HF
				1	L-InLeq	2.3	1.0	Half Bridge	-	Powered Left LF
				2	R-InLeq	4.5	2	Half Bridge	-	Powered Right HF
				3	R-InLeq	6.7	2	Half Bridge	-	Powered Right LF
				4	-	-	-	-	-	-

Revision History

The revision history provides the technical information for previous versions. It is not necessarily a complete list of all changes made in the document. Please go to the web to make sure that you have the latest revision.

Date	Revision	Details
Mar 28, 2019	FN8763.2	Changed the base part no.page 2 to page 3. Inserted in 32-4 Family Audio SOC. Updated Related Literature section. Replaced all words named "DSSxBoxTM" to "32 Audio DSP", "DSS-X" to "32-X Family", "Digital Audio Suite" to "32 Audio Development Suite", "Sound Box" to "Sound Enhancement Algorithm", "DSP Composer X" to "32 Audio Customization GUI". Updated Audio Enhancement Feature Processing bullet points on page page 32. Updated Ordering Information section. Updated Figures 2, 3, 4, 5, and 6. Removed Block Interl section. Updated Revision section. Updated disclaimer.
May 5, 2016	FN8763.1	Updated entire datasheet applying Intersil's new standards. Updated the Ordering Information table on page 3. Updated Note 8 on page 6. Updated Block Diagram (DSP, DSS) Technology License Required Notice. Added Ordering Information section. Replaced Products on page 3 to About Intersil section. Updated Revision History section. Revision changes are as follows: Changed "Intersil" to "Renesas" throughout document. Updated "Dimension applies to..." to "Between from where dimension is measured to the tolerance". Removed Note of Fig. 5, 6 and 7 in a timeglb.

Trademarks

DTS(R),SRS,and DTS-X(R),WOW, HD™ are registered trademarks of DTS(R),SRS Corporation. Windows™ is a registered trademark of Microsoft Corporation. Other product names are for identification purposes and may be trademarks and/or registered trademarks of their respective companies.

Disclaimer for DTS®(SRS) Technology License Required Notice:

NOTICE OF LICENSE REQUIREMENT: Supply of this implementation of DTS technology to DTS-Product Licensees directly or through a distributor does not issue a royalty payment or convey a license, reduced DTS rights in the implementation, or imply a right under any patent or any other industrial or intellectual property right of DTS to use, offer for sale, sell, or import such implementation in any finished end-user or ready-to-use final product. A license fee and royalty payment to DTS is required prior to and for such use.

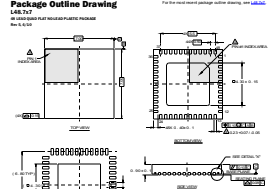
Package Outline Drawing

For the most recent package outline drawing, see L48.7x7.

L48.7x7

48 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

Rev 0, 6/10



NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are responsible for designing, developing, and testing your products in accordance with the latest versions of Renesas Electronics products, taking into account such matters as the operating ranges, safety standards, and other related laws and regulations. Renesas Electronics assumes no liability for losses incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics assumes no liability for infringements of intellectual property or other rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in its original or modified state. Renesas Electronics also assumes no liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
4. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High-Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic devices and industrial robots etc.
   "High-Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large scale communication equipment; financial terminal systems; safety control equipment etc.
   Unless expressly designated in a Renesas Electronics document or other agreement as suitable for use in automotive or in Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may cause damage to human life or bodily injury (artificial life support devices or systems, surgical implantations, etc.), or may cause serious property damage (space systems; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment etc.). Renesas Electronics assumes no liability for any losses and liability for any damages incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Standard" or "High-Quality" in the absence of a prior written agreement between Renesas Electronics and your.
5. When using Renesas Electronics products, refer to the latest published information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating ranges, signal input characteristics, mounting conditions, etc. Renesas Electronics assumes any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
6. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high-reliability product or a product for in-vehicle applications, Renesas Electronics does not consider any single product to be sufficient in terms of safety. Your responsibility as an end-product or system designer includes, but is not limited to, ensuring safety by implementing safety measures using your system or hardware designs, providing redundancy, fire control, and malfunction prevention, assessing the failure or malfunction rate of any Renesas Electronics product, and properly designing for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation, or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
7. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurred as a result of your noncompliance with applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses incurred by you or third parties arising from such noncompliance.
8. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
9. You shall not use Renesas Electronics products or technologies for (1) any purpose relating to the development, design, manufacture, use, stockpiling, etc. of weapons of mass destruction; or (2) any purpose relating to any military application or use by the armed forces of any country.
10. This document shall not be reproduced, reprinted or distributed in any form, in whole or in part, without prior written consent of Renesas Electronics.
11. Contact Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 November 2017)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. Other company names and product names are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/