IMS1600
IMS1601L
CMOS
High Performance
64K x 1 Static RAM

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- 64K x 1 Bit Organization
- 25, 30, 35, 45 and 55 nsec Access Times
- Fully TTL Compatible
- Separate Data Input & Output
- Three-state Output
- Power Down Function
- Single +5V ± 10% Operation
- 22-Pin, 300-mil DIP (JEDEC Std.)
- 22-Pin Ceramic LCC (JEDEC Std.)
- 24-Pin, 300-mil SOJ
- Battery Backup Operation - 2V Data Retention (L version only)

DESCRIPTION

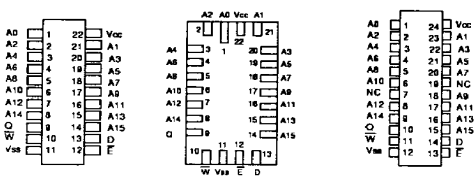
The INMOS IMS1600 is a high performance 64K x 1 CMOS Static RAM. The IMS1600 provides maximum density and speed enhancements with the additional CMOS benefits of lower power and superior reliability.

The IMS1600 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1600 provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

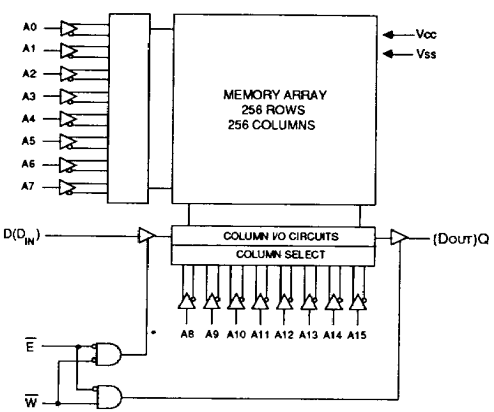
The IMS1601L is a low power version offering battery backup data retention operating from a 2 volt supply.

The IMS1600M and IMS1601LM are MIL-STD-883 versions intended for military applications.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{15}	ADDRESS INPUTS	Q	DATA OUTPUT
$\overline{W}$	WRITE ENABLE	Vcc	POWER
$\overline{E}$	CHIP ENABLE	Vss	GROUND
D	DATA INPUT		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss.....-2.0 to 7.0V
Voltage on Q.....-1.0 to (Vcc+0.5)
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA
(One Second Duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc+0.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	0	25	70	°C	400 linear ft/min air flow

*V_{IL} min = -3 volts for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		77 70	mA mA	tAVAV = 25ns and 30ns (PRELIM) tAVAV = 35, 45 and 55ns
I_{CC2}	Vcc Power Supply Current (Standby,Stable TTL Input Levels)		25	mA	$\overline{E} \geq V_{IH}$. All other inputs at $V_{IN} \leq V_{IL}$ or $\geq V_{IH}$
	IMS1601L version		15		
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		14	mA	$\overline{E} \geq (V_{CC} - 0.2)$. All other inputs at $V_{IN} \leq 0.2$ or $\geq (V_{CC} - 0.2V)$
	IMS1601L version		2		
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		15	mA	$\overline{E} \geq (V_{CC} - 0.2)$. Inputs cycling at $V_{IN} \leq 0.2$ or $\geq (V_{CC} - 0.2V)$
	IMS1601L version		5		
I_{ILK}	Input Leakage Current (Any Input)		± 1	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		± 5	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OL} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OH} = 8mA

Note a: Icc is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels ..... Vss to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels..1.5V
Output Load .....See Figure 1

CAPACITANCE[b] (T_A=25°C, f=1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

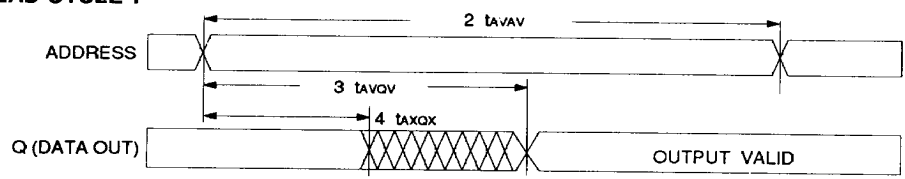
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE[g]

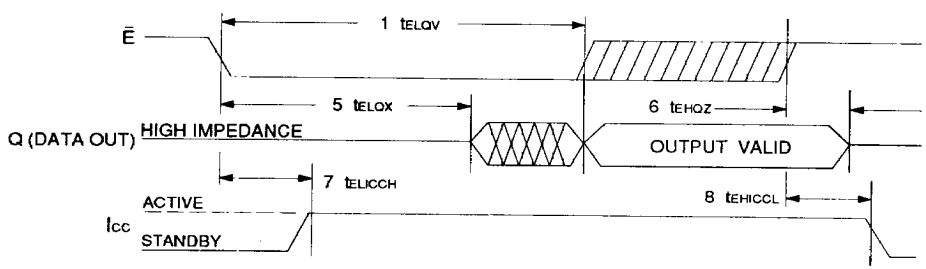
No.	SYMBOL Standard	SYMBOL Alternate	PARAMETER	IMS 1600-25 PRELIM MIN	IMS 1600-25 PRELIM MAX	IMS 1600-30 PRELIM MIN	IMS 1600-30 PRELIM MAX	IMS 1600-35 & 1601-35 MIN	IMS 1600-35 & 1601-35 MAX	IMS 1600-45 & 1601-45 MIN	IMS 1600-45 & 1601-45 MAX	IMS 1600-55 & 1601-55 MIN	IMS 1600-55 & 1601-55 MAX	UNITS	NOTES
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		30		35		45		55	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	25		30		35		45		55		ns	c
3	t_{AVQV}	t_{AA}	Address Access Time		25		30		35		45		55	ns	d
4	t_{AXQX}	t_{OH}	O/P Hold After Address Change	3		3		5		5		5		ns	
5	t_{ELQX}	t_{LZ}	Chip Enable to O/P Active	3		3		5		5		5		ns	j
6	t_{EHQZ}	t_{HZ}	Chip Disable to O/P Inactive	0	15	0	15	0	20	0	25	0	30	ns	f, j
7	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0		0		0		ns	j
8	t_{EHICCL}	t_{PD}	Chip Enable to Power Down		25		30		35		45		55	ns	j
		t_T	I/P Rise and Fall Times		50		50		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c,d]



READ CYCLE 2[c]



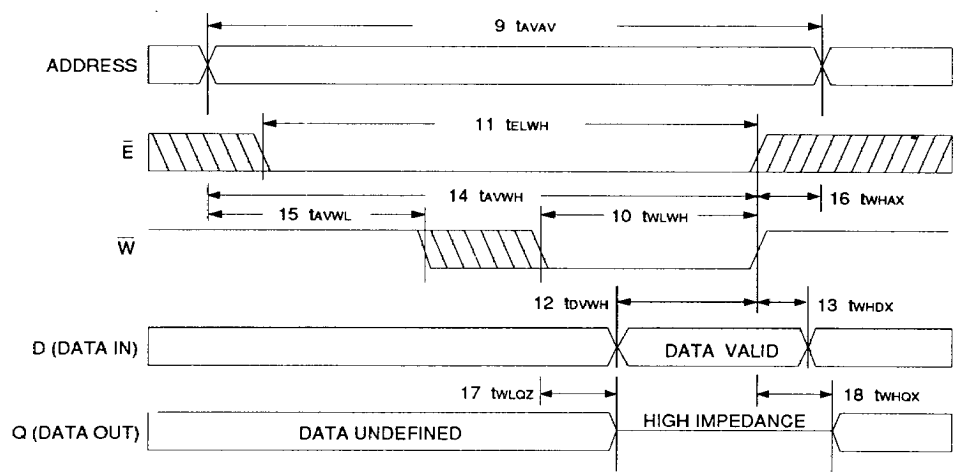
RECOMMENDED AC OPERATING CONDITIONS ($0°C \le T_A \le 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g,h]

No	SYMBOL Standard	SYMBOL Alternate	PARAMETER	IMS 1600-25 PRELIM MIN	IMS 1600-25 PRELIM MAX	IMS 1600-30 PRELIM MIN	IMS 1600-30 PRELIM MAX	IMS 1600-35 & 1601-35 MIN	IMS 1600-35 & 1601-35 MAX	IMS 1600-45 & 1601-45 MIN	IMS 1600-45 & 1601-45 MAX	IMS 1600-55 & 1601-55 MIN	IMS 1600-55 & 1601-55 MAX	UNITS	NOTES
9	tAVAV	tWC	Write Cycle Time	25		30		35		45		55		ns	
10	tWLWH	tWP	Write Plus Width	20		20		20		20		25		ns	
11	tELWH	tCW	Chip Enable to End of Write	20		20		30		30		30		ns	
12	tDVWH	tDW	Data Setup to End of Write	15		15		15		20		20		ns	
13	tWHDX	tDH	Data Hold after End of Write	0		0		0		0		0		ns	
14	tAVWH	tAW	Address Setup End of Write	20		20		25		25		30		ns	
15	tAVWL	tAS	Address Setup to Start of Write	5		5		5		5		5		ns	
16	tWHAX	tWR	Address Hold after End of Write	5		5		5		5		5		ns	
17	tWLQZ	tWZ	Write Enable to Output Disable	0	15	0	15	0	20	0	20	0	25	ns	f,j
18	tWHQX	tOW	Write Enable to Output Disable	0		0		0		0		0		ns	i

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\ge V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



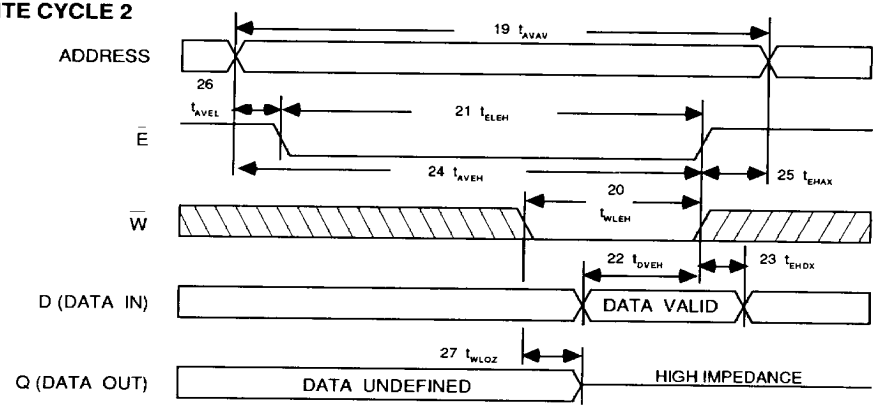
RECOMMENDED AC OPERATING CONDITIONS (0°C ≤ Ta ≤ 70°C) (Vcc = 5.0V ±10%)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g, h]

No	SYMBOL Standard	SYMBOL Alternate	PARAMETER	IMS 1600-25 PRELIM MIN	IMS 1600-25 PRELIM MAX	IMS 1600-30 PRELIM MIN	IMS 1600-30 PRELIM MAX	IMS 1600-35 1601-35 MIN	IMS 1600-35 1601-35 MAX	IMS 1600-45 1601-45 MIN	IMS 1600-45 1601-45 MAX	IMS 1600-55 1601-55 MIN	IMS 1600-55 1601-55 MAX	UNITS	NOTES
19	tAVAV	tWC	Write Cycle Time	25		30		35		45		55		ns	
20	tWLEH	tWP	Write Plus Width	20		20		20		20		25		ns	
21	tELEH	tCW	Chip Enable to End of Write	20		20		30		30		30		ns	
22	tDVEH	tDW	Data Setup to End of Write	15		15		15		20		20		ns	
23	tEHDX	tDH	Data Hold after End of Write	0		0		0		0		0		ns	
24	tAVEH	tAW	Address Setup to End of Write	20		20		30		30		30		ns	
25	tEHAX	tWR	Address Hold after End of Write	5		5		5		5		5		ns	
26	tAVEL	tAS	Address Setup to Start of Write	0		0		0		0		0		ns	
27	tWLQZ	tWZ	Write Enable to Output Disable	0	15	0	15	0	20	0	20	0	25	ns	f,j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between VIH to VIL or VIL to VIH in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be ≥ VIH during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1600 has two control inputs, Chip Enable (/E) and Write Enable (/W), 16 address inputs (A0 -A15), a data in (D) and a data out (Q).

The /E input controls device selection as well as active and standby modes. With /E low, the device is selected and the 16 address inputs are decoded to select one memory cell out of 65,536. Read and Write operations on the memory cell are controlled by the /W input. With /E high, the device is deselected, the output is disabled and the power consumption is reduced to less than one-fourth of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as /W $\geq V_{IH}$ min with /E $\leq V_{IL}$ max. Read access time is measured from either /E going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while /E is low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and long as /E remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by /E going low. As long as address is stable when /E goes low, valid data is at the output at the specified Chip Enable Access time. If address is not valid when /E goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1600 is initiated by the latter of /E or /W to transition from a high to a low. In the case of /W falling last, the output buffer will be turned on t_{ELQX} after the falling edge of /E (just as in a read cycle). The output buffer is then turned off within t_{WLQZ} of the falling edge of /W. During this interval it is possible to have bus contention between devices with D and Q connected together in a common I/O configuration. Therefore input data should not be active until t_{WLQZ} to aviod bus contention.

WRITE CYCLE 1 waveform shows a write cycle terminated by /W going high. Data set-up and hold times are referenced to the rising edge of /W. When /W goes high at the end of the cycle with /E active, the output of the memory becomes active. The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by /E going high. Data set-up and hold times are referenced to the rising edge of /E. With /E high the output remains in the high impedance state.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1600. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Current transients associated with the operation of any high speed device have very high frequency components, so line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad and be placed between each row of devices in the array. A larger tantalum capacitor of a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path. The ground grid of the memory array should extend to the TTL driver periphery circuit area. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

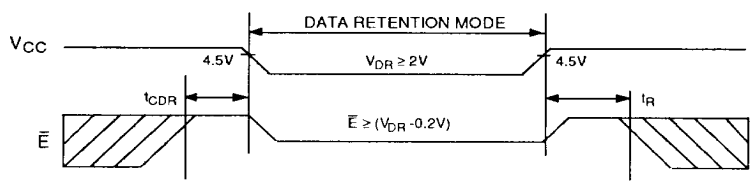
Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.

DATA RETENTION (L version only) ($0°C \le T_A \le 70°C$)

SYMBOL	PARAMETER	MIN	TYP*	MAX	UNITS	NOTES
V_{DR}	Data Retention Voltage	2.0			volts	$V_{IN} \le 0.2V$ or $\ge (V_{CC}-0.2V)$ $\overline{E} \ge (V_{CC}-0.2V)$
I_{CCDR1}	Data Retention Current		8	100	µA	V_{CC} = 3.0 volts
I_{CCDR2}	Data Retention Current		5	70	µA	V_{CC} = 2.0 volts
t_{EHVCCL}	Deselect Time (t_{CDR})	0			ns	j, k
t_{VCCHEL}	Recovery Time (t_R)	t_{RC}			ns	j, k (t_{RC} = Read Cycle Time)

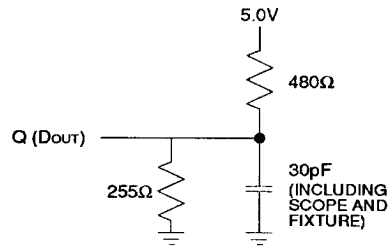
*Typical data retention parameters at 25°C.
Note j: Parameter guaranteed but not tested.
Note k: Supply recovery rate should not exceed 100mV per µs from V_{DR} to V_{CC} min.

LOW V_{CC} DATA RETENTION



Type	Package	Lead finish
A	Formed flat-pack	gold
B	Formed flat-pack	solder
C	LCC	gold
D	Cerdip	solder
E	Small outline, J-bend	solder
G	PGA	gold
H	Small outline, Gull wing	solder
J	PLCC, J-bend	solder
K	Sidebraze ceramic DIP	solder
N	Ceramic LCC	solder
P	Plastic DIP	solder
S	Sidebraze ceramic DIP	gold
T	(Skinny) Flat-pack	solder
W	Ceramic LCC	gold
Y	(Skinny) Flat-pack	gold

FIGURE 1. OUTPUT LOAD

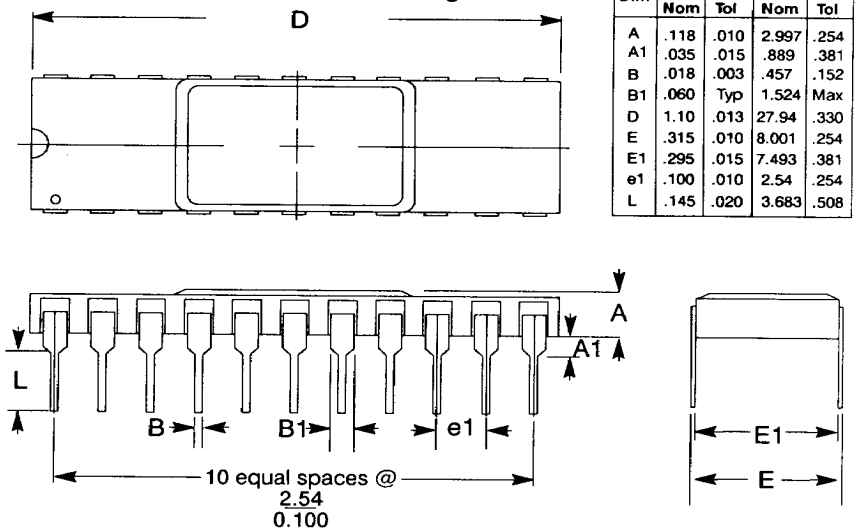


ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER	
			STANDARD	LOW POWER
IMS1600 IMS1601L	25ns	PLASTIC DIP	IMS1600P-25	
	25ns	CERAMIC DIP	IMS1600S-25	
	25ns	CERAMIC LCC	IMS1600W-25	
	25ns	PLASTIC SOJ	IMS1600E-25	
	30ns	PLASTIC DIP	IMS1600P-30	
	30ns	CERAMIC DIP	IMS1600S-30	
	30ns	CERAMIC LCC	IMS1600W-30	
	30ns	PLASTIC SOJ	IMS1600E-30	
	35ns	PLASTIC DIP	IMS1600P-35	IMS1601LP35
	35ns	CERAMIC DIP	IMS1600S-35	IMS1601LS35
	35ns	CERAMIC LCC	IMS1600W-35	IMS1601LW35
	35ns	PLASTIC SOJ	IMS1600E-35	IMS1601LE35
	45ns	PLASTIC DIP	IMS1600P-45	IMS1601LP45
	45ns	CERAMIC DIP	IMS1600S-45	IMS1601LS45
	45ns	CERAMIC LCC	IMS1600W-45	IMS1601LW45
	45ns	PLASTIC SOJ	IMS1600E-45	IMS1601LE45
	55ns	PLASTIC DIP	IMS1600P-55	IMS1601LP55
	55ns	CERAMIC DIP	IMS1600S-55	IMS1601LS55
	55ns	CERAMIC LCC	IMS1600W-55	IMS1601LW55
	55ns	PLASTIC SOJ	IMS1600E-55	IMS1601LE55

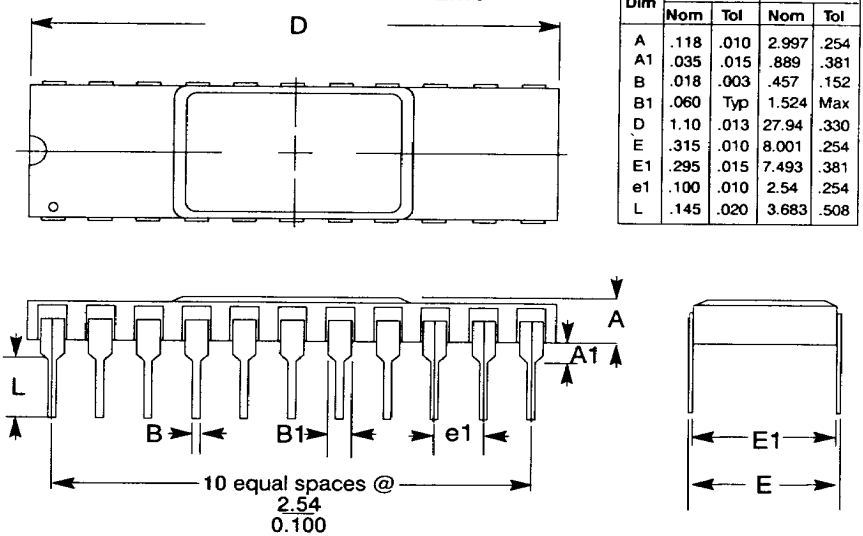
PACKAGING INFORMATION

22 Pin Dual-In-Line-Package



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.118	.010	2.997	.254
A1	.035	.015	.889	.381
B	.018	.003	.457	.152
B1	.060	Typ	1.524	Max
D	1.10	.013	27.94	.330
E	.315	.010	8.001	.254
E1	.295	.015	7.493	.381
e1	.100	.010	2.54	.254
L	.145	.020	3.683	.508

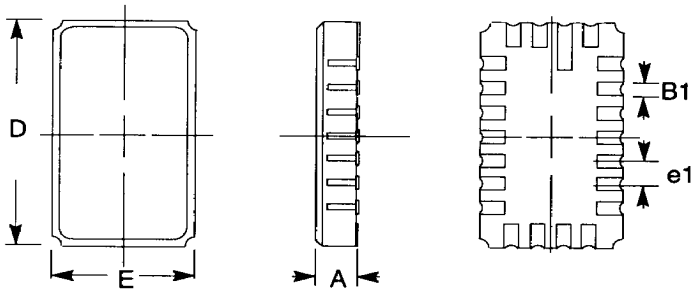
22 Pin Ceramic Dual-In-Line



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.118	.010	2.997	.254
A1	.035	.015	.889	.381
B	.018	.003	.457	.152
B1	.060	Typ	1.524	Max
D	1.10	.013	27.94	.330
E	.315	.010	8.001	.254
E1	.295	.015	7.493	.381
e1	.100	.010	2.54	.254
L	.145	.020	3.683	.508

22 Pin Leadless Chip Carrier

Dim	Inches		mm		Notes
	Nom	Tol	Nom	Tol	
A	.071	.007	1.803	.178	
B1	.025	.003	.635	.076	
D	.490	.006	13.446	.152	
E	.290	.006	7.366	.152	
e1	.050		1.270		



24 Pin Plastic J Leaded SOJ

Dim	Inches		mm		Notes
	Min	Max	Min	Max	
A	.120	.140	3.048	3.556	
B1	.014	.019	.356	.483	
C	.010		.254		
D	.602	.612	15.291	15.545	
E	.335	.347	8.509	8.814	
E1	.292	.299	7.417	7.595	
e1	.050	.050	1.270	1.270	
eA	.262	.272	6.655	6.909	
L	.028	.036	.711	.914