DATA SHEET

PCA9541

2-to-1 I^2C master selector with interrupt logic and reset

Product data sheet
Supersedes data of 2003 Dec 02

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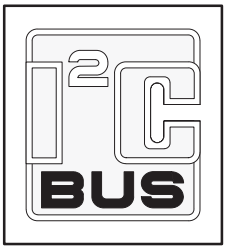
2-to-1 I²C master selector with interrupt logic and reset PCA9541



FEATURES

- 2-to-1 bi-directional master selector
- I²C interface logic; compatible with SMBus standards
- PCA9541/01 powers-up with Channel 0 selected
- PCA9541/02 powers-up with Channel 0 selected after STOP condition detected (bus idle) on Channel 0
- PCA9541/03 powers-up with no channel selected and either master can take control of the bus
- Active LOW Interrupt Input
- 2 Active LOW Interrupt Outputs
- Active LOW Reset Input
- 4 address pins allowing up to 16 devices on the I²C-bus
- Channel selection via I²C-bus
- Bus initialization/recovery function
- Bus traffic sensor
- Low Rds_{ON} switches
- Allows voltage level translation between 1.8 V, 2.5 V, 3.3 V and 5 V buses
- No glitch on power-up
- Supports hot insertion
- Software identical for both masters
- Low stand-by current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 6.0 V tolerant Inputs
- 0 to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO16, TSSOP16, HVQFN16

APPLICATIONS

- High reliability systems with dual masters
- Gatekeeper multiplexer on long single bus
- Bus initialization/recovery for slave devices without hardware reset
- Allows masters without arbitration logic to share resources

DESCRIPTION

The PCA9541 is a 2-to-1 I²C master selector designed for high reliability dual master I²C applications where system operation is required, even when one master fails or the controller card is removed for maintenance. The two masters (e.g., primary and back-up) are located on separate I²C-buses that connect to the same downstream I²C-bus slave devices. I²C commands are sent by either I²C-bus master and are used to select one master at a time. Either master at any time can gain control of the slave devices if the other master is disabled or removed from the system. The failed master is isolated from the system and will not affect communication between the on-line master and the slave devices on the downstream I²C-bus.

Three versions are offered for different architectures. PCA9541/01 with channel 0 selected at start-up, PCA9541/02 with channel 0 selected after start-up and after stop condition is detected, and PCA9541/03 with no channel selected after start-up.

The interrupt outputs are used to provide an indication of which master has control of the bus. One interrupt input ($\overline{INT\_IN}$) collects downstream information and propagates it to the 2 upstream I²C-buses ($\overline{INT0}$ and $\overline{INT1}$) if enabled. $\overline{INT0}$ and $\overline{INT1}$ are also used to let the previous bus master know that it is not in control of the bus anymore and to indicate the completion of the bus recovery/initialization sequence. Those interrupts can be disabled and will not generate an interrupt if the masking option is set.

A bus recovery/initialization if enabled sends nine clock pulses, a not acknowledge, and a stop condition in order to set the downstream I²C-bus devices to an initialized state before actually switching the channel to the selected master.

An interrupt is sent to the upstream channel when the recovery/initialization procedure is completed.

An internal bus sensor senses the downstream I²C traffic and generates an interrupt if a channel switch occurs during a non-idle bus condition. This function is enabled when the PCA9541 recovery/initialization is not used. The interrupt signal informs the master that an external I²C-bus recovery/initialization needs to be performed. It can be disabled and an interrupt will not be generated.

The pass gates of the switches are constructed such that the V_{DD} pin can be used to limit the maximum high voltage, which will be passed by the PCA9541. This allows the use of different bus voltages on each pair, so that 1.8 V 2.5 V or 3.3 V devices can communicate with 5 V devices without any additional protection.

The PCA9541 does not isolate the capacitive loading on either side of the device so the designer must take into account all trace and device capacitances on both sides of the device, and pull-up resistors must be used on all channels.

External pull-up resistors pull the bus to the desired voltage level for each channel. All I/O pins are 6.0 V tolerant.

An active-LOW Reset Input allows the PCA9541 to be initialized. Pulling the $\overline{RESET}$ pin LOW resets the I²C state machine and configures the device to its default state as does the internal power on reset function.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DRAWING NUMBER
16-Pin Plastic SO	–40 to +85 °C	PCA9541D/01	PCA9541D/01	SOT109-1
16-Pin Plastic TSSOP	–40 to +85 °C	PCA9541PW/01	9541/01	SOT403-1
16-Pin Plastic HVQFN	–40 to +85 °C	PCA9541BS/01	41/1	SOT629-1
16-Pin Plastic SO	–40 to +85 °C	PCA9541D/02	PCA9541D/02	SOT109-1
16-Pin Plastic TSSOP	–40 to +85 °C	PCA9541PW/02	9541/02	SOT403-1
16-Pin Plastic HVQFN	–40 to +85 °C	PCA9541BS/02	41/2	SOT629-1
16-Pin Plastic SO	–40 to +85 °C	PCA9541D/03	PCA9541D/03	SOT109-1
16-Pin Plastic TSSOP	–40 to +85 °C	PCA9541PW/03	9541/03	SOT403-1
16-Pin Plastic HVQFN	–40 to +85 °C	PCA9541BS/03	41/3	SOT629-1

Standard packing quantities and other packaging data are available at www.standardproducts.philips.com/packaging.

PIN CONFIGURATION

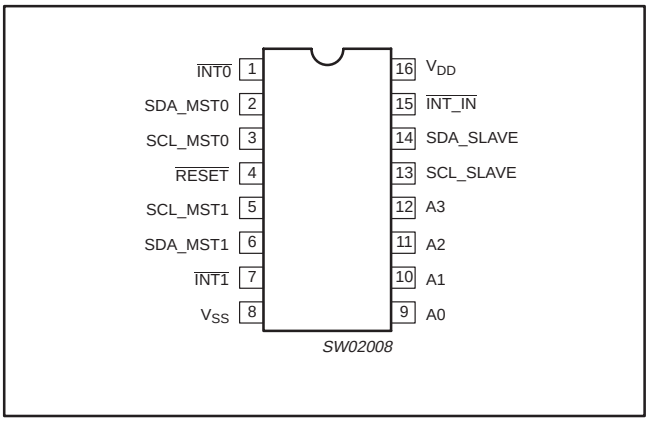


Figure 1. SO16/TSSOP16 pin configuration.

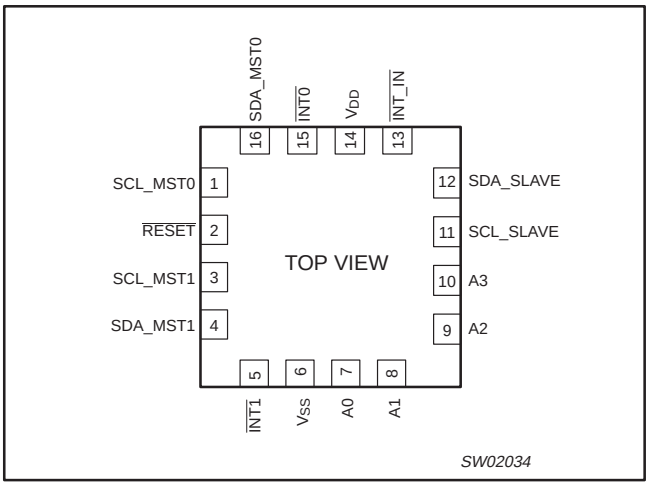


Figure 2. HVQFN16 pin configuration.

PIN DESCRIPTION

SO/TSSOP PIN NUMBER	HVQFN PIN NUMBER	SYMBOL	FUNCTION
1	15	$\overline{INT0}$	Active LOW interrupt output 0 (external pull-up required)
2	16	SDA_MST0	Serial data master 0 (external pull-up required)
3	1	SCL_MST0	Serial clock master 0 (external pull-up required)
4	2	$\overline{RESET}$	Active LOW reset input (external pull-up required)
5	3	SCL_MST1	Serial clock master 1 (external pull-up required)
6	4	SDA_MST1	Serial data master 1 (external pull-up required)
7	5	$\overline{INT1}$	Active LOW interrupt output 1 (external pull-up required)
8	6	V_{SS}	Supply ground
9	7	A0	Address input 0 (externally held to GND or V_{CC})
10	8	A1	Address input 1 (externally held to GND or V_{CC})
11	9	A2	Address input 2 (externally held to GND or V_{CC})
12	10	A3	Address input 3 (externally held to GND or V_{CC})
13	11	SCL_SLAVE	Serial clock slave (external pull-up required)
14	12	SDA_SLAVE	Serial data slave (external pull-up required)
15	13	$\overline{INT\_IN}$	Active LOW interrupt input (external pull-up required)
16	14	V_{DD}	Supply voltage

BLOCK DIAGRAM

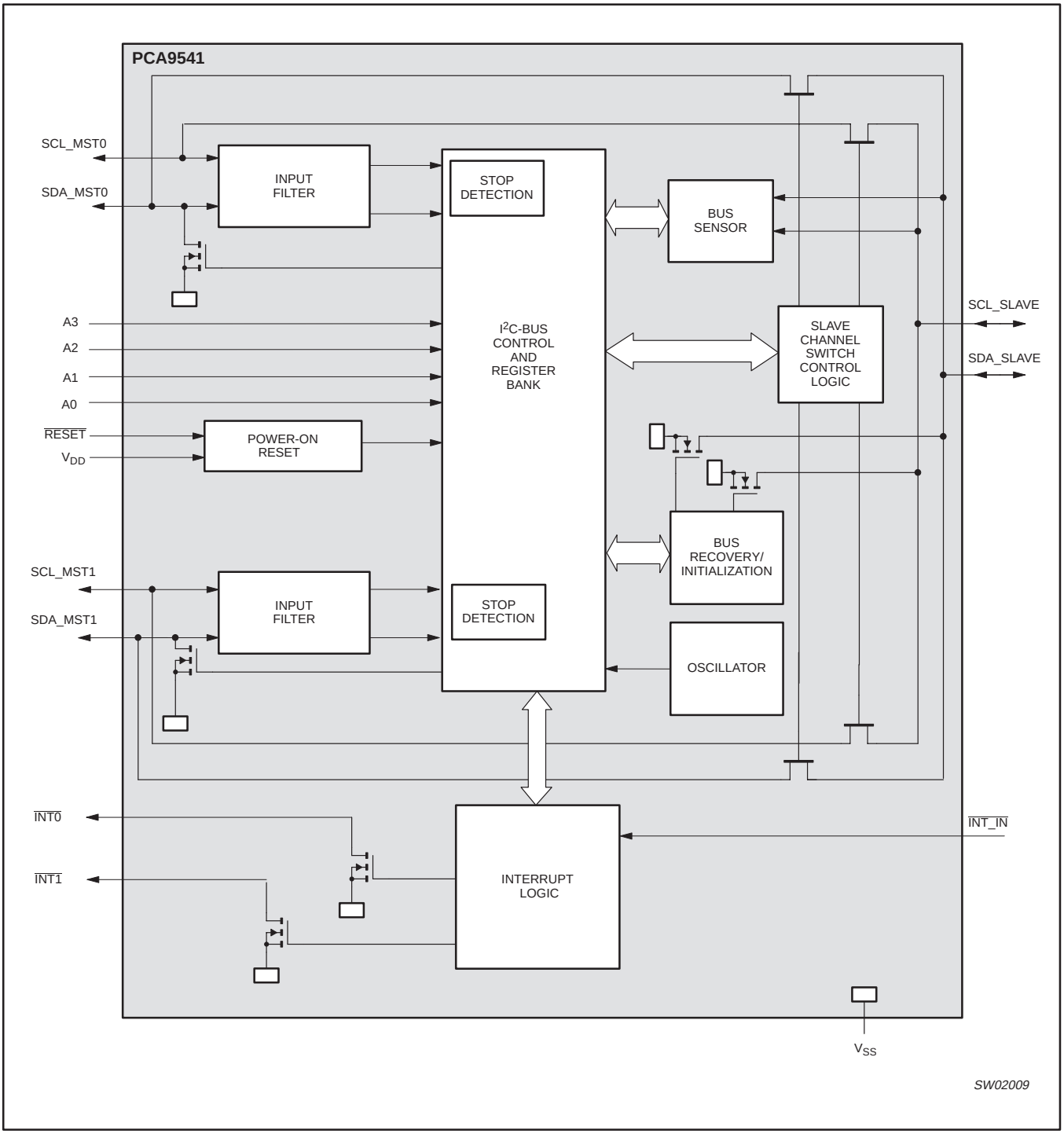


Figure 3. Block diagram

DEVICE ADDRESS

Following a START condition, the upstream master that wants to control the I²C-bus or make a status check must send the address of the slave it is accessing. The slave address of the PCA9541 is shown in Figure 4. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable pins and they must be pulled HIGH or LOW.

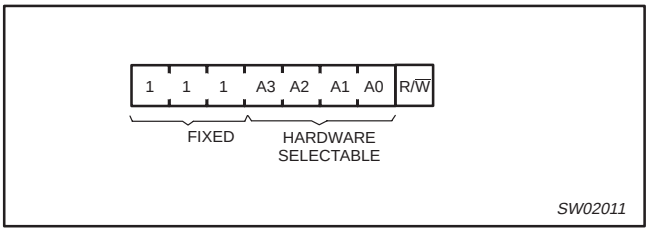


Figure 4. Slave address

The last bit of the slave address defines the operation to be performed. When set to logic 1 a read is selected while logic 0 selects a write operation.

COMMAND CODE

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9541, which will be stored in the Command Code register.

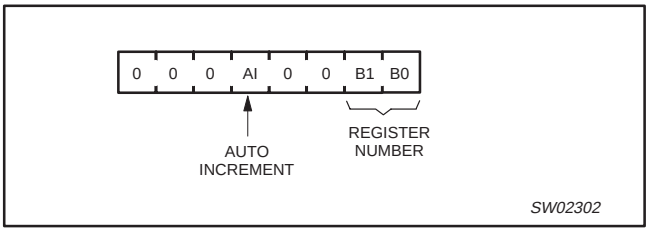


Figure 5. Command Code

The 2 LSBS are used as a pointer to determine which register will be accessed.

If the auto-increment flag is set (AI=1), the two least significant bits of the Command Code are automatically incremented after a byte has been read or written. This allows the user to program the registers sequentially or to read them sequentially.

- During a Read operation, the contents of these bits will rollover to “00” after the last allowed register is accessed (“10”).
- During a Write operation, the PCA9541 will acknowledge bytes sent to the IE and CONTROL registers but will not acknowledge a byte sent to the Interrupt Status Register since it is a read-only register. The 2 LSB’s of the Command Code do not roll over to 00 but stays at 10.

Only the 2 least significant bits are affected by the AI flag.

Unused bits must be programmed with zeroes. Any command code (Write operation) different from “000AI0000”, “000AI0001”, and “000AI0010” will not be acknowledged. At power-up, this register defaults to all zeros.

Table 1. Command Code Register

B1	B0	REGISTER NAME	TYPE	REGISTER FUNCTION
0	0	IE	Read/Write	Interrupt Enable
0	1	CONTROL	Read/Write	Control Switch
1	0	ISTAT	Read	Interrupt Status
1	1	NOT ALLOWED		

Each system master controls its own set of registers, however they can also read specific bits from the other system master.

PCA9541 INTERNAL REGISTER MAP

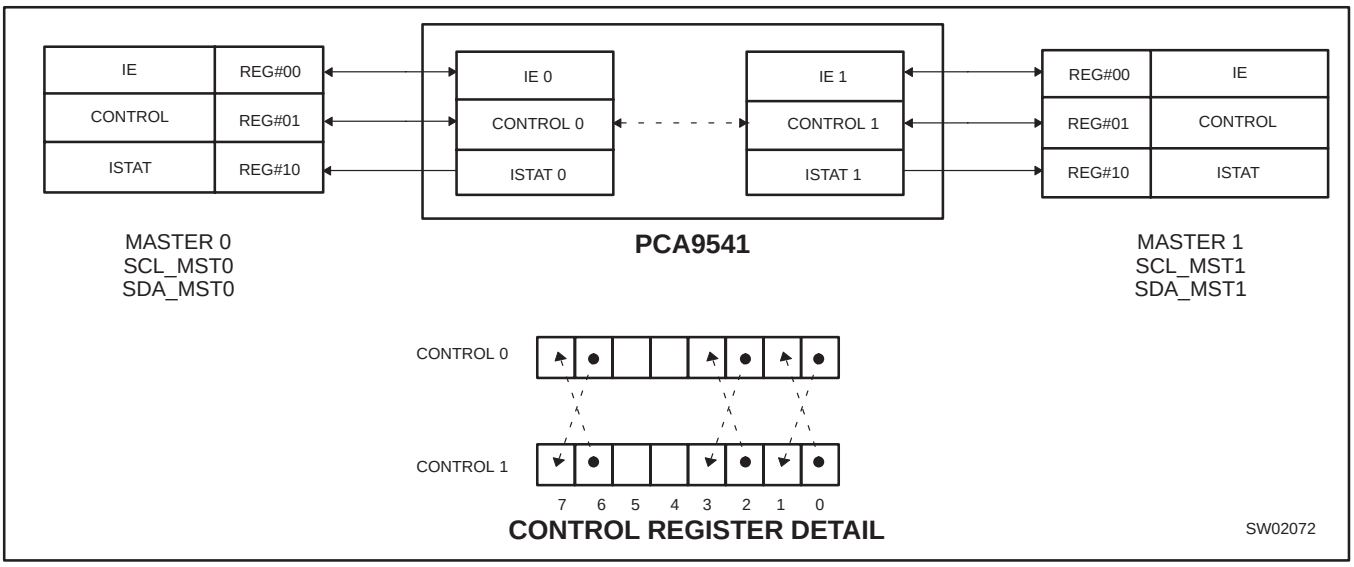


Figure 6. Internal register map

INTERRUPT ENABLE AND CONTROL REGISTERS DESCRIPTION

When a master seeks control of the bus by connecting its I²C channel to the PCA9541 downstream channel, it has to write to the Control Register (Reg#01)

Bits MYBUS and BUSON allow the master to take control of the bus.

The MYBUS and the NMYBUS bits determine which master has control of the bus. Tables 4 and 5 explain which master gets control of the bus and how. There is no arbitration. Any master can take control of the bus when it wants regardless of whether the other master is using it or not.

The BUSON and the NBUSON bits determine whether the upstream bus is connected or disconnected to/from the downstream bus.

Internally, the state machine does the following:

- If the combination of the BUSON and the NBUSON bits causes the upstream to be disconnected from the downstream bus, then that is done. So in this case, the values of the MYBUS and the NMYBUS do not matter.
- If a master was connected to the downstream bus prior to the disconnect, then an interrupt is sent on the respective interrupt output in an attempt to let that master know that it is no longer connected to the downstream bus. This is indicated by setting the BUSLOST bit in the Interrupt Status Register.
- If the combination of the BUSON and the NBUSON bits causes a master to be connected to the downstream bus and if there is no change in the BUSON bits since when the disconnect took effect, then the master requesting the bus is connected to the downstream bus. If it requests a bus initialization sequence, then it is performed.
- If there is no change in the combination of the BUSON and the NBUSON bits and a new master wants the bus, then the downstream bus is disconnected from the old master that was using it and the new master gets control of it. Again, the bus initialization if requested is done. The appropriate interrupt signals are generated.

After a master has sent the bus control request:

1. The previous master is disconnected from the I²C-bus. An interrupt to the previous master is sent through its $\overline{INT}$ line to let it know that it lost control of the bus. BUSLOST bit in the Interrupt Status Register is set. This interrupt can be masked by setting the BUSLOSTMSK bit to 1.
2. A built-in bus initialization/recovery function can take temporary control of the downstream channel to initialize the bus before making the actual switch to the new bus master. This function is activated by setting the BUSINIT to 1 by the master during the same write sequence as the one programming MYBUS and BUSON bits.

   When activated and whether the bus was previously idle or not:
   - 9 clock pulses are sent on the SCL_SLAVE.
   - SDA_SLAVE line is released (HIGH) when the clock pulses are sent to SCL_SLAVE. This is equivalent to sending 8 data bits and a not acknowledge
   - Finally a STOP condition is sent to the downstream slave channel.

   This sequence will complete any read transaction which was previously in process and the downstream slave configured as a slave-transmitter should release the SDA line because the PCA9541 did not acknowledge the last byte.
3. When the initialization has been requested and completed, the PCA9541 sends an interrupt to the new master through its $\overline{INT}$ line and connects the new master to the downstream channel. BUSINIT bit in the Interrupt Status Register is set. **The switch operation occurs after the master asking the bus control has sent a STOP command.** This interrupt can be masked by setting the BUSINITMSK bit to 1.
4. When the bus initialization/recovery function has not been requested (BUSINIT=0), the PCA9541 connects the new master to the slave downstream channel. **The switch operation occurs after the master asking the bus control has sent a STOP command.** PCA9541 sends an interrupt to the new master through its $\overline{INT}$ line if the built-in bus sensor function detects a non-idle condition in the downstream slave channel at the switching time. BUSOK bit in the Interrupt Status Register is set. This means that a STOP condition has not been detected in the previous bus communication and that an external bus recovery/initialization must be performed. If an idle condition has been detected at the switching time, no interrupt will be sent. This interrupt can be masked by setting the BUSOKMSK bit to 1.

Interrupt status can be read. See paragraph INTERRUPT STATUS REGISTER DESCRIPTION for more information.

The MYTEST and the NMYTEST bits cause the interrupt pins of the respective masters to be activated for a ”functional interrupt test”.

NOTES:

1. The regular way to proceed is that a master asks to take the control of the bus by programming MYBUS and BUSON bits. Nevertheless, the same master can also decide to give up the control of the bus and give it to the other master. This is also done by programming the MYBUS and BUSON bits.
2. Any writes either to the Interrupt Enable Register or the Control Register cause the respective register to be updated on the 9th clock cycle, i.e. on the rising edge of the acknowledge clock cycle.
3. The actual switch from one channel to another or the switching off of both the channels happens on a STOP command.

Register 0: Interrupt Enable (IE) Register (B1B0 = 00)

This register allows a master to read and/or write (if needed) Mask options for its own channel.

The Interrupt Enable Register described below is identical for both the masters. Nevertheless, there are physically 2 internal Interrupt Enable Registers, one for each upstream channel.

When Master 0 reads/writes in this register, the internal Interrupt Enable Register 0 will be accessed.

When Master 1 reads/writes in this register, the internal Interrupt Enable Register 1 will be accessed.

BIT	7	6	5	4	3	2	1	0
SYMBOL	0	0	0	0	BUSLOSTMSK	BUSOKMSK	BUSINITMSK	INTINMSK

Table 2. Register 0

BIT	SYMBOL	READ/ WRITE	DEFAULT	DESCRIPTION
0	INTINMSK	R/W	0	0: Interrupt on $\overline{INT\_IN}$ will generate an interrupt on $\overline{INT}$
				1: Interrupt on $\overline{INT\_IN}$ will not generate an interrupt on $\overline{INT}$ (masked)
1	BUSINITMSK	R/W	0	0: After connection is requested and Bus Initialization requested (BUSINIT = 1), an interrupt on $\overline{INT}$ will be generated when the bus initialization is done. Note: Channel switching is done after bus initialization completed.
				1: After connection is requested and Bus Initialization requested (BUSINIT = 1), an interrupt on $\overline{INT}$ will not be generated when the bus initialization is done (masked). Note: Channel switching is done after bus initialization completed.
2	BUSOKMSK	R/W	0	0: After connection is requested and Bus Initialization not requested (BUSINIT = 0), an interrupt on $\overline{INT}$ will be generated when a non-Idle situation has been detected on the downstream slave channel by the bus sensor at the switching moment. Note: Channel switching is done automatically after the STOP command.
				1: After connection is requested and Bus Initialization not requested (BUSINIT = 0), an interrupt on $\overline{INT}$ will not be generated when a non-Idle situation has been detected on the downstream slave channel by the bus sensor at the switching moment (masked). Note: Channel switching is done automatically after the STOP command.
3	BUSLOSTMSK	R/W	0	0: An interrupt on $\overline{INT}$ will be generated after the other master has been been disconnected
				1: An interrupt on $\overline{INT}$ will not be generated after the other master has been been disconnected.
4	NOT USED	R only	0	
5	NOT USED	R only	0	
6	NOT USED	R only	0	
7	NOT USED	R only	0	

NOTE:
Default values are the same for PCA9541/01, PCA9541/02, and PCA9541/03

Register 1: Control Register (B1B0 = 01)

x stands for 0 or 1 and is applied to the master that reads or writes in the Control Register explained below

The Control Register described below is identical for both the masters. Nevertheless, there are physically 2 internal Control Registers, one for each upstream channel.

When master 0 reads/writes in this register, the internal Control Register 0 will be accessed.

When master 1 reads/writes in this register, the internal Control Register 1 will be accessed.

BIT	7	6	5	4	3	2	1	0
SYMBOL	NTESTON	TESTON	0	BUSINIT	NBUSON	BUSON	NMYBUS	MYBUS

Table 3. Register 1

BIT	SYMBOL	READ/ WRITE	DEFAULT	DESCRIPTION
0	MYBUS	R/W	See Table 6	MYBUS bit along with the NMYBUS bit decides which upstream channel is connected to the downstream channel See Table 4
1	NMYBUS	R only	See Table 6	NMYBUS bit is a copy of the MYBUS bit for the other channel See Table 4
2	BUSON	R/W	See Table 6	BUSON bit along with the NBUSON bit decides whether any upstream channel is connected to the downstream channel or not See Table 5
3	NBUSON	R only	See Table 6	NBUSON bit is a copy of the BUSON bit for the other channel See Table 5
4	BUSINIT	R/W	0	0: Bus initialization not requested
				1 : Bus initialization requested
5	NOT USED	R only	0	
6	TESTON	R/W	0	0: a Logic Level High to the $\overline{INT}$ line is sent (interrupt cleared)
				1: a Logic Level Low to the $\overline{INT}$ line is sent (interrupt generated)
7	NTESTON	R only	0	0: a Logic Level High to the $\overline{INT}$ line of the other channel is sent (interrupt cleared)
				1: a Logic Level Low to the $\overline{INT}$ line of the other channel is sent (interrupt generated)

Table 4. MYBUS and NMYBUS Truth Table

NMYBUS	MYBUS	SLAVE CHANNEL
0	0	to the switching initiator
1	0	to the other channel
0	1	to the other channel
1	1	to the switching initiator

Table 5. BUSON and NBUSON Truth Table

NBUSON	BUSON	SLAVE CHANNEL
0	0	OFF
1	0	ON
0	1	ON
1	1	OFF

NOTES:

1. Switch to the new channel is done when the master initiating the switch request sends a STOP command to the PCA9541.
2. If Master 0 wants to change the connection to the downstream channel in any way, it needs to write to **its Control Register (Reg#01), and then send a STOP command** because an update of the connection to the downstream according to the values in the two internal Control Registers happens only on a STOP command. Writing to one control register followed by a STOP condition on the other Master's channel will not cause an update to the downstream connection.
3. When both masters request a switch to their own channel at the same time, the master who last wrote to its control register before the PCA9541 receives a STOP command wins the switching sequence. There is no arbitration performed.
4. Auto Increment feature (AI=1) allows to program the PCA9541 in 4 bytes:
   - Start
   - 111A3A2A1A0 + 0 PCA9541 Address + Write
   - 00010000 Select Reg#00 with AI = 1
   - Data Reg#00 Interrupt Enable Register Data
   - Data Reg#01 Control Register Data
   - Stop

Table 6. Default Control Register Values

	BIT	7	6	5	4	3	2	1	0
VERSION	SYMBOL	NTESTON	TESTON	NOT USED	BUSINIT	NBUSON	BUSON	NMYBUS	MYBUS
PCA9541/01	MST_0	0	0	0	0	0	1	0	0
	MST_1	0	0	0	0	1	0	1	0
PCA9541/02	MST_0	0	0	0	0	0	0	0	0
	MST_1	0	0	0	0	0	0	1	0
PCA9541/03	MST_0	0	0	0	0	0	0	0	0
	MST_1	0	0	0	0	0	0	1	0
PCA9541/02 (AFTER STOP)	MST_0	0	0	0	0	0	1	0	0
	MST_1	0	0	0	0	1	0	1	0

Table 7 describes which command needs to be written to the Control Register when a master device wants to take control of the I²C-bus. Byte written to the Control Register is a function of the current I²C-bus control status performed after an initial reading of the Control Register.

Current status of the I²C-bus is determined by the bits MYBUS, NMYBUS, BUSON and NBUSON is one of the following:

– The master reading its Control Register does not have control and the I²C-bus is off.
– The master reading its Control Register does not have control and the I²C-bus is on.
– The master reading its Control Register has control and the I²C-bus is off.
– The master reading its Control Register has control and the I²C-bus is on.

'I²C-bus off' means that upstream and downstream channels are not connected together.

'I²C-bus on' means that upstream and downstream channels are connected together.

Remark: Only the 4 LSBs of the Control Register are described in Table 7 since only those bits control the I²C-bus control. The logic value for the 4 MSBs is specific to the application and are not discussed in the table.

The Read sequence is performed by the master as following:
S — 111xxxx0 — 000x0001 — Sr — 111xxxx1 — DataRead — P

The Write sequence is performed by the master as following:
S — 111xxxx0 — 000x0001 — DataWritten — P

Table 7. Bus control sequence

Read Control Register performed by the Master							Write Control Register performed by the Master		
Byte Read only the 4 LSBs are shown	Status		NBUSON	BUSON	NMYBUS	MYBUS	Byte Written only the 4 LSBs are shown (see Note 1)		Action performed to take Mastership
Hex							Binary	Hex	
0x0	Bus off	Has control	0	0	0	0	x1x0	0x4	Bus on
0x1	Bus off	No control	0	0	0	1	x1x0	0x4	Bus on, Take control
0x2	Bus off	No control	0	0	1	0	x1x1	0x5	Bus on, Take control
0x3	Bus off	Has control	0	0	1	1	x1x1	0x5	Bus on
0x4	Bus on	Has control	0	1	0	0	No write required	–	No change
0x5	Bus on	No control	0	1	0	1	x1x0	0x4	Take control
0x6	Bus on	No control	0	1	1	0	x1x1	0x5	Take control
0x7	Bus on	Has control	0	1	1	1	No write required	–	No change
0x8	Bus on	Has control	1	0	0	0	No write required	–	No change
0x9	Bus on	No control	1	0	0	1	x0x0	0x0	Take control
0xA	Bus on	No control	1	0	1	0	x0x1	0x1	Take control
0xB	Bus on	Has control	1	0	1	1	No write required	–	No change
0xC	Bus off	Has control	1	1	0	0	x0x0	0x0	Bus on
0xD	Bus off	No control	1	1	0	1	x0x0	0x0	Bus on, Take control
0xE	Bus off	No control	1	1	1	0	x0x1	0x1	Bus on, Take control
0xF	Bus off	Has control	1	1	1	1	x0x1	0x1	Bus on

NOTES:
1. x0x0 = 0x0, 0x2, 0x8, 0xA
   x0x1 = 0x1, 0x3, 0x9, 0xB
   x1x0 = 0x4, 0x6, 0xC, 0xE
   x1x1 = 0x5, 0x7, 0xD, 0xF

INTERRUPT STATUS REGISTERS DESCRIPTION

The PCA9541 provides 4 different types of interrupt:

1. To indicate to the former I²C-bus master that it is not in control of the bus anymore.
2. To indicate to the new I²C-bus master that:
   - The bus recovery/initialization has been performed and that the downstream channel connection has been done (built-in bus recovery/initialization active).
   - A “bus not well initialized” condition has been detected by the PCA9541 when the switch has been done (built-in bus recovery/initialization not active). This information can be used by the new master to initiate its own bus recovery/initialization sequence.
3. Indicate to both I²C upstream masters that a downstream interrupt has been generated through the INT_IN pin.
4. Functionality wiring test.

Bus control lost interrupt

When an upstream master takes control of the I²C-bus while the other channel was using the downstream channel, an interrupt is generated to the master losing control of the bus ($\overline{INT}$ line goes LOW to let the master know that it lost the control of the bus) immediately after disconnection from the downstream channel.

By setting the BUSLOSTMSK bit to 1, the interrupt is masked and the upstream master that lost the I²C-bus control does not receive an interrupt ($\overline{INT}$ line does not go LOW).

Recovery/initialization interrupt

Before switching to a new upstream channel, an automatic bus recovery/initialization can be performed by the PCA9541. This function is requested by setting the BUSINIT bit to 1. When the downstream bus has been initialized, an interrupt to the new master is generated ($\overline{INT}$ line goes LOW).

By setting the BUSINITMSK bit to 1, the interrupt is masked and the new master does not receive an interrupt ($\overline{INT}$ line does not go LOW).

When the automatic bus recovery/initialization is not requested, if the built-in bus sensor function (sensing permanently the downstream I²C traffic) detects a non-idle condition (previous bus channel connected to the downstream slave channel, was between a START and STOP condition), then an interrupt to the new master is sent ($\overline{INT}$ line goes LOW). This interrupt tells the new master that an external bus recovery/initialization must be performed. By setting the BUSOKMSK bit to 1, the interrupt is masked and the new master does not receive an interrupt ($\overline{INT}$ line does not go LOW).

NOTE: In this particular situation, after the switch to the new master is performed, **a read of the Interrupt Status Register is not possible if the switch happened in the middle of a read sequence** because the new master does not have control of the SDA line

Downstream interrupt

An interrupt can also be generated by a downstream device by asserting the $\overline{INT\_IN}$ pin LOW. When $\overline{INT\_IN}$ is asserted LOW and if both INTINMSK bits are not set to 1 by either master, $\overline{INT0}$ and $\overline{INT1}$ both go LOW.

By setting the INTINMSK bit to 1 by a master and/or the INTINMSK bit to 1 by the other master, the interrupt(s) is (are) masked and the corresponding masked channel(s) does (do) not receive an interrupt ($\overline{INT0}$ and/or $\overline{INT1}$ line does (do) not go LOW).

Functional test interrupt

A master can send an interrupt to itself to test its own $\overline{INT}$ wire or send an interrupt to the other master to test its $\overline{INT}$ line. This is done by:

- Setting the TESTON bit to 1 to test its own $\overline{INT}$ line.
- Setting the NTESTON bit to 1 to test the other master $\overline{INT}$ line.

Setting the TESTON and/or NTESTON bits to 0 by a master will clear the interrupt(s).

NOTE: Interrupt outputs have an open-drain structure. Interrupt input does not have any internal pull-up resistor and must not be left floating (e.g., pulled high to V_{CC} through resistor) in order to avoid any undesired interrupt conditions.

Register 2: Interrupt Status Register (B1B0 = 10)

The Interrupt Status Register for both the masters is identical and is described below. Nevertheless, there are physically 2 internal Interrupt Registers, one for each upstream channel.

When Master 0 reads this register, the internal Interrupt Register 0 will be accessed.

When Master 1 reads this register, the internal Interrupt Register 1 will be accessed.

BIT	7	6	5	4	3	2	1	0
SYMBOL	NMYTEST	MYTEST	0	0	BUSLOST	BUSOK	BUSINIT	INTIN

Table 8. Register 2

BIT	SYMBOL	READ/ WRITE	DEFAULT	DESCRIPTION
0	INTIN	R only	0	0: No interrupt on interrupt input ($\overline{INT\_IN}$)
				1: Interrupt on interrupt input ($\overline{INT\_IN}$)
1	BUSINIT	R only	0	0: No interrupt generated by the bus recovery/initialization function
				1: Interrupt generated by the bus recovery/initialization function – recovery/initialization done
2	BUSOK	R only	0	0: No interrupt generated by bus sensor function
				1: Interrupt generated by bus sensor function (masked when bus recovery/initialization requested) – Bus was not idle when the switch occurred
3	BUSLOST	R only	0	0: No interrupt generated to the previous master when switching to the new one is initiated
				1: Interrupt generated to the previous master when switching to the new one is initiated
4	NOT USED	R only	0	
5	NOT USED	R only	0	
6	MYTEST	R only	0	0: No interrupt generated by TESTON bit f (TESTON = 0)
				1: Interrupt generated by TESTON bit (TESTON = 1)
7	NMYTEST	R only	0	0: No interrupt generated due to NTESTON bit from the other master (NTESTON = 0 from the other master)
				1: Interrupt generated due to TESTON bit from the other master (NTESTON = 1 from the other master)

NOTES:

1. Interrupt on a master is cleared after TESTON bit is cleared the same master or NTESTON bit is cleared by the other master.
2. If the interrupt condition remains on $\overline{INT\_IN}$ after the Read sequence, another interrupt will be generated (if the interrupt has not been masked)
3. Default values are the same for PCA9541/01, PCA9541/02 and PCA9541/03
4. Reading the Interrupt Status Register does not clear the MYTEST, NMYTEST or the INTIN bits. They are cleared if:
   - $\overline{INT\_IN}$ lines goes HIGH for INTIN bit
   - TESTON bit is cleared for MYTEST bit
   - NTESTON bit is cleared for NMYTEST bit
5. BUSINIT, BUSOK and BUSLOST bits in the Interrupt Status Register gets cleared after a Read of the same register is done. Precisely, the register gets cleared on the second clock pulse during the read operation.

POWER-ON RESET

When power is applied to V_{DD}, an internal Power-On Reset holds the PCA9541 in a reset condition until V_{DD} has reached V_{POR}. At this point, the reset condition is released and the internal registers are initialized to their default states, with:

	Default	Stop Detect
PCA9541/01	Channel 0	
PCA9541/02	Channel 0	✓
PCA9541/03	No Channel	

1. PCA9541/01: after power-up and/or insertion of the device in the main I²C-bus, the upstream Channel 0 and the downstream slave channel are connected together.
2. PCA9541/02: after power-up and/or insertion of the device in the main I²C-bus, the upstream Channel 0 and the downstream slave channel are connected together after a STOP condition has been detected by the PCA9541/02 on Channel 0.
   - If the bus was not idle, Channel 0 and the downstream slave device will be connected together as soon as a STOP condition occurs at the conclusion of the transmission sequence on Channel 0.
   - If the bus was idle, then Channel 0 is connected to the downstream slave channel after a STOP condition is detected on Channel 0. This I²C-bus command may or may not be addressed to the PCA9541/02.
   - If a switch to channel 1 (initiated by the master on channel 1) is requested (before or after the default switch to Channel 0 has been performed), the upstream channel 1 is connected to the downstream slave channel when the master located in Channel 1 sends the STOP command.
3. PCA9541/03: after power-up and/or insertion of the device in the main I²C-bus, no channel will be connected to the downstream channel. The device is ready to receive a START condition and its address by a master.

   If either register writes to its Control Register, then the connection between the upstream and the downstream channels is determined by the values on the Control Registers.

Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

EXTERNAL RESET

A reset can be accomplished by holding the $\overline{RESET}$ pin LOW for a minimum of t_w. The PCA9541 registers and I²C state machine will be held in their default states until the $\overline{RESET}$ input is once again HIGH. This input typically requires a pull-up resistor to V_{DD}.

Default states are:

- I²C upstream Channel 0 connected to the I²C downstream channel for the PCA9541/01
- no I²C upstream channel connected to the I²C downstream channel for the PCA9541/02 with Channel 0 connected to the downstream I²C channel after detection of a STOP on the upstream channel.
- no I²C upstream channel connected to the I²C downstream channel for the PCA9541/03.

VOLTAGE TRANSLATION

The pass gate transistors of the PCA9541 are constructed such that the V_{DD} voltage can be used to limit the maximum voltage that will be passed from one I²C-bus to another.

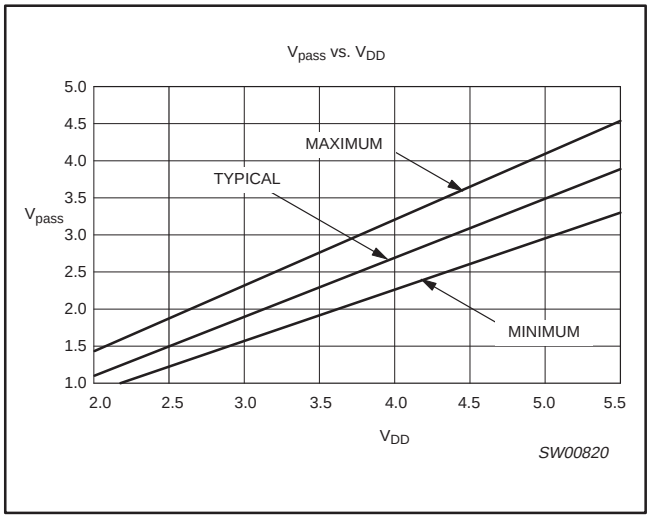


Figure 7. V_{pass} voltage

Figure 7 shows the voltage characteristics of the pass gate transistors (note that the graph was generated using the data specified in the DC Characteristics section of this datasheet). In order for the PCA9541 to act as a voltage translator, the V_{pass} voltage should be equal to, or lower than the lowest bus voltage. For example, if the main buses were running at 5 V, and the downstream bus was 3.3 V, then V_{pass} should be equal to or below 3.3 V to effectively clamp the downstream bus voltages. Looking at Figure 7, we see that V_{pass} (max.) will be at 3.3 V when the PCA9541 supply voltage is 3.5 V or lower so the PCA9541 supply voltage could be set to 3.3 V. Pull-up resistors can then be used to bring the bus voltages to their appropriate levels (see Figure 16).

More Information on voltage translation can be found in Application Note AN262 *PCA954X family of I²C/SMBus multiplexers and switches.*

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see FIgure 8).

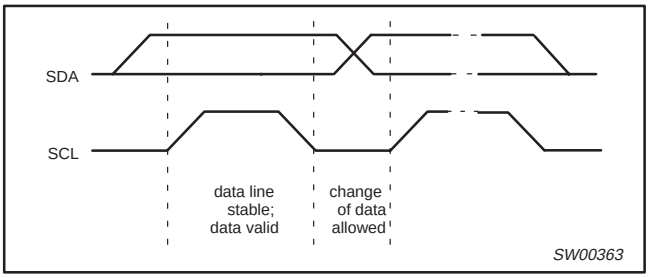


Figure 8. Bit transfer

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P) (see Figure 9).

System configuration

A device generating a message is a transmitter: a device receiving is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves (see Figure 10).

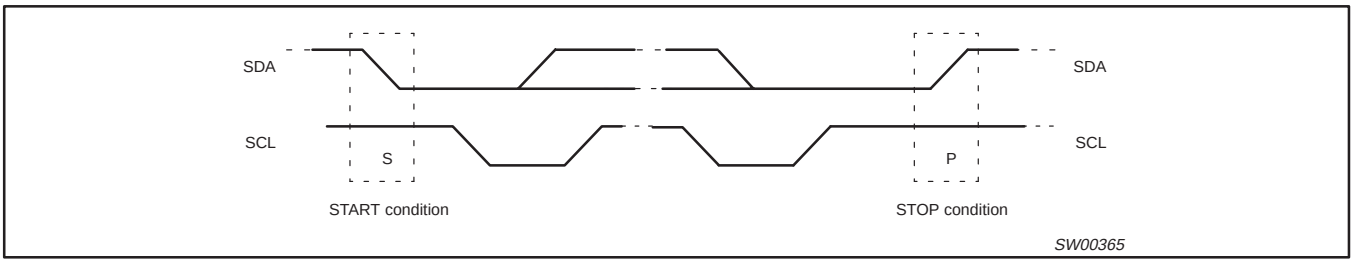


Figure 9. Definition of start and stop conditions

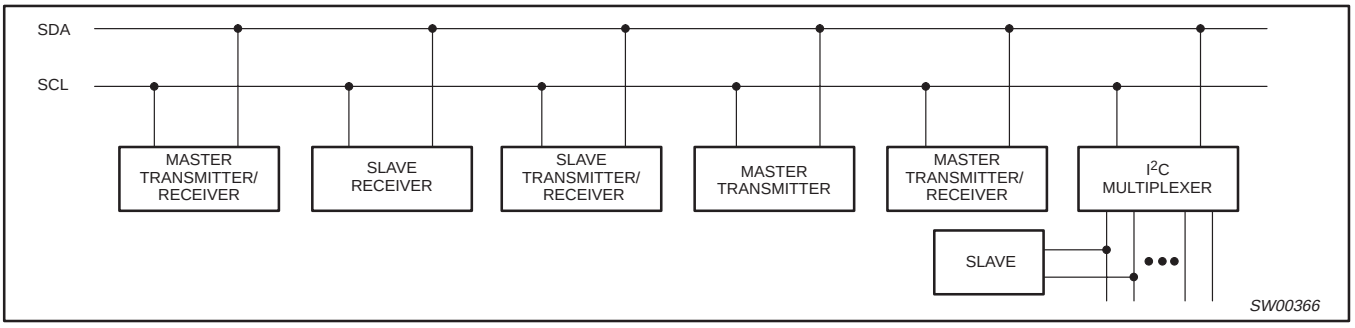


Figure 10. System configuration

Acknowledge

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

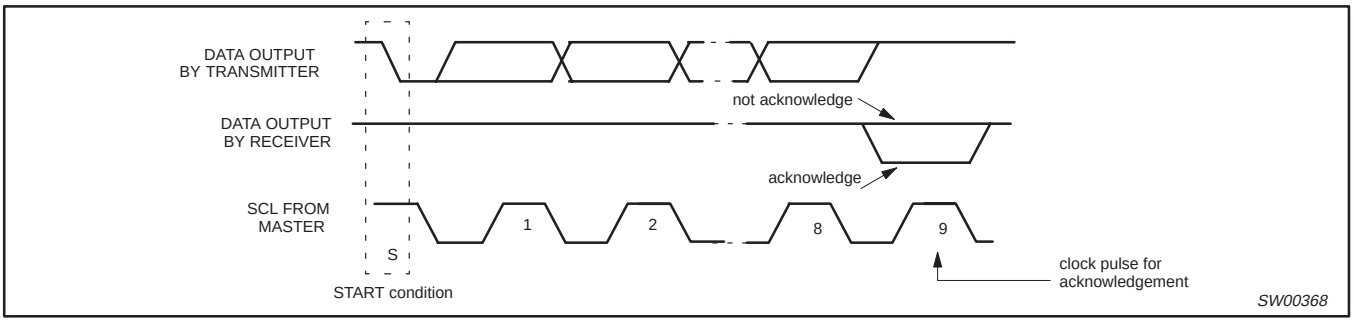


Figure 11. Acknowledgement on the I2C-bus

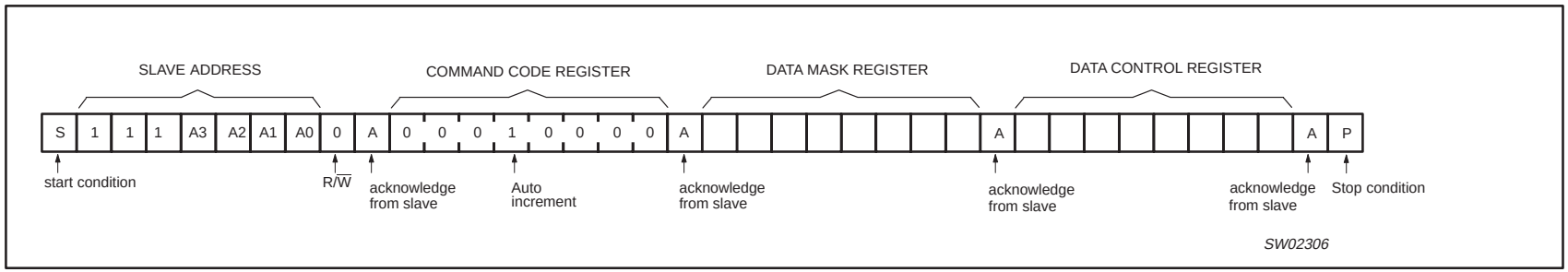


Figure 12. Write to the Mask and Control Registers using the Auto-Increment (AI) bit

NOTE: If a 3rd data byte is sent, it will not be acknowledged by the PCA9541.

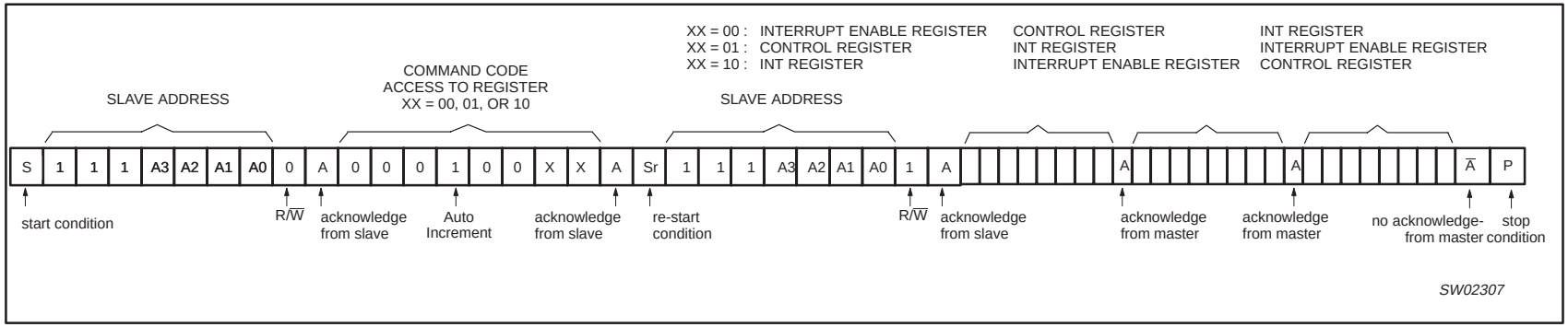


Figure 13. Read the 3 registers using the Auto-Increment (AI) bit

NOTE: If a 4th data byte is read, the first Register will be accessed.

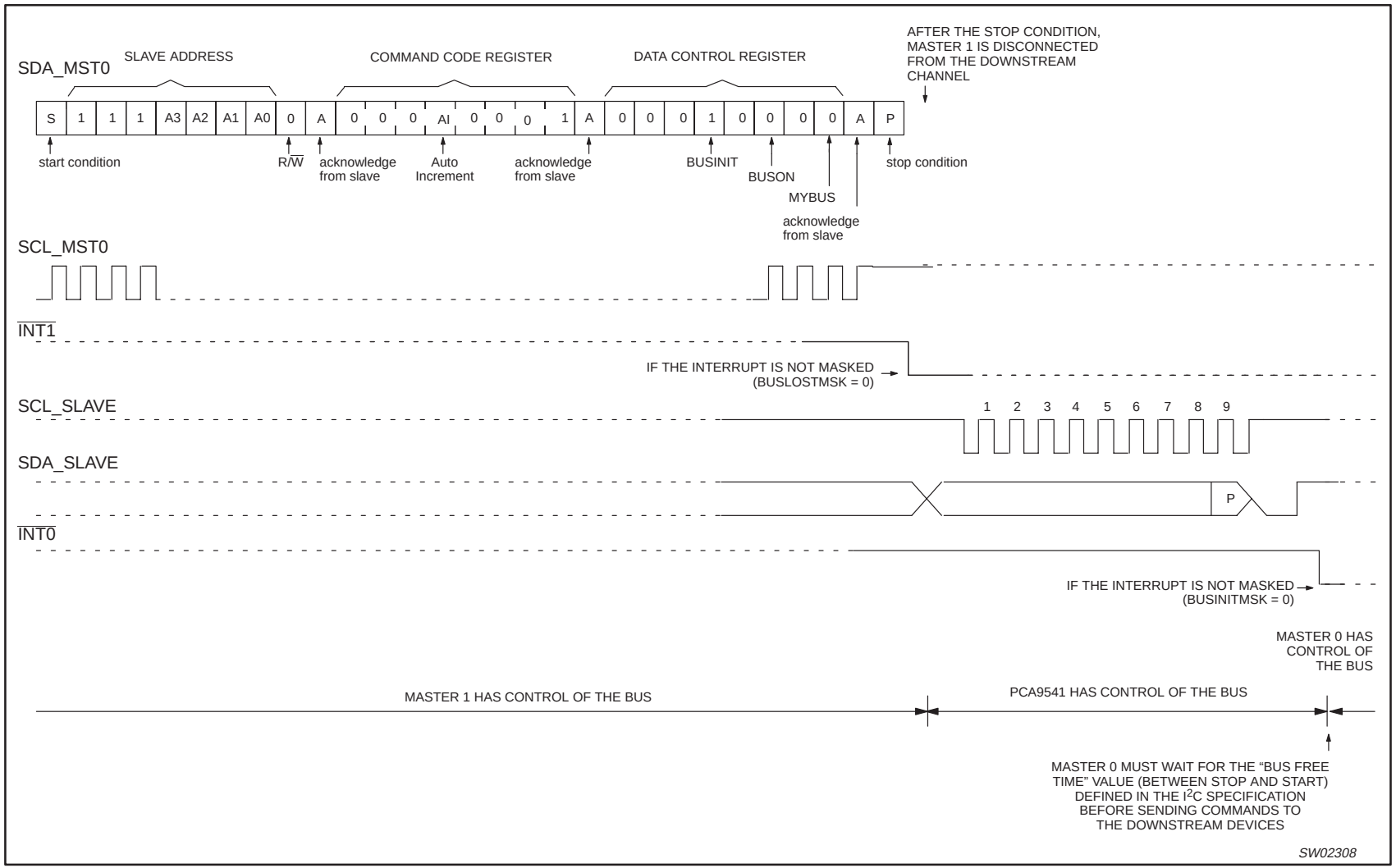


Figure 14. Write to the control register and switch from channel 1 to channel 0 (bus recovery/initialization requested)

NOTE: We assume that a Read of the control register was done by Master 1 and that 000x1010 was read.

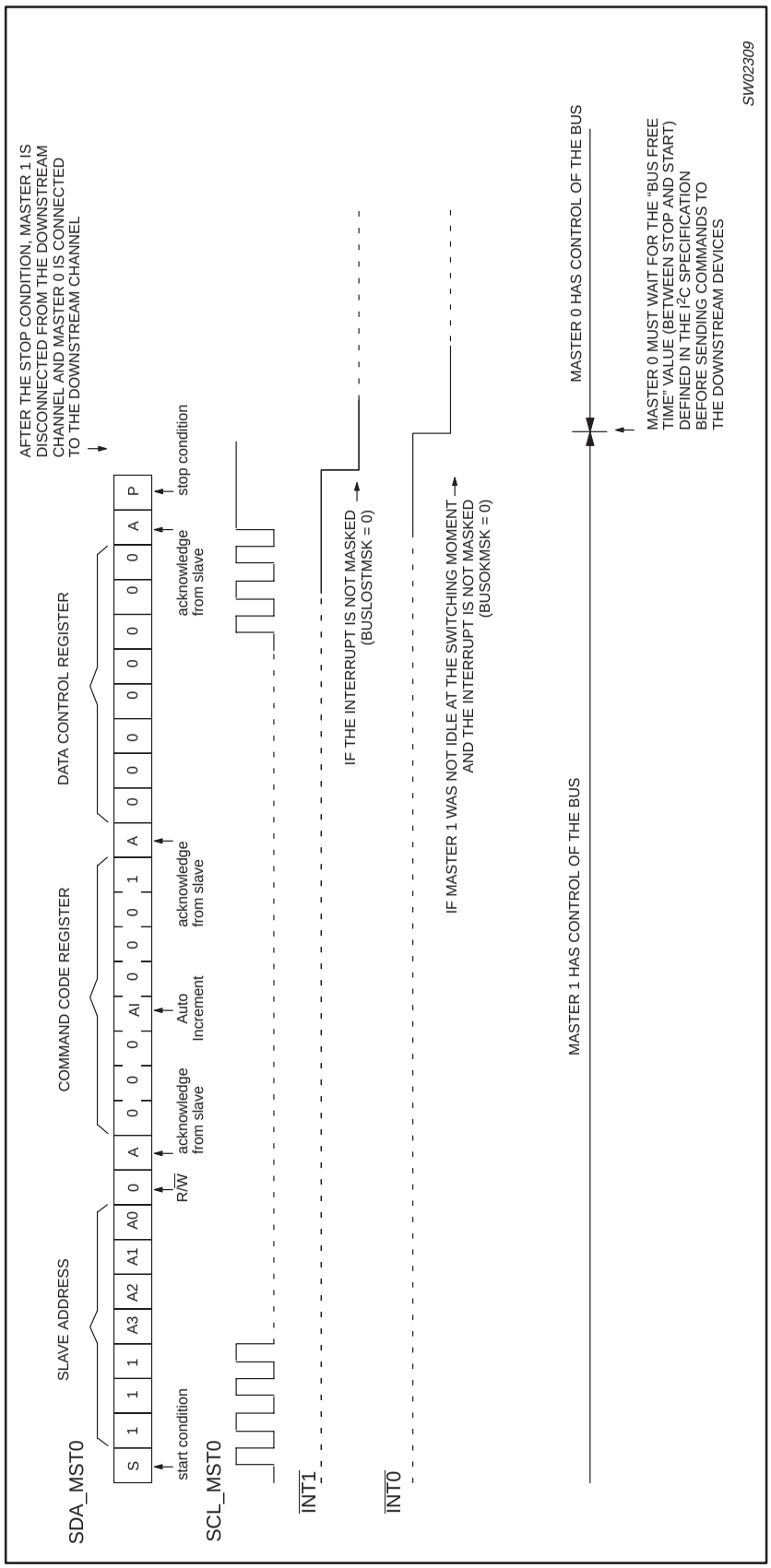


Figure 15. Write to the control register and switch from channel 1 to channel 0 (bus recovery/initialization not requested)

TYPICAL APPLICATION

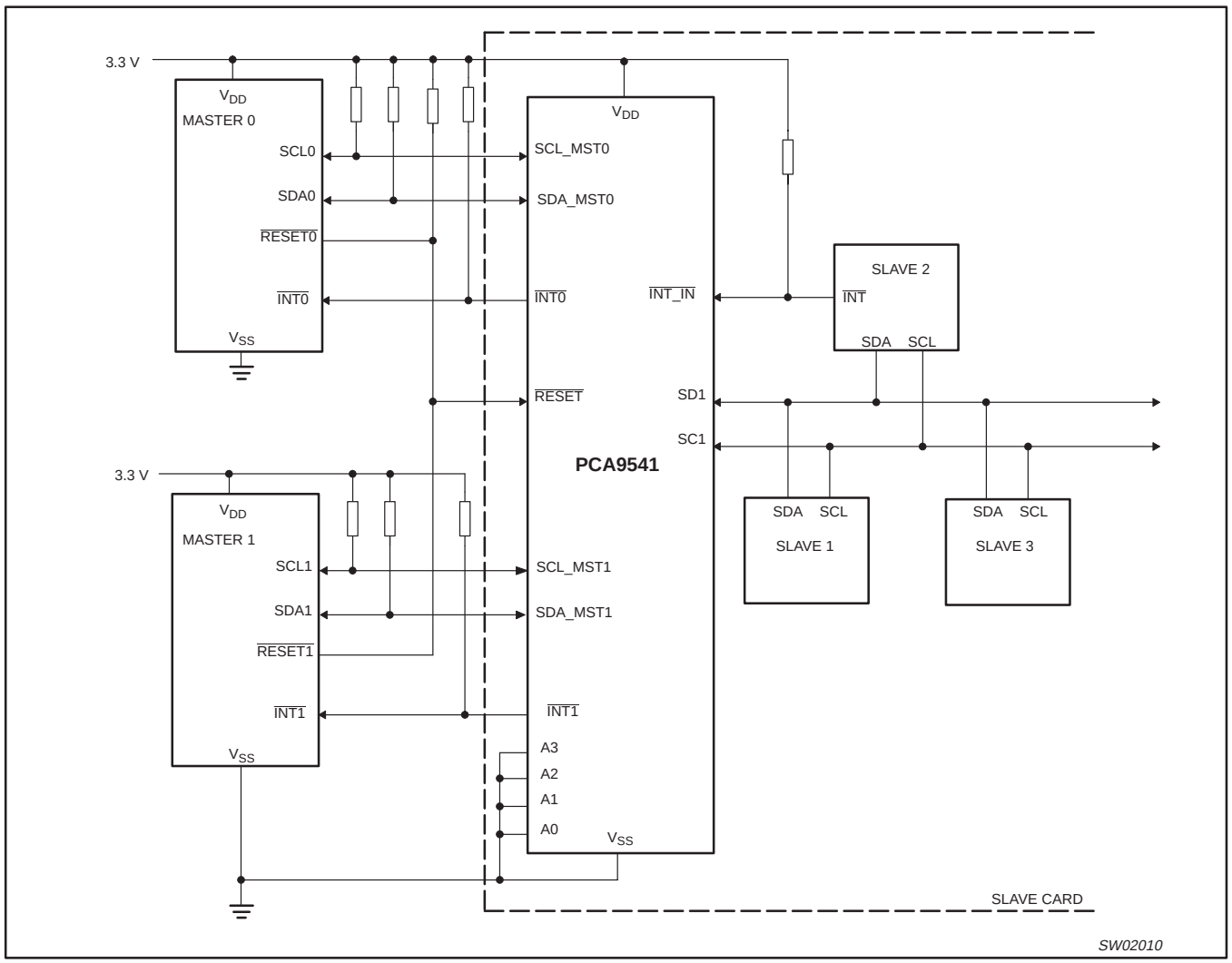


Figure 16. Typical application

SPECIFIC APPLICATIONS

The PCA9541 is a 2-to-1 I²C master selector designed for dual master, high reliability I²C applications, where continuous maintenance and control monitoring is required even if one master fails or its controller card is removed for maintenance. The PCA9541 can also be used in other applications, such as where masters share the same resource but cannot share the same bus, as a gatekeeper multiplexer in long single bus applications or as a bus initialization/recovery device.

HIGH RELIABILITY SYSTEMS

In a typical multi-point application, shown in Figure 17, the two masters (e.g., primary and back-up) are located on separate I²C-buses that connect to multiple downstream I²C-bus slave cards/devices via a PCA9541/01 for non-hot swap applications or the PCA9541/02 for hot swap applications to provide high reliability of the I²C-bus.

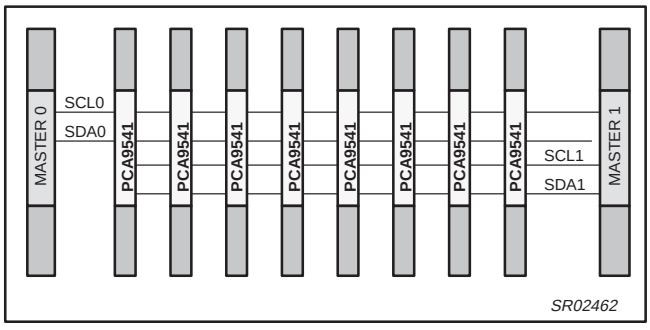


Figure 17. High Reliability Backplane Application

I²C commands are sent via the primary or back-up master and either master can take command of the I²C-bus. Either master at any time can gain control of the slave devices if the other master is disabled or removed from the system. The failed master is isolated from the system and will not affect communication between the on-line master and the slave devices located on the cards.

For even higher reliability in multi-point backplane applications, two dedicated masters can be used for every card as shown in Figure 18.

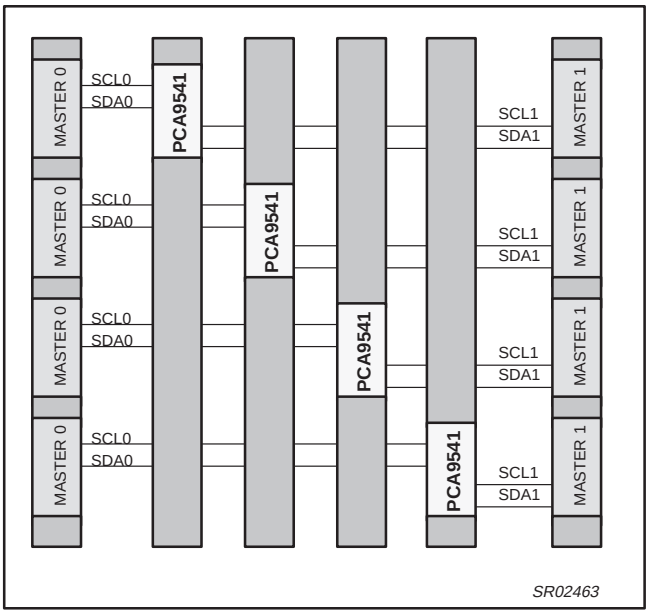


Figure 18. Very High Reliability Backplane Application

MASTERS WITH SHARED RESOURCES

Some masters may not be multi-master capable or some masters may not work well together and continually lock up the bus. The PCA9541 can be used to separate the masters, as shown in Figure 19, but still allow shared access to slave devices, such as Field Replaceable Unit (FRU) EEPROMs or temperature sensors.

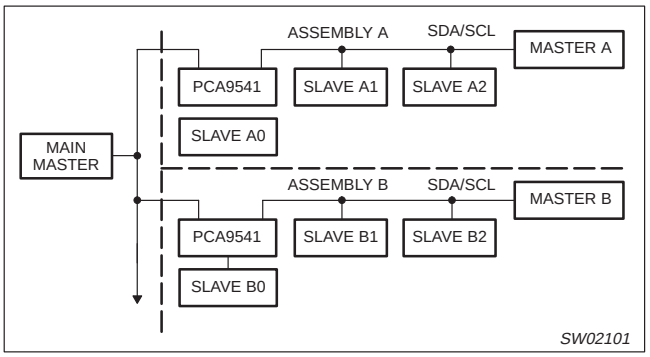


Figure 19. Masters with Shared Resources Application

GATEKEEPER MULTIPLEXER

The PCA9541/03 can act as a gatekeeper multiplexer in applications where there are multiple I²C devices with the same fixed address (e.g., EEPROMs with address of “Z” as shown in Figure 20) connected in a multi-point arrangement to the same I²C-bus. Up to 16 hot swappable cards/devices can be multiplexed to the same bus master by using one PCA9541/03 per card/device. Since each PCA9541/03 has its own unique address (e.g., “A”, “B”, “C”, etc), the EEPROMs can be connected to the master, one at a time, by connecting one PCA9541/03 (Master 0 position) while keeping the rest of the cards/devices isolated (off position).

The alternative, shown with dashed lines, is to use a PCA9548 1-to-8 channel switch on the master card and run 8 I²C-buses, one to each EEPROM card, to multiplex the master to each card. The number of card pins used is the same in either case, but there are 7 less pairs of SDA/SCL traces on the PC board if the PCA9541/03 is used.

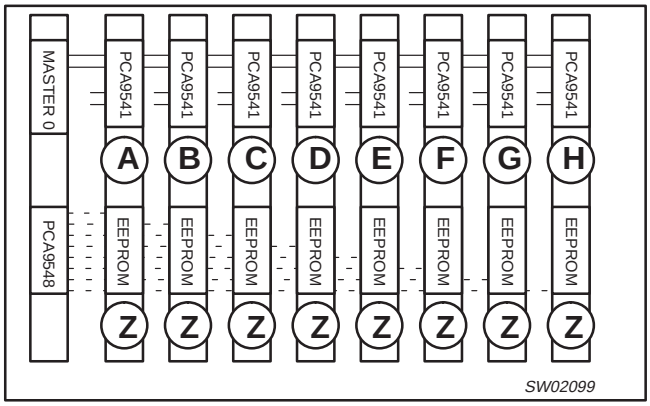


Figure 20. Gatekeeper Multiplexer Application

BUS INITIALIZATION/RECOVERY

If the I²C-bus is hung, I²C devices without a hardware reset pin (e.g., Slave 1 and 2 in Figure 21) can be isolated from the master by the PCA9541/03. The PCA9541/03 disconnects the bus when it is reset via the hardware reset line, restoring the master’s control of the rest of the bus (e.g., Slave 0). The bus master can then command the PCA9541/03 to send 9 clock pulses/ stop condition to reset the downstream I²C devices before they are reconnected to the master or leave the downstream devices isolated.

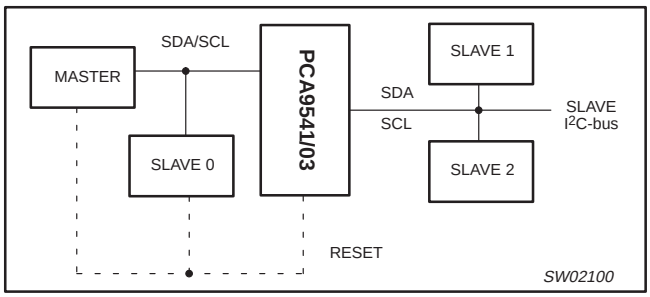


Figure 21. Bus Initialization/Recovery Application

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{DD}	DC supply voltage		–0.5 to +7.0	V
V_I	DC input voltage		–0.5 to +7.0	V
I_I	DC input current		± 20	mA
I_O	DC output current		± 25	mA
I_{DD}	Supply current		± 100	mA
I_{SS}	Supply current		± 100	mA
P_{tot}	total power dissipation		400	mW
T_{stg}	Storage temperature range		–60 to +150	°C
T_{amb}	Operating ambient temperature		–40 to +85	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

DC CHARACTERISTICS

V_{DD} = 2.3 V to 3.6 V; V_{SS} = 0 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified. (See page 21 for V_{DD} = 3.6 V to 5.5 V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Supply						
V_{DD}	Supply voltage		2.3	—	3.6	V
I_{DD}	Supply current	Operating mode; V_{DD} = 3.6 V; no load; $V_I = V_{DD}$ or V_{SS}; f_{SCL} = 100 kHz	—	152	200	µA
I_{stb}	Standby current	Standby mode; V_{DD} = 3.6 V; no load; $V_I = V_{DD}$ or V_{SS}; f_{SCL} = 0 kHz	—	10	100	µA
V_{POR}	Power-on reset voltage (Note 1)	no load; $V_I = V_{DD}$ or V_{SS}	—	1.5	2.1	V
Input SCL; input/output SDA (upstream and downstream channels)						
V_{IL}	LOW-level input voltage		–0.5	—	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	—	6	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	—	—	mA
		V_{OL} = 0.6 V	6	—	—	
I_L	Leakage current	$V_I = V_{DD}$ or V_{SS}	–1	—	+1	µA
C_i	Input capacitance	$V_I = V_{SS}$	—	4	5	pF
Select inputs A0 to A3 / $\overline{INT\_IN}$ / $\overline{RESET}$						
V_{IL}	LOW-level input voltage		–0.5	—	$+0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	—	6	V
I_{LI}	Input leakage current	$V_I = V_{DD}$ or V_{SS}	–1	—	+1	µA
C_i	Input capacitance	$V_I = V_{SS}$	—	2	3	pF
Pass Gate						
R_{ON}	Switch resistance	V_{CC} = 3.0 V to 3.6 V, V_O = 0.4 V, I_O = 15 mA	5	14	30	Ω
		V_{CC} = 2.3 V to 2.7 V, V_O = 0.4 V, I_O = 10 mA	7	17	55	
V_{Pass}	Switch output voltage	$V_{swin} = V_{DD}$ = 3.3 V; I_{swout} = –100 µA	—	2.2	—	V
		$V_{swin} = V_{DD}$ = 3.0 V to 3.6 V; I_{swout} = –100 µA	1.6	—	2.8	
		$V_{swin} = V_{DD}$ = 2.5 V; I_{swout} = –100 µA	—	1.5	—	
		$V_{swin} = V_{DD}$ = 2.3 V to 2.7 V; I_{swout} = –100 µA	1.1	—	2.0	
I_L	Leakage current	$V_I = V_{DD}$ or V_{SS}	–1	—	+1	µA
$\overline{INT0}$ and $\overline{INT1}$ outputs						
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	—	—	mA

NOTE:
1. V_{DD} must be lowered to 0.2 V in order to reset part.

DC CHARACTERISTICS

V_{DD} = 3.6 V to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified. (See page 20 for V_{DD} = 2.3 V to 3.6 V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Supply						
V_{DD}	Supply voltage		3.6	—	5.5	V
I_{DD}	Supply current	Operating mode; V_{DD} = 5.5 V; no load; V_I = V_{DD} or V_{SS}; f_{SCL} = 100 kHz	—	349	600	µA
I_{stb}	Standby current	Standby mode; V_{DD} = 5.5 V; no load; V_I = V_{DD} or V_{SS}; f_{SCL} = 0 kHz	—	10	200	µA
V_{POR}	Power-on reset voltage (Note 1)	no load; V_I = V_{DD} or V_{SS}	—	1.5	2.1	V
Input SCL; input/output SDA (upstream and downstream channels)						
V_{IL}	LOW-level input voltage		–0.5	—	0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	—	6	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	—	—	mA
		V_{OL} = 0.6 V	6	—	—	mA
I_{IL}	LOW-level input current	V_I = V_{SS}	–10	—	10	µA
I_{IH}	HIGH-level input current	V_I = V_{DD}	—	—	100	µA
C_i	Input capacitance	V_I = V_{SS}	—	4	6	pF
Select inputs A0 to A3 / $\overline{\text{INT\_IN}}$ / $\overline{\text{RESET}}$						
V_{IL}	LOW-level input voltage		–0.5	—	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	—	6	V
I_{LI}	Input leakage current	V_I = V_{DD} or V_{SS}	–1	—	+50	µA
C_i	Input capacitance	V_I = V_{SS}	—	2	5	pF
Pass Gate						
R_{ON}	Switch resistance	V_{CC} = 4.5 V to 5.5 V; V_O = 0.4 V; I_O = 15 mA	4	12	24	Ω
V_{Pass}	Switch output voltage	V_{swin} = V_{DD} = 5.0 V; I_{swout} = –100 µA	—	3.6	—	V
		V_{swin} = V_{DD} = 4.5 to 5.5 V; I_{swout} = –100 µA	2.6	—	4.5	V
I_L	Leakage current	V_I = V_{DD} or V_{SS}	–1	—	+100	µA
$\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ outputs						
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	—	—	mA

NOTE:
1. V_{DD} must be lowered to 0.2 V in order to reset part.

AC CHARACTERISTICS

SYMBOL	PARAMETER	STANDARD-MODE I²C-bus		FAST-MODE I²C-bus		UNIT
		MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay from SDA to SD_n or SCL to SC_n	—	0.3[1]	—	0.3[1]	ns
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
f_{SCLIR}	SCL bus initialization/recovery clock frequency	50	150	50	150	kHz
t_{BUF}	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
$t_{HD;STA}$	Hold time (repeated) START condition After this period, the first clock pulse is generated	4.0	—	0.6	—	µs
t_{LOW}	LOW period of the SCL clock	4.7	—	1.3	—	µs
t_{HIGH}	HIGH period of the SCL clock	4.0	—	0.6	—	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
$t_{SU;STO}$	Set-up time for STOP condition	4.0	—	0.6	—	µs
$t_{HD;DAT}$	Data hold time	0[2]	3.45	0[2]	0.9	µs
$t_{SU;DAT}$	Data set-up time	250	—	100	—	ns
t_R	Rise time of both SDA and SCL signals	—	1000	$20 + 0.1C_b$[3]	300	ns
t_F	Fall time of both SDA and SCL signals	—	300	$20 + 0.1C_b$[3]	300	µs
C_b	Capacitive load for each bus line	—	400	—	400	µs
t_{SP}	Pulse width of spikes which must be suppressed by the input filter	—	50	—	50	ns
$t_{VD:DATL}$	Data valid (HL)[4]	—	1	—	1	µs
$t_{VD:DATH}$	Data valid (LH)[4]	—	0.6	—	0.6	µs
$t_{VD:ACK}$	Data valid Acknowledge	—	1	—	1	µs
$\overline{INT0}$ and $\overline{INT1}$ outputs						
t_{iv}	$\overline{INT\_in}$ to $\overline{INT1}$ or $\overline{INT2}$ active valid time	—	4	—	4	µs
t_{ir}	$\overline{INT\_in}$ to $\overline{IINT1}$ or $\overline{INT2}$ inactive delay time	—	2	—	2	µs
L_{pwr}	LOW level pulse width rejection or $\overline{INT\_in}$ input	1	—	1	—	ns
H_{pwr}	HIGH level pulse width rejection or $\overline{INT\_in}$ input	0.5	—	0.5	—	µs
$\overline{RESET}$						
t_W	Pulse width LOW reset	4	—	4	—	ns
t_{rst}	Reset time (SDA clear)	500	—	500	—	ns
$t_{REC:STA}$	Recovery to Start[5, 6]	0	—	0	—	ns

NOTES:
1. Pass gate propagation delay is calculated from the 20 Ω typical R_{ON} and the 15 pF load capacitance.
2. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH(min)}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
3. C_b = total capacitance of one bus line in pF.
4. Measurements taken with 1 kΩ pull-up resistor and 50 pF load.
5. Resetting the device while actively communicating on the bus may cause glitches or errant STOP conditions.
6. Upon reset, the full delay will be the sum of t_{RESET} and the RC time constant of the SDA bus.

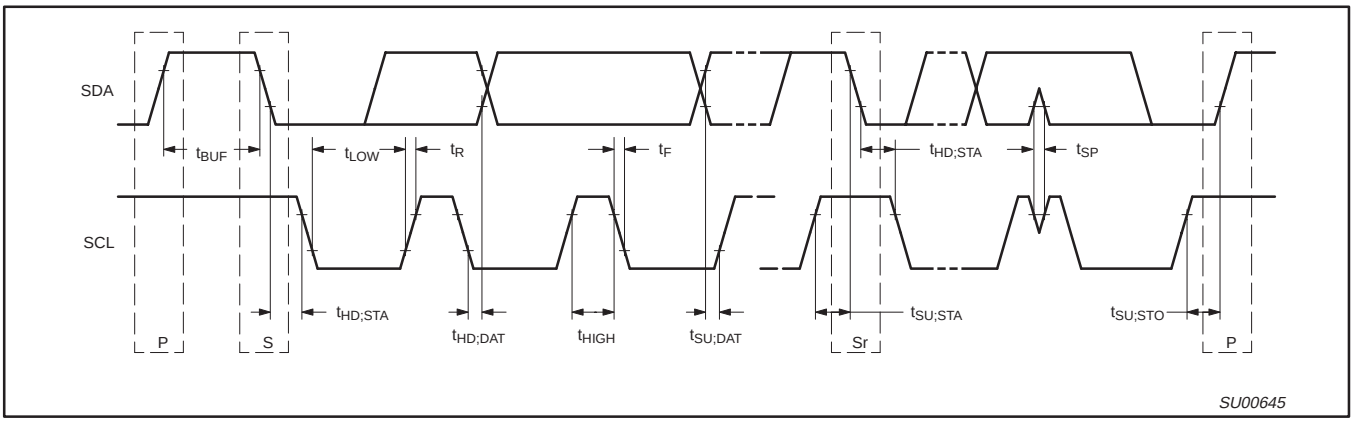


Figure 22. Definition of timing on the I²C-bus

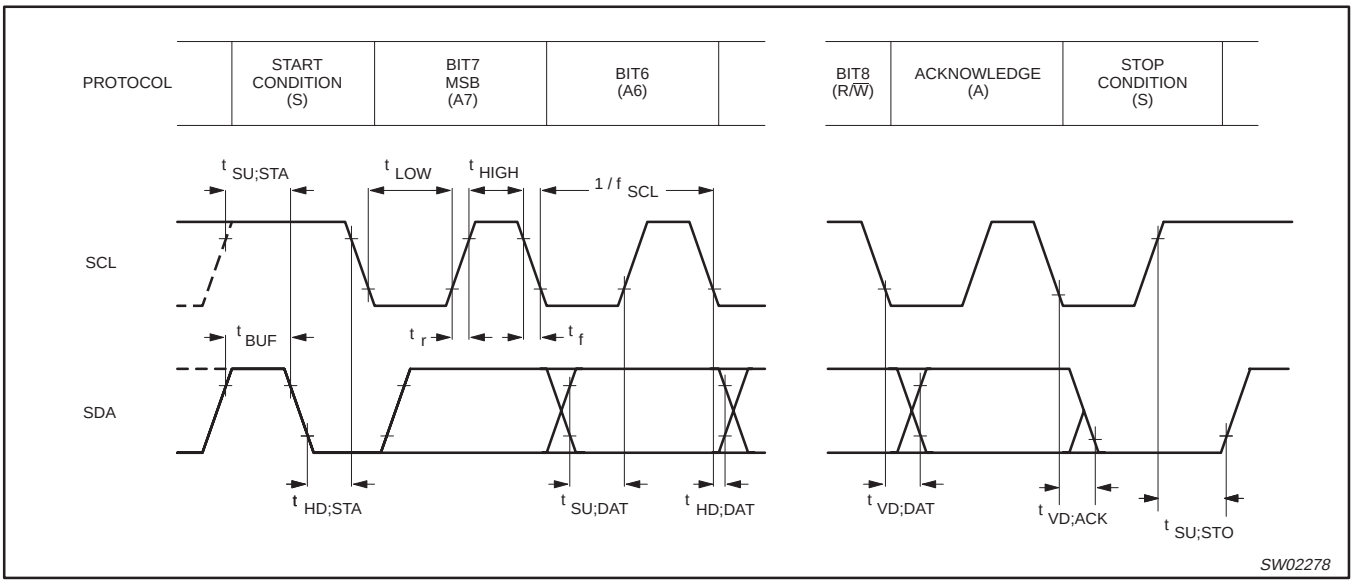


Figure 23. I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}

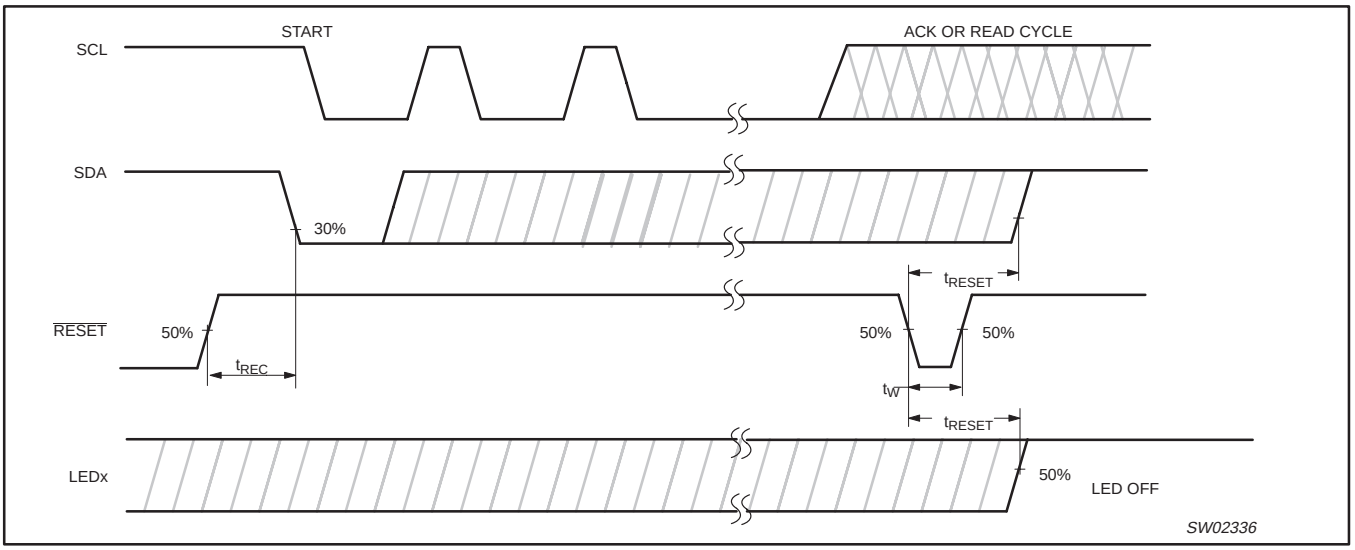
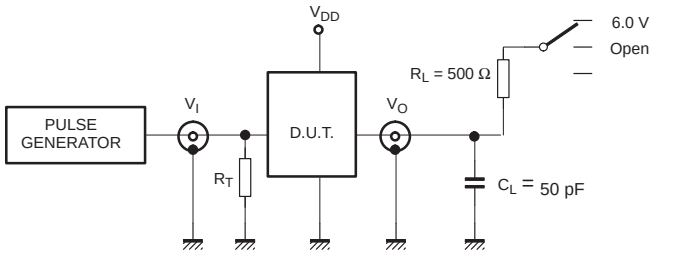


Figure 24. Definition of $\overline{\text{RESET}}$ timing



DEFINITIONS

R_L = Load resistor.

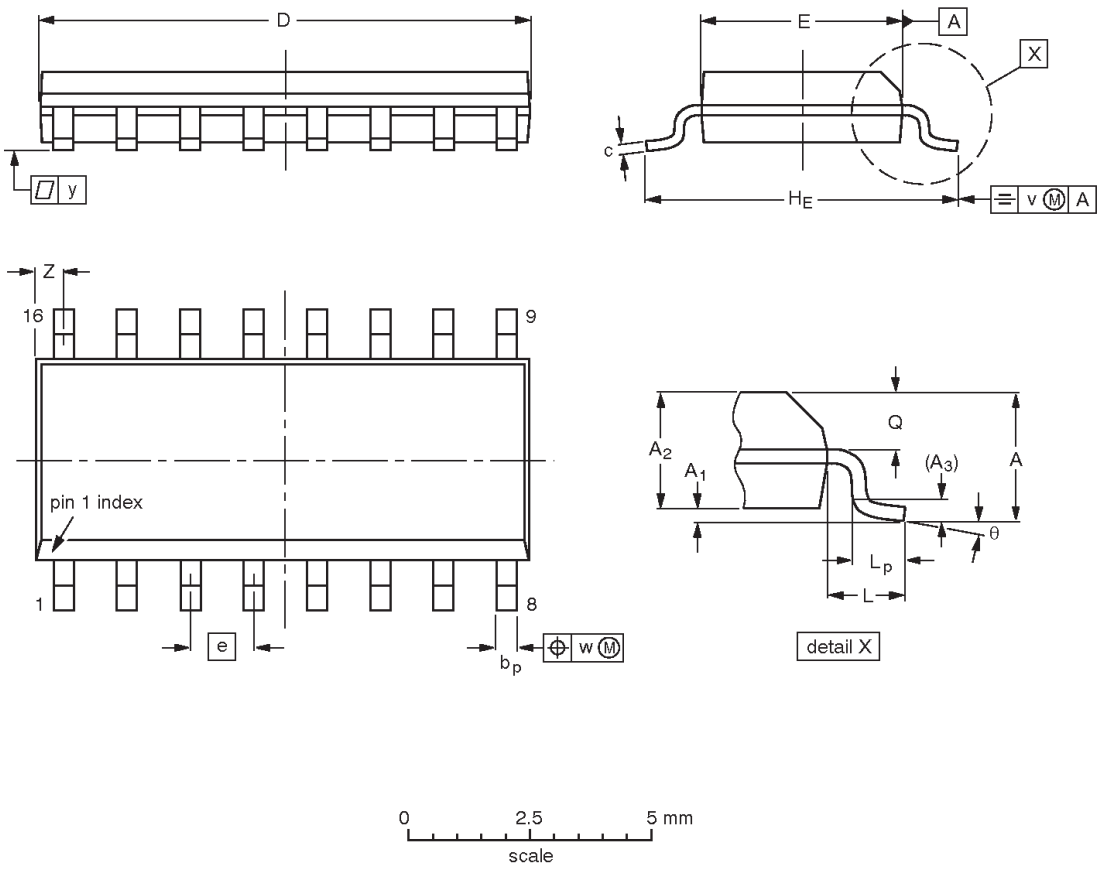
C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to the output impedance Z_O of the pulse generators.

SW02279

Figure 25. Test circuitry for switching times

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

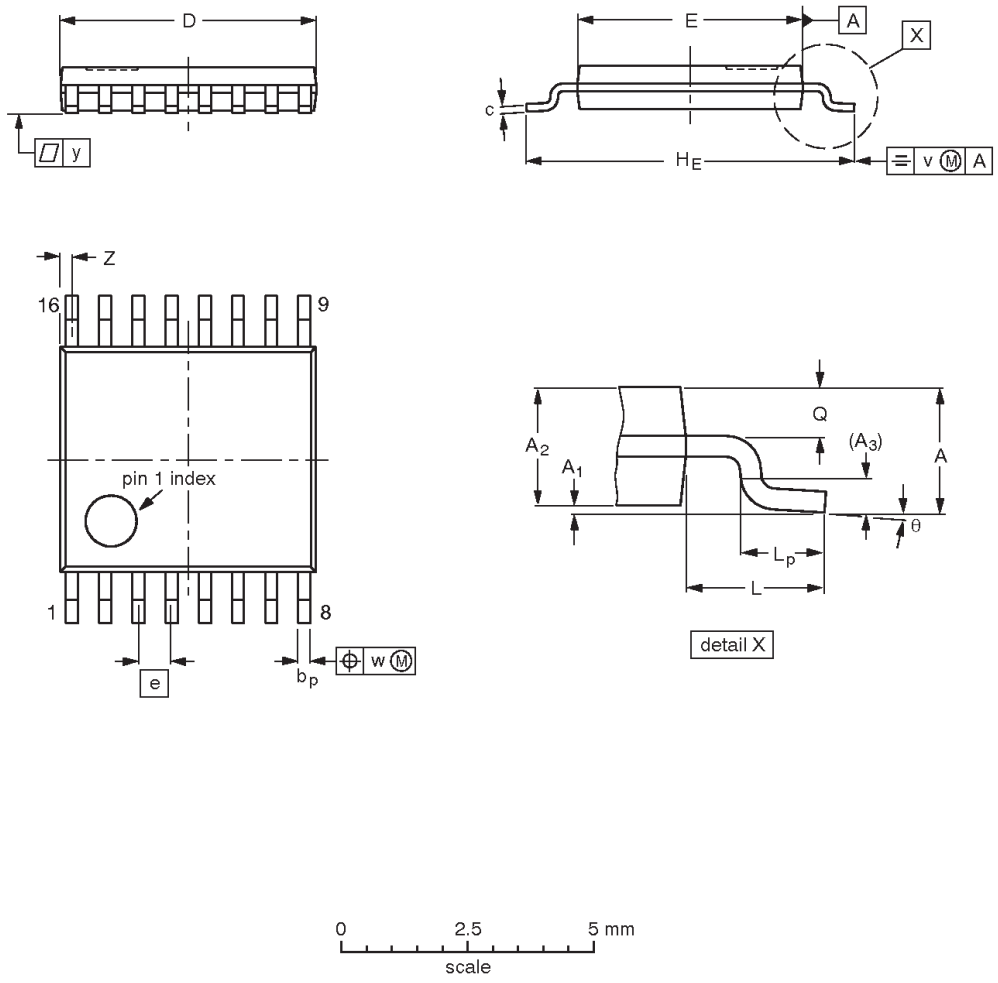
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

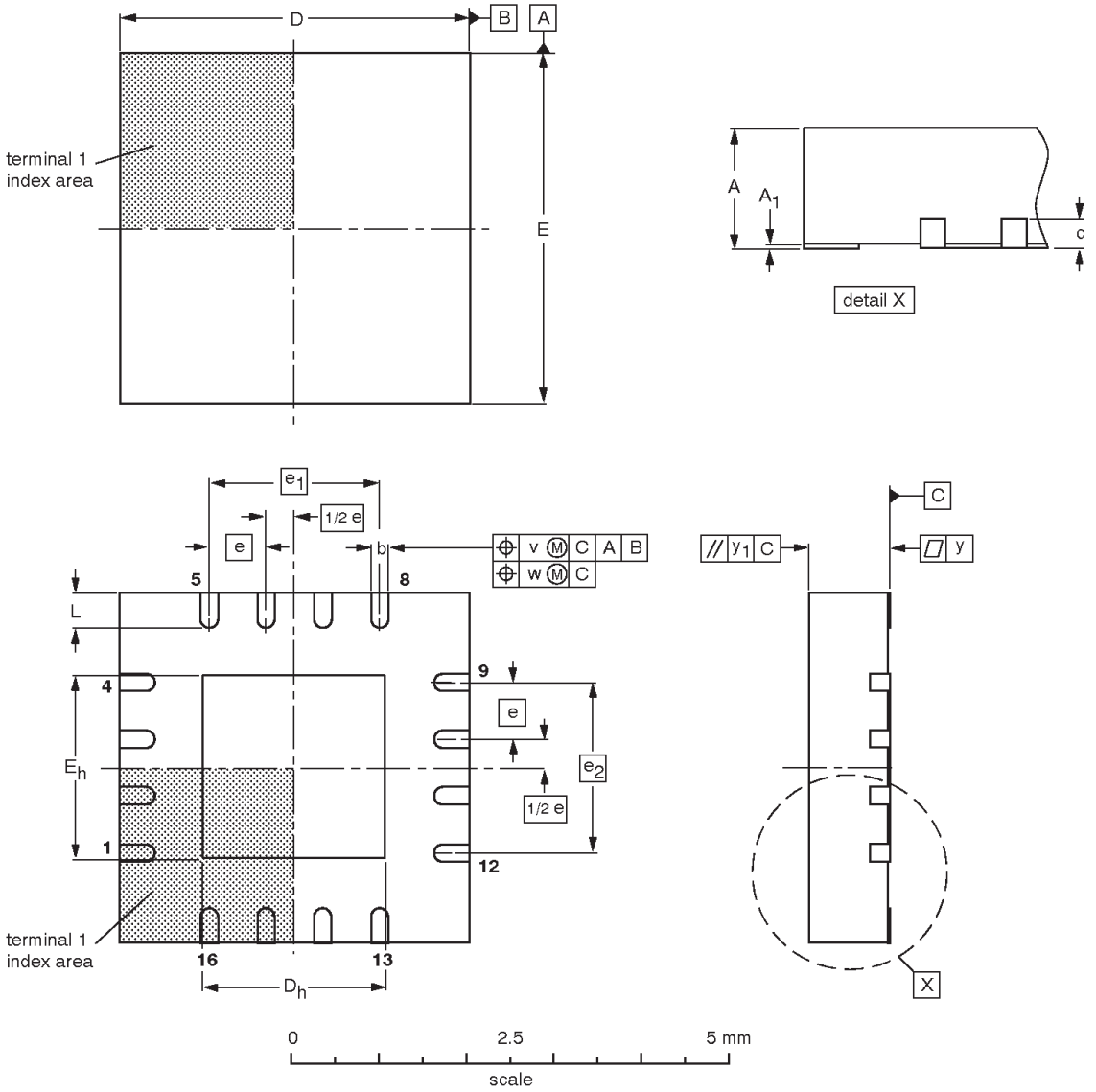
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 4 x 4 x 0.85 mm **SOT629-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1
mm	1	0.05 0.00	0.38 0.23	0.2	4.1 3.9	2.25 1.95	4.1 3.9	2.25 1.95	0.65	1.95	1.95	0.75 0.50	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT629-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

REVISION HISTORY

Rev	Date	Description
_2	20041001	**Product data (9397 750 13629); supersedes data of 02 December 2003 (9397 750 12453).** Modifications: ● Table 7 and its description added to page 10. ● "Power-On Reset" section on page 13: – first sentence: change **from** "... in a reset state until V_{DD} has reached V_{POR}." **to** " ... in a reset condition until V_{DD} has reached V_{POR}." – Add last sentence in section. ● Add Note 1 to DC Characteristics tables on pages 20 and 21, and reference to it at parameter V_{POR}. ● AC characterists table on page 22: – Add Note 4 and references to it at parameters $t_{VD;DATL}$ and $t_{VD;DATH}$. – Add Notes 5 and 6 and references to them at parameter $t_{REC:STA}$ ● Add (new) Figure 24, 'Definition of $\overline{\text{RESET}}$ timing'.
_1	20031202	**Product data (9397 750 12453); ECN 853-2436 01-A14594 dated 11 November 2003.**

2-to-1 I²C demultiplexer with interrupt logic and reset PCA9541

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

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