SRM20V100LLMX7

CMOS 1 M-BIT STATIC RAM

- **Low Supply Voltage**
- **Wide Temperature Range**
- **Low Supply Current**
- **Access Time 70ns (2.7V)**
- **131,072 Words × 8-Bit Asynchronous**

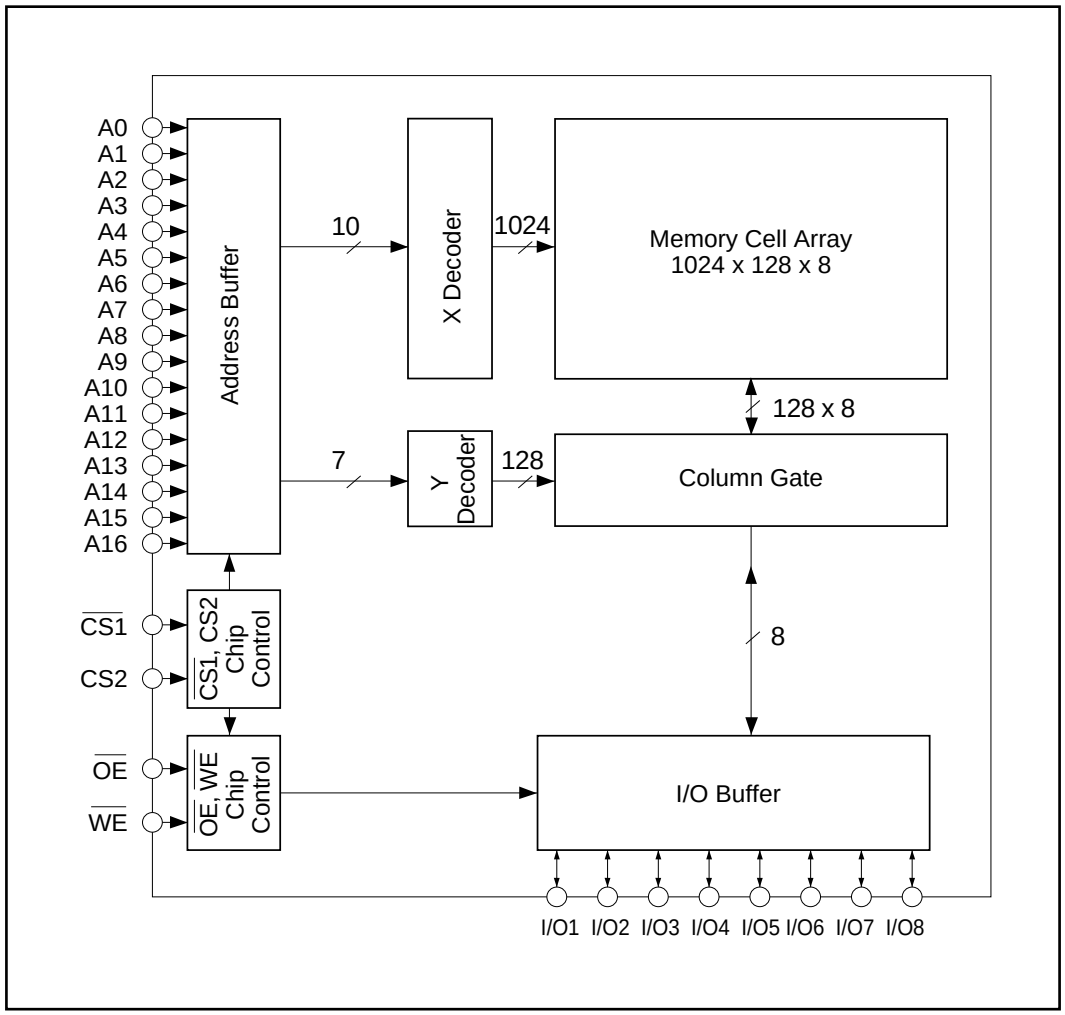
■ DESCRIPTION

The SRM20V100LLMX7 is a 131,072 words × 8-bit asynchronous, static, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The –25 to 85°C operating temperature range makes it ideal for portable equipment. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible and 3-state output allows easy expansion of memory capacity.

■ FEATURES

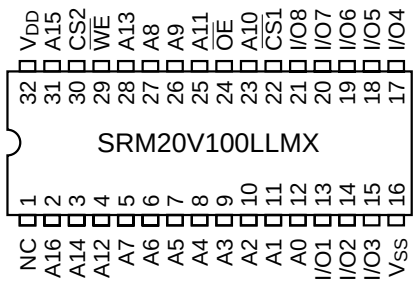
- Wide temperature range . . . . . –25 to 85°C
- Fast Access time. . . . . SRM20V100LLMX7 . . . . . 70ns (Max.)
- Low supply current . . . . . Standby: . . . . . 0.6 μA (Typ.)
  Operation: . . . . . 8mA/1MHz (Typ.)
- Completely static. . . . . No clock required
- Supply voltage . . . . . 2.7V to 3.6V
- TTL compatible inputs and outputs
- 3-state output with wired-OR capability
- Non-volatile storage with back-up batteries
- Package . . . . . SRM20V100LLMX7 . . . . . SOP6-32pin (plastic)
  SRM20V100LLTX7 . . . . . TSOP (I)-32pin (plastic)
  SRM20V100LLRX7 . . . . . TSOP (I)-32pin-R1 (plastic)

■ **BLOCK DIAGRAM**

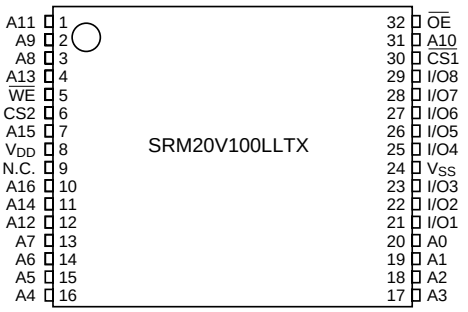


■ PIN CONFIGURATION

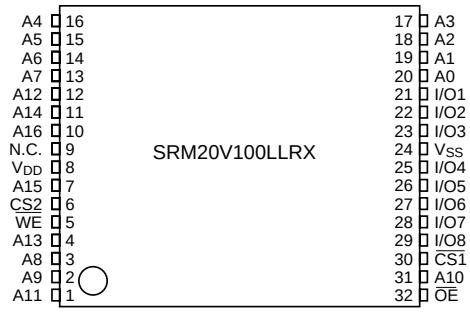
(SOP6)



(TSOP)



(TSOP6-R1)



■ PIN DESCRIPTION

A0 to A16	Address input
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS1}$, CS2	Chip Select
I/O1 to I/O8	Data I/O
V_{DD}	Power Supply (2.7V to 3.6V)
V_{SS}	Power Supply (0V)
N.C.	No Connection

■ ABSOLUTE MAXIMUM RATINGS

V_{SS} = 0V

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	–0.5 to 4.6	V
Input voltage	V_I	–0.5 to V_{DD} + 0.3	V
Input/output voltage	$V_{I/O}$	–0.5 to V_{DD} + 0.3	V
Power dissipation	P_D	0.5	W
Operating temperature	T_{OPR}	–25 to 85	°C
Storage temperature	T_{STG}	–65 to 150	°C
Soldering temperature and time	T_{SOL}	260°C, 10s (Lead only)	—

Note: V_I, $V_{I/O}$ (Min.) = –3.0V (pulse width is 50ns)

■ DC RECOMMENDED OPERATING CONDITIONS

V_{SS} = 0V, T_a = –25 to 85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	—	2.7	3.0	3.6	V
	V_{SS}	—	0	0	0	V
Input voltage	V_{IH}	—	2.2	—	V_{DD} + 0.3	V
	V_{IL}	—	–0.3*	—	0.4	V

* If pulse width is less than 50ns, it is –3.0V

■ ELECTRICAL CHARACTERISTICS

● DC Electrical Characteristics

(V_{DD} = 2.7 to 3.6V, V_{SS} = 0V, T_a = –25 to 85°C)

Parameter	Symbol	Conditions	SRM20V100LLMX7			Unit
			Min	Typ*	Max	
Input leakage	I_{LI}	V_I = 0 to V_{DD}	–1	—	1	µA
Output leakage	I_{LO}	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0 to V_{DD}	–1	—	1	µA
Standby supply current	I_{DDS}	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL}	—	—	1.0	mA
	I_{DDS1}	$\overline{CS1}$ = CS2 ≥ V_{DD} – 0.2V or CS2 ≤ 0.2V	—	0.6	60	µA
Average operating current	I_{DDA}	V_I = V_{IL}, V_{IH} $I_{I/O}$ = 0mA, t_{CYC} = Min	—	20	35	mA
	I_{DDA}1	V_I = V_{IL}, V_{IH} $I_{I/O}$ = 0mA, t_{CYC} = 1µs	—	8	15	mA
Operating supply current	I_{DDO}	V_I = V_{IL}, V_{IH} I_{LO} = 0mA	—	8	15	mA
High level output voltage	V_{OH}	V_{DD} ≥ 3V, I_{OH} = –2.0mA	2.4	—	—	V
		I_{OH} = –100µA,	V_{DD}–0.2	—	—	
Low level output voltage	V_{OL}	V_{DD} ≥ 3V, I_{OL} = –2.0mA	—	—	0.4	V
		I_{OL} = 100µA	—	—	0.2	

*1 Typical values are measured at T_a = 25°C and V_{DD} = 3.0V

● Terminal Capacitance

(f = 1MHz, T_a = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address capacitance	C_{ADD}	V_{ADD} = 0V	—	—	8	pF
Input capacitance	C_I	V_I = 0V	—	—	8	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	—	10	pF

- **AC Electrical Characteristics**
  - **Read Cycle**

V_{DD} = 2.7V to 3.6V, V_{SS} = 0V, T_a = –25 to 85°C

Parameter	Symbol	Conditions	SRM20V100LLMX7		Unit
			Min.	Max.	
Read cycle time	t_{RC}	*1	70	—	ns
Address access time	t_{ACC}		—	70	ns
Chip select1 access time	t_{ACS1}		—	70	ns
Chip select2 access time	t_{ACS2}		—	70	ns
Output enable access time	t_{OE}		—	40	ns
Chip select1 output set time	t_{CLZ1}	*2	5	—	ns
Chip select1 output floating	t_{CHZ1}		—	30	ns
Chip select2 output set time	t_{CLZ2}		5	—	ns
Chip select2 output floating	t_{CHZ2}		—	30	ns
Output enable output set time	t_{OLZ}		0	—	ns
Output enable output floating	t_{OHZ}		—	30	ns
Output hold time	t_{OH}	*1	10	—	ns

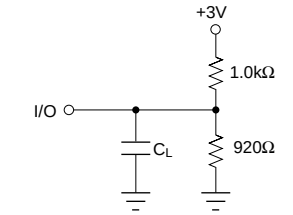
- **Write Cycle**

V_{DD} = 2.7V to 3.6V, V_{SS} = 0V, T_a = –25 to 85°C

Parameter	Symbol	Conditions	SRM20V100LLMX7		Unit
			Min.	Max.	
Write cycle time	t_{WC}	*1	70	—	nS
Chip Select time1	t_{CW1}		60	—	nS
Chip Select time2	t_{CW2}		60	—	nS
Address enable	t_{AW}		60	—	nS
Address setup time	t_{AS}		0	—	nS
Write pulse width	t_{WP}		55	—	nS
Address hold time	t_{WR}		0	—	nS
Input data setup time	t_{DW}		30	—	nS
Input data hold time	t_{DH}		0	—	nS
$\overline{WE}$ output floating	t_{WHZ}	*2	—	30	nS
$\overline{WE}$ output setup time	t_{OW}		5	—	nS

***1. Test Conditions**

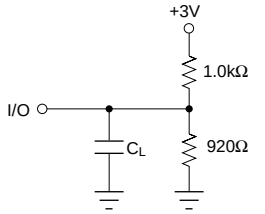
1. Input pulse level: 0.4V to 2.4V
2. tr = tr = 5ns
3. Input and output timing reference levels : 1.5V
4. Output load CL = 100pF



C_L=100pF (Includes Jig Capacitance)

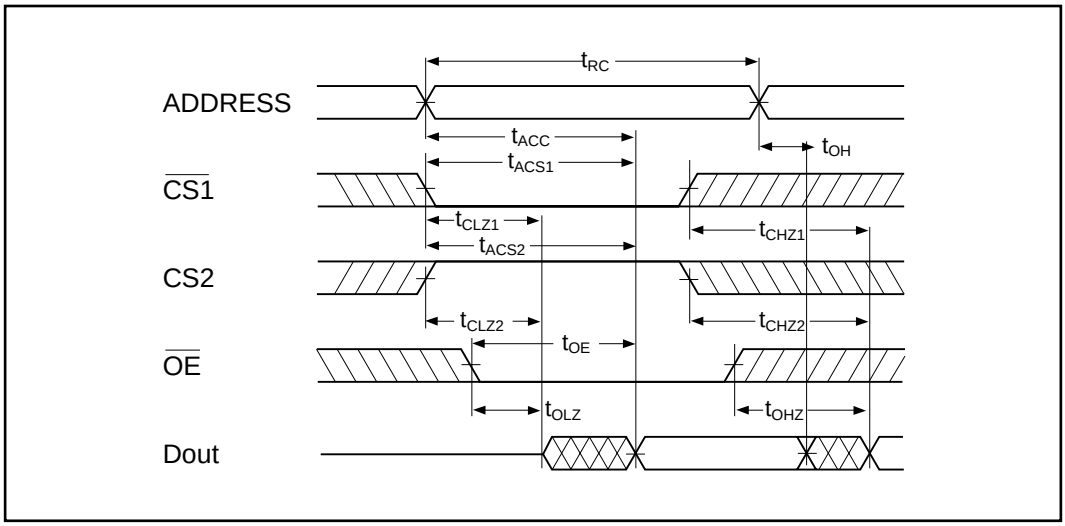
***2. Test Conditions**

1. Input pulse level: 0.4V to 2.4V
2. tr = tr = 5ns
3. Input timing reference levels : 1.5V
4. Output timing reference levels: ± 200mV (the level displaced from stable output voltage level)
5. Output load CL = 5pF



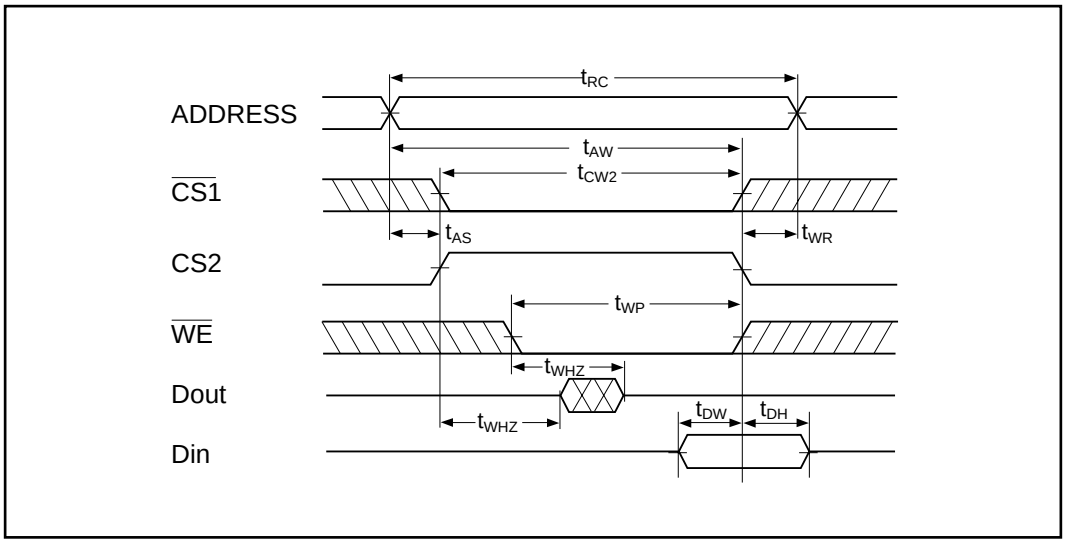
C_L=5pF (Includes Jig Capacitance)

- **Timing Charts**
  - **Read Cycle*1**



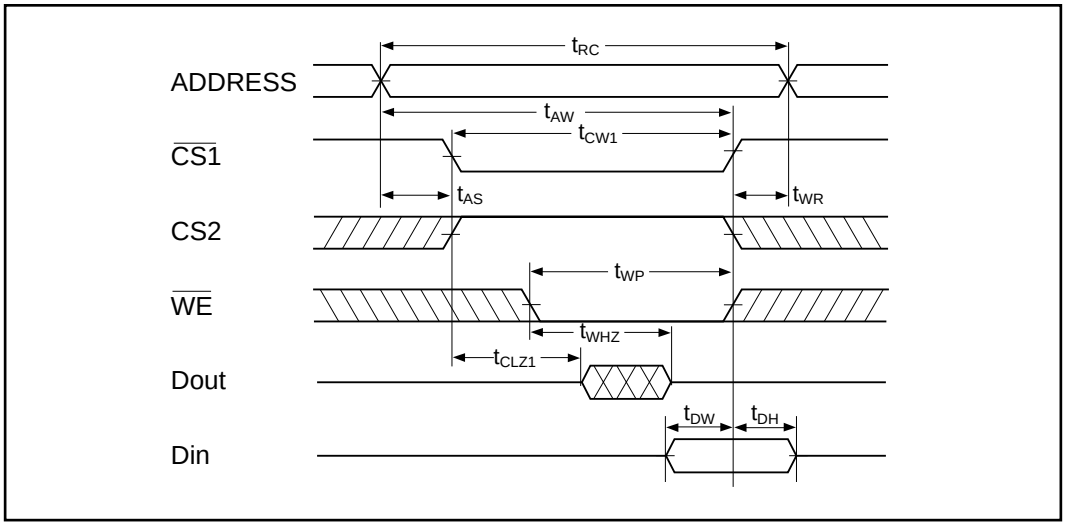
Note: *1. During the read cycle, $\overline{WE}$ must be “H”.

  - **Write Cycle (1) ($\overline{CS1}$ Control)*2**



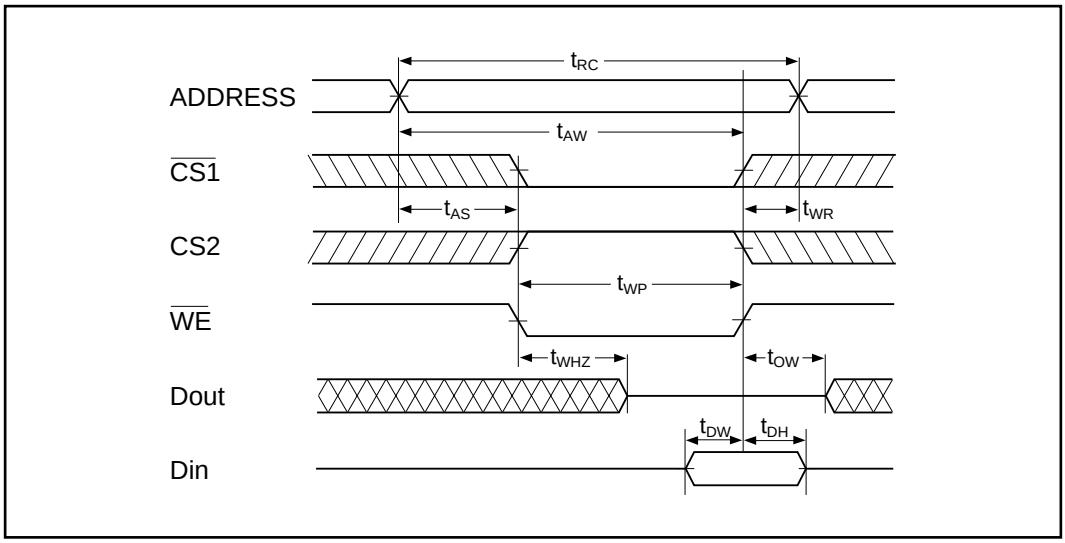
Note: *2. During write cycle that is controlled by $\overline{CS1}$ or CS2, Output Buffer is in high impedance state, whether $\overline{OE}$ level is “H” or “L”.

○ **Write Cycle (2) (CS2 Control)*2**



Note: *2. During write cycle that is controlled by $\overline{CS1}$ or CS2, Output Buffer is in high impedance state, whether $\overline{OE}$ level is "H" or "L".

○ **Write Cycle (3) ($\overline{WE}$ Control)*3, *4**



Note: *3. During write cycle that is controlled by $\overline{WE}$, Output Buffer is in high impedance state if $\overline{OE}$ is "H" level.
*4. When I/O terminals are output mode, be careful not to give the opposite signals to the I/O terminals.

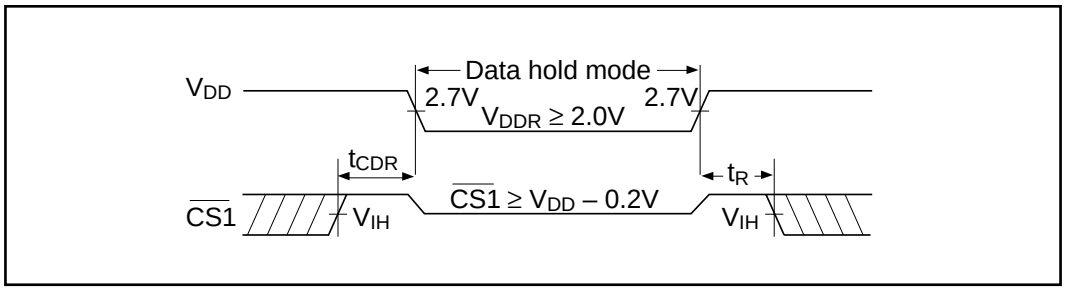
■ DATA RETENTION CHARACTERISTIC WITH LOW VOLTAGE POWER SUPPLY

V_{SS} = 0V, T_a = –25 to 85°C)

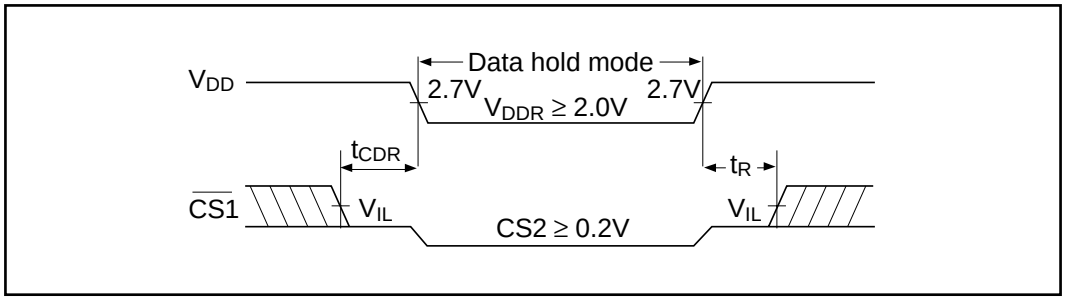
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDR}		2.0	—	3.6	V
Data retention current	I_{DDR}	V_{DD} = 2.7V $\overline{CS1}$ = CS2 ≥ V_{DD} – 0.2V or CS2 ≤ 0.2V	—	0.5*	50	µA
Chip select data hold time	t_{CDR}		0	—	—	ns
Operation recovery time	t_R		5	—	—	ms

* T_a = 25°C

● **Data Retention Timing ($\overline{CS1}$ Control)**



● **Data Retention Timing (CS2 Control)**



* When retaining data in standby mode, supply voltage can be lowered within a certain range. But read or write cycle cannot be performed while the supply voltage is low.

■ FUNCTIONS

● Truth Table

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	Data I/O	Mode	I_{DD}
H	X	X	X	Hi-Z	Unselected	I_{DDS}, I_{DDS1}
X	L	X	X	Hi-Z	Unselected	I_{DDS}, I_{DDS1}
L	H	X	L	Input data	Write	I_{DDO}
L	H	L	H	Output data	Read	I_{DDO}
L	H	H	H	Hi-Z	Output disable	I_{DDO}

X: "H" or "L"

● Reading Data

Data is able to be read when the address is set while holding $\overline{CS1}$ = "L", CS2 = "H", $\overline{OE}$ = "L" and $\overline{WE}$ = "H". Since data I/O terminals are in high impedance state when $\overline{OE}$ = "H", the data bus line can be used for any other objective, then access time apparently is able to be cut down.

● Writing Data

There are the following 4 ways of writing data into memory:

(1) Hold CS2 = "H", $\overline{WE}$ = "L", set addresses and give "L" pulse to $\overline{CS1}$.
(2) Hold $\overline{CS1}$ = "L", $\overline{WE}$ = "L", set addresses and give "H" pulse to CS2.
(3) Hold $\overline{CS1}$ = "L", CS2 = "H", set addresses and give "L" pulse to $\overline{WE}$.
(4) After setting addresses, give "L" pulse to $\overline{CS1}$, $\overline{WE}$ and give "H" pulse to CS2.

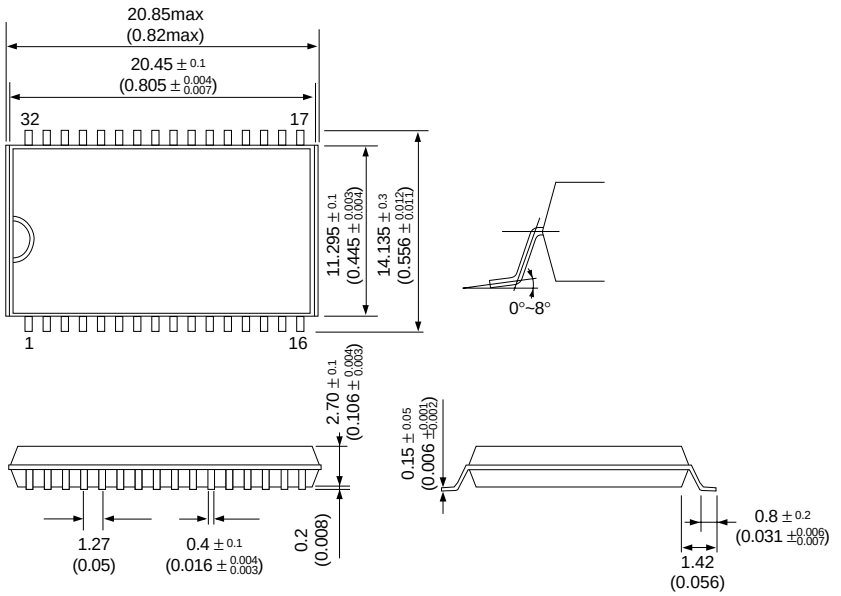
Anyway, data on the data I/O terminals are latched up into the SRM20V100LLMX7 at the end of the period that $\overline{CS1}$, $\overline{WE}$ are "L" level, and CS2 is "H" level. As data I/O terminals are in high impedance state when any of $\overline{CS1}$, $\overline{OE}$ = "H", or CS2 = "L", the contention on the data bus can be avoided.

● Standby Mode

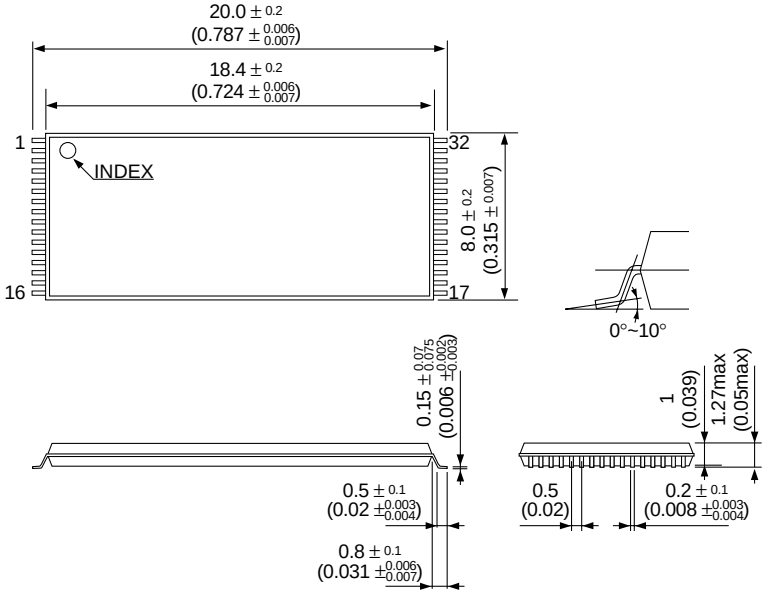
When $\overline{CS1}$ is "H" or CS2 is "L" level, the SRM20V100LLMX7 is in the standby mode which has retaining data operation. In this case, data I/O terminals are Hi-Z, and all inputs of addresses, $\overline{WE}$ and data can be any "H" or "L". When $\overline{CS1}$ and CS2 level are in the range over V_{DD}–0.2V, CS2 level is in the range under 0.2V, in the SRM20V100LLMX7 there is almost no current flow except through the high resistance parts of the memory.

■ PACKAGE DIMENSIONS

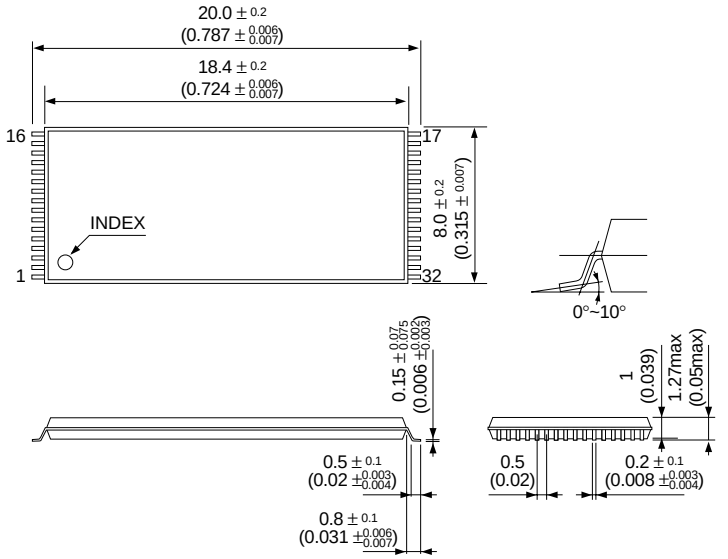
Plastic SOP6-32 pin **Unit: mm (inch)**



Plastic TSOP(I)-32 pin **Unit: mm (inch)**

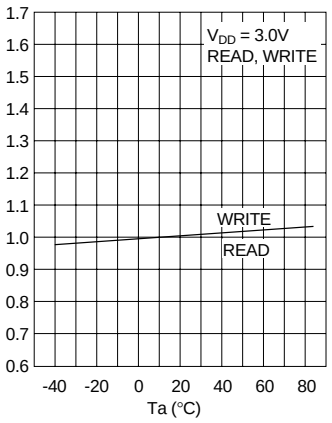


Plastic TSOP (I)-32 pin-R1 **Unit: mm (inch)**

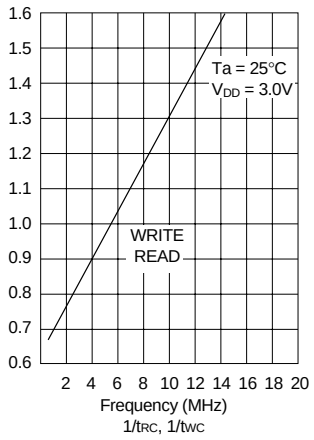


■ CHARACTERISTIC CURVES

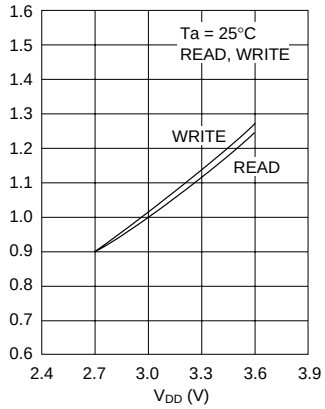
Normalized I_{DDA}–Ta



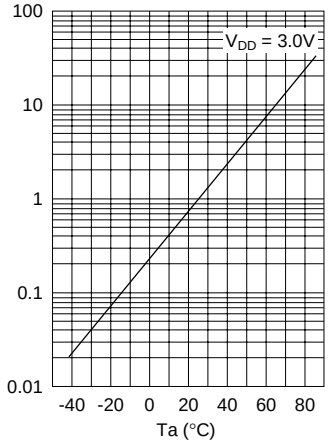
Normalized I_{DDA}–Frequency



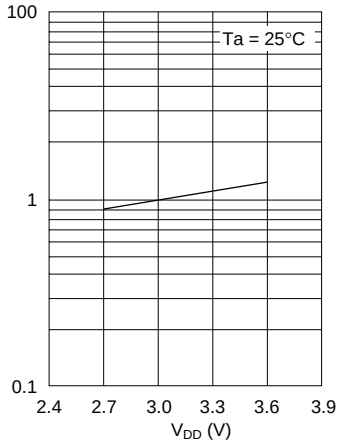
Normalized I_{DDA}–V_{DD}



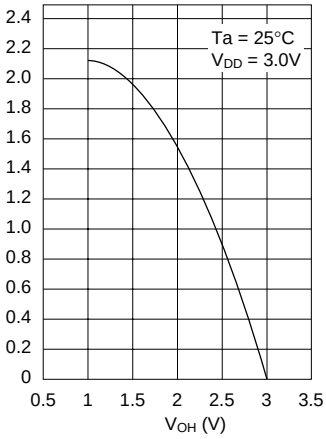
Normalized I_{DDS1}–Ta

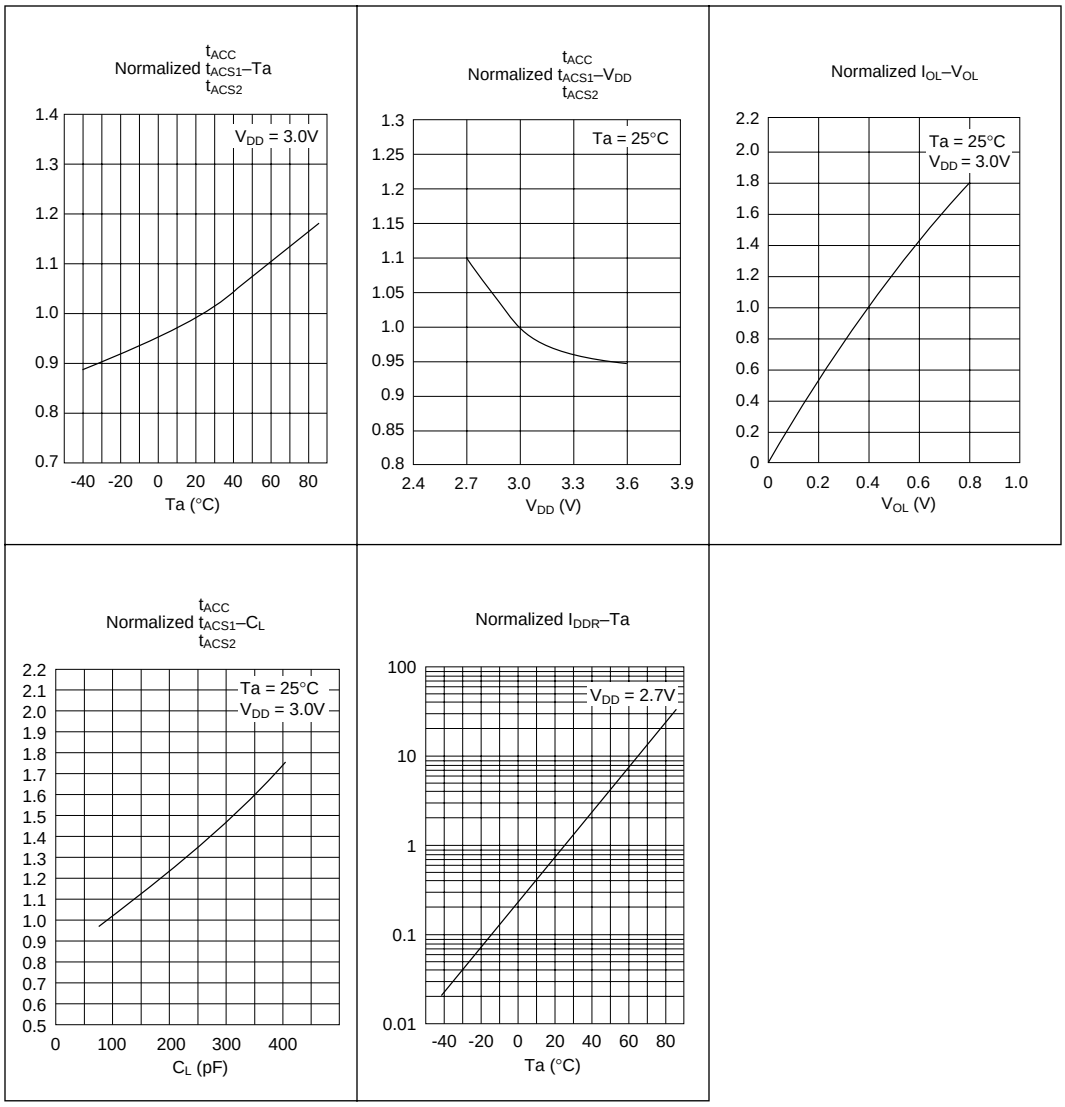


Normalized I_{DDS1}–V_{DD}



Normalized I_{OH}–V_{OH}




tACC
Normalized tACS1–Ta
tACS2
VDD = 3.0V
1.4
1.3
1.2
1.1
1.0
0.9
0.8
0.7
-40 -20 0 20 40 60 80
Ta (°C)
tACC
Normalized tACS1–VDD
tACS2
Ta = 25°C
1.3
1.25
1.2
1.15
1.1
1.05
1.0
0.95
0.9
0.85
0.8
2.4 2.7 3.0 3.3 3.6 3.9
VDD (V)
Normalized IOL–VOL
Ta = 25°C
VDD = 3.0V
2.2
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0
0 0.2 0.4 0.6 0.8 1.0
VOL (V)
tACC
Normalized tACS1–CL
tACS2
Ta = 25°C
VDD = 3.0V
2.2
2.1
2.0
1.9
1.8
1.7
1.6
1.5
1.4
1.3
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
0 100 200 300 400
CL (pF)
Normalized IDDR–Ta
VDD = 2.7V
100
10
1
0.1
0.01
-40 -20 0 20 40 60 80
Ta (°C)

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