

The RF MOSFET Line

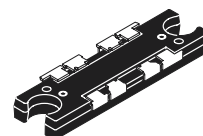
RF Power Field Effect Transistors N-Channel Enhancement-Mode Lateral MOSFETs

Designed for broadband commercial and industrial applications with frequencies up to 470 MHz. The high gain and broadband performance of these devices make them ideal for large-signal, common source amplifier applications in 12.5 volt mobile FM equipment.

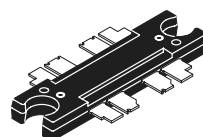
- Specified Performance @ 470 MHz, 12.5 Volts
 - Output Power — 70 Watts
 - Power Gain — 10 dB
 - Efficiency — 50%
- Capable of Handling 20:1 VSWR, @ 15.6 Vdc, 470 MHz, 2 dB Overdrive
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Broadband-Full Power Across the Band: 135–175 MHz
400–470 MHz
- Broadband Demonstration Amplifier Information Available Upon Request
- Available in Tape and Reel. T1 Suffix = 500 Units per 44 mm, 13 inch Reel.

MRF1570T1
MRF1570FT1

470 MHz, 70 W, 12.5 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFETs



CASE 1366-03, STYLE 1
TO-272 SPLIT LEAD
PLASTIC
MRF1570T1



CASE 1366A-02, STYLE 1
TO-272 STRAIGHT LEAD
PLASTIC
MRF1570FT1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	40	Vdc
Gate-Source Voltage	V_{GS}	± 20	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	165 0.5	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	- 65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	175	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M2 (Minimum)
Charge Device Model	C2 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.75	$^\circ\text{C}/\text{W}$

NOTE – CAUTION – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Zero Gate Voltage Drain Current ($V_{DS} = 60\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μA
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ON CHARACTERISTICS

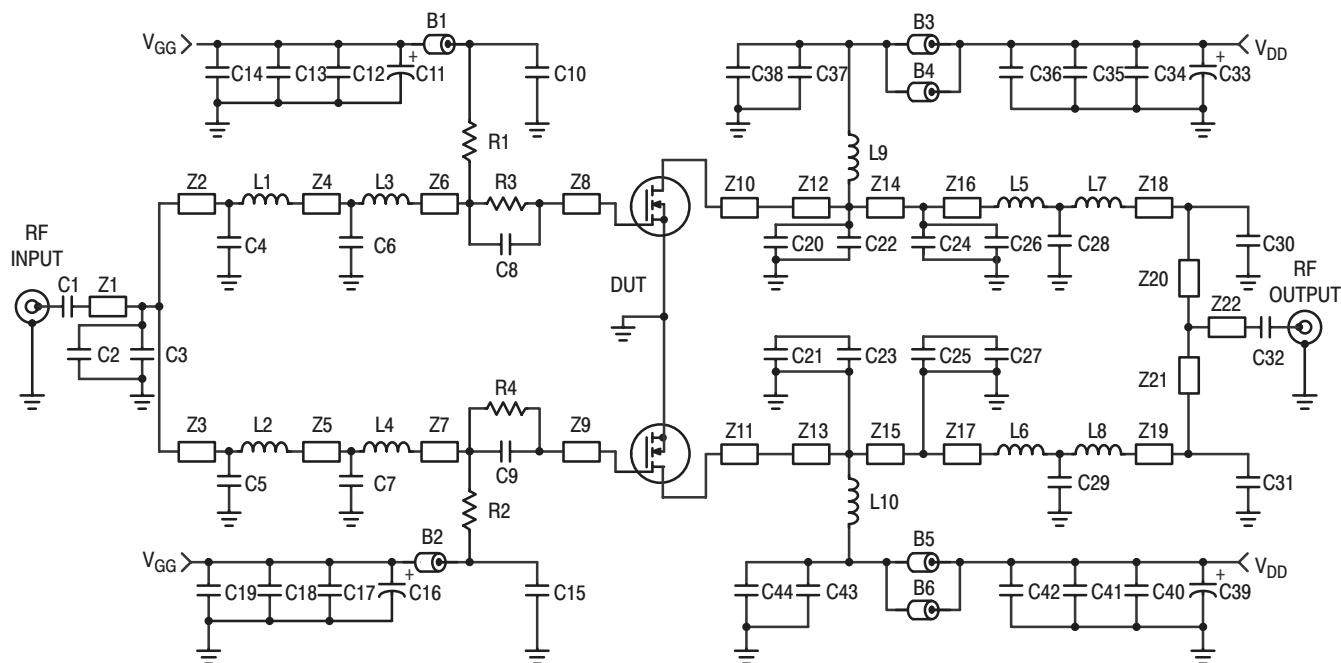
Gate Threshold Voltage ($V_{DS} = 12.5\text{ Vdc}$, $I_D = 0.8\text{ mAdc}$)	$V_{GS(th)}$	1.0	—	3	Vdc
Drain–Source On–Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 2.0\text{ Adc}$)	$V_{DS(on)}$	—	—	1	Vdc

DYNAMIC CHARACTERISTICS

Input Capacitance (Includes Input Matching Capacitance) ($V_{DS} = 12.5\text{ Vdc}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$)	C_{iss}	—	—	500	pF
Output Capacitance ($V_{DS} = 12.5\text{ Vdc}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$)	C_{oss}	—	—	250	pF
Reverse Transfer Capacitance ($V_{DS} = 12.5\text{ Vdc}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$)	C_{rss}	—	—	35	pF

RF CHARACTERISTICS (In Motorola Test Fixture)

Common–Source Amplifier Power Gain ($V_{DD} = 12.5\text{ Vdc}$, $P_{out} = 70\text{ W}$, $I_{DQ} = 800\text{ mA}$) $f = 470\text{ MHz}$	G_{ps}	10	—	—	dB
Drain Efficiency ($V_{DD} = 12.5\text{ Vdc}$, $P_{out} = 70\text{ W}$, $I_{DQ} = 800\text{ mA}$) $f = 470\text{ MHz}$	η	50	—	—	%
Load Mismatch ($V_{DD} = 15.6\text{ Vdc}$, $f = 470\text{ MHz}$, 2 dB Input Overdrive, VSWR 20:1 at All Phase Angles)	Ψ	No Degradation in Output Power Before and After Test			



B1, B2, B3, B4, B5, B6 Long Ferrite Beads, Fair Rite Products
 C1, C32, C37, C43 270 pF, 100 mil Chip Capacitors
 C2, C20, C21 33 pF, 100 mil Chip Capacitors
 C3 18 pF, 100 mil Chip Capacitor
 C4, C5 30 pF, 100 mil Chip Capacitors
 C6, C7 180 pF, 100 mil Chip Capacitors
 C8, C9 150 pF, 100 mil Chip Capacitors
 C10, C15 300 pF, 100 mil Chip Capacitors
 C11, C16, C33, C39 10 μ F, 50 V Electrolytic Capacitors
 C12, C17, C34, C40 0.1 μ F, 100 mil Chip Capacitors
 C13, C18, C35, C41 1000 pF, 100 mil Chip Capacitors
 C14, C19, C36, C42 470 pF, 100 mil Chip Capacitors
 C22, C23 110 pF, 100 mil Chip Capacitors
 C24, C25 68 pF, 100 mil Chip Capacitors
 C26, C27 120 pF, 100 mil Chip Capacitors
 C28, C29 24 pF, 100 mil Chip Capacitors
 C30, C31 27 pF, 100 mil Chip Capacitors
 C38, C44 240 pF, 100 mil Chip Capacitors
 L1, L2 17.5 nH, 6 Turn Inductors, Coilcraft

L3, L4 5 nH, 2 Turn Inductors, Coilcraft
 L5, L6, L7, L8 1 Turn, #18 AWG, 0.33" ID Inductors
 L9, L10 3 Turn, #16 AWG, 0.165" ID Inductors
 N1, N2 Type N Flange Mounts
 R1, R2 25.5 Ω Chip Resistors (1206)
 R3, R4 9.3 Ω Chip Resistors (1206)
 Z1 0.32" x 0.080" Microstrip
 Z2, Z3 0.46" x 0.080" Microstrip
 Z4, Z5 0.34" x 0.080" Microstrip
 Z6, Z7 0.45" x 0.080" Microstrip
 Z8, Z9, Z10, Z11 0.28" x 0.240" Microstrip
 Z12, Z13 0.39" x 0.080" Microstrip
 Z14, Z15 0.27" x 0.080" Microstrip
 Z16, Z17 0.25" x 0.080" Microstrip
 Z18, Z19 0.29" x 0.080" Microstrip
 Z20, Z21 0.14" x 0.080" Microstrip
 Z22 0.32" x 0.080" Microstrip
 Board 31 mil Glass Teflon®

Figure 1.135 – 175 MHz Broadband Test Circuit Schematic

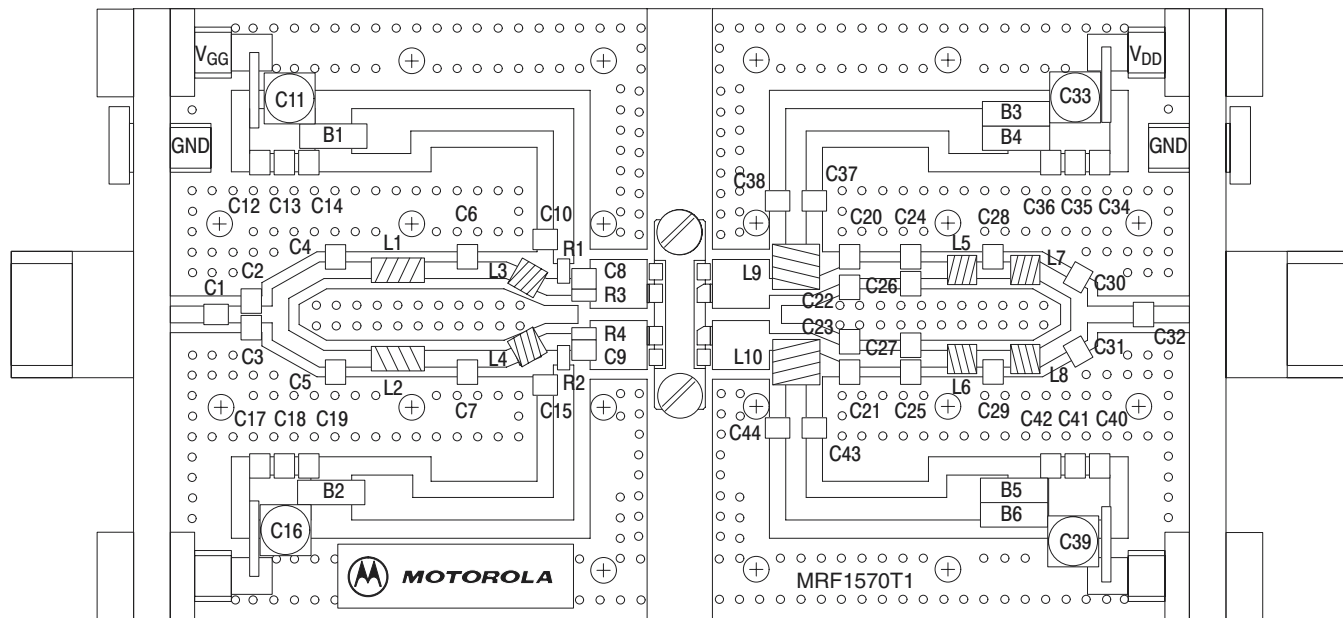


Figure 2. 135 – 175 MHz Broadband Test Circuit Component Layout

TYPICAL CHARACTERISTICS, 135 – 175 MHz

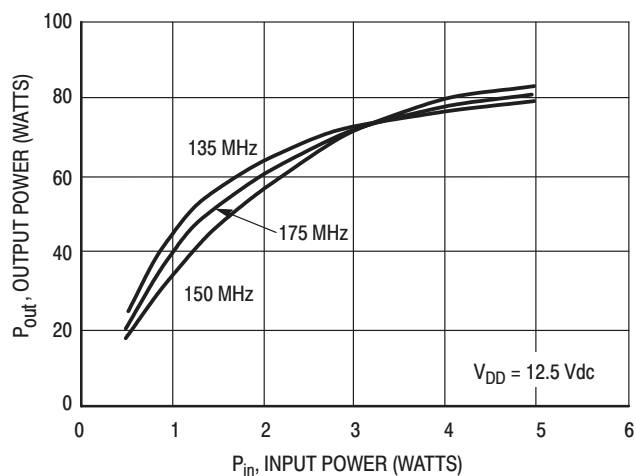


Figure 3. Output Power versus Input Power

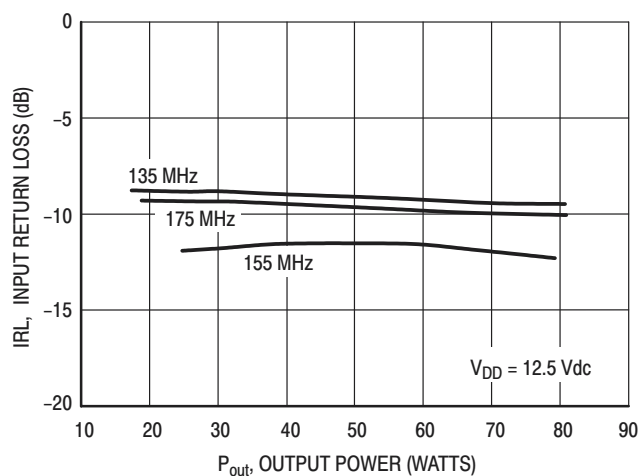


Figure 4. Input Return Loss versus Output Power

TYPICAL CHARACTERISTICS, 135 – 175 MHz

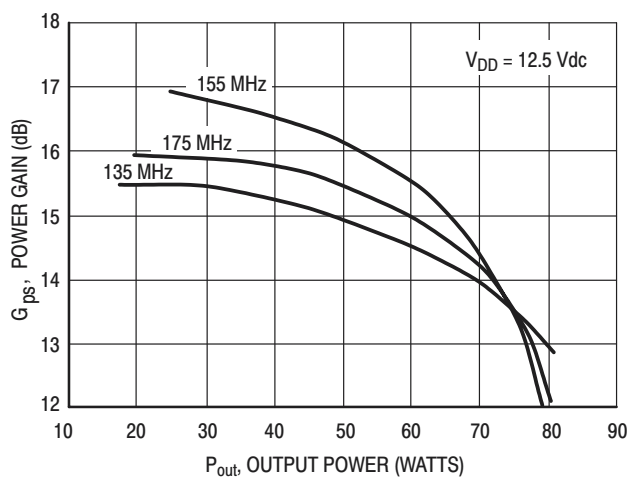


Figure 5. Gain versus Output Power

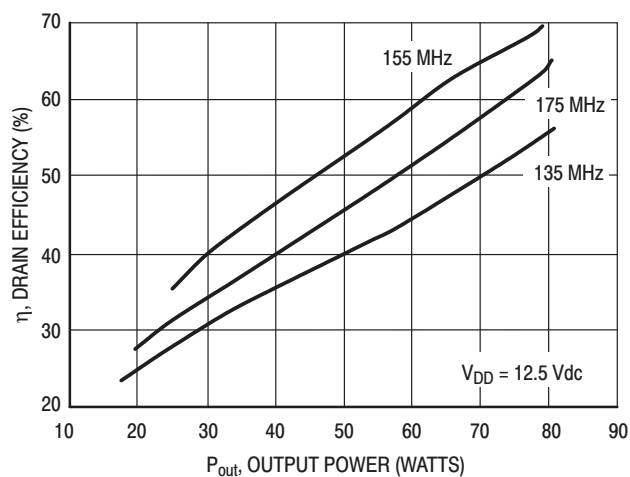


Figure 6. Drain Efficiency versus Output Power

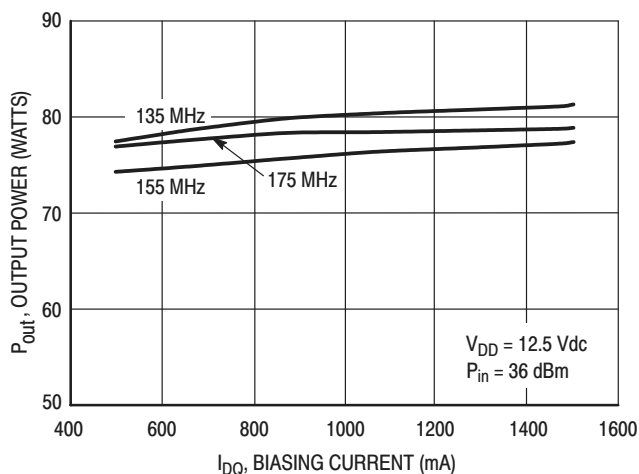


Figure 7. Output Power versus Biasing Current

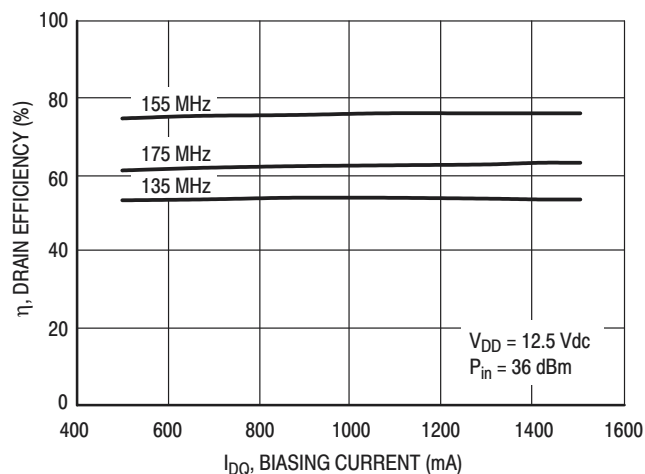


Figure 8. Drain Efficiency versus Biasing Current

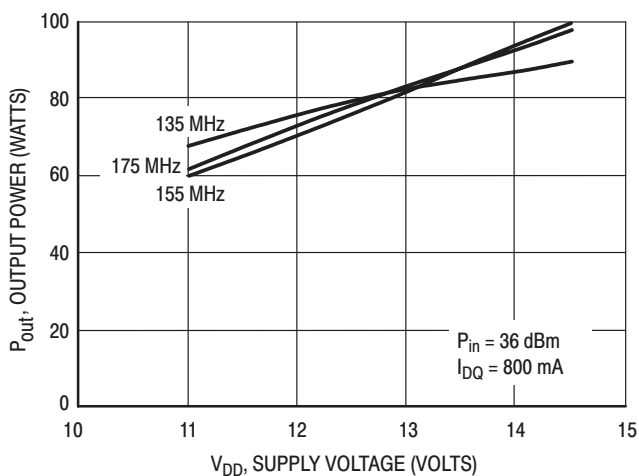


Figure 9. Output Power versus Supply Voltage

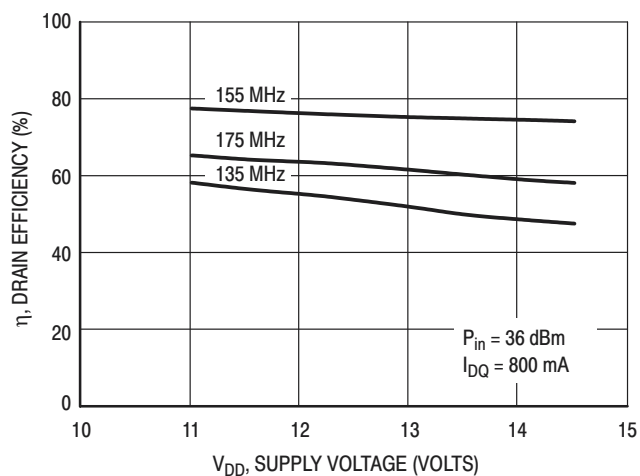
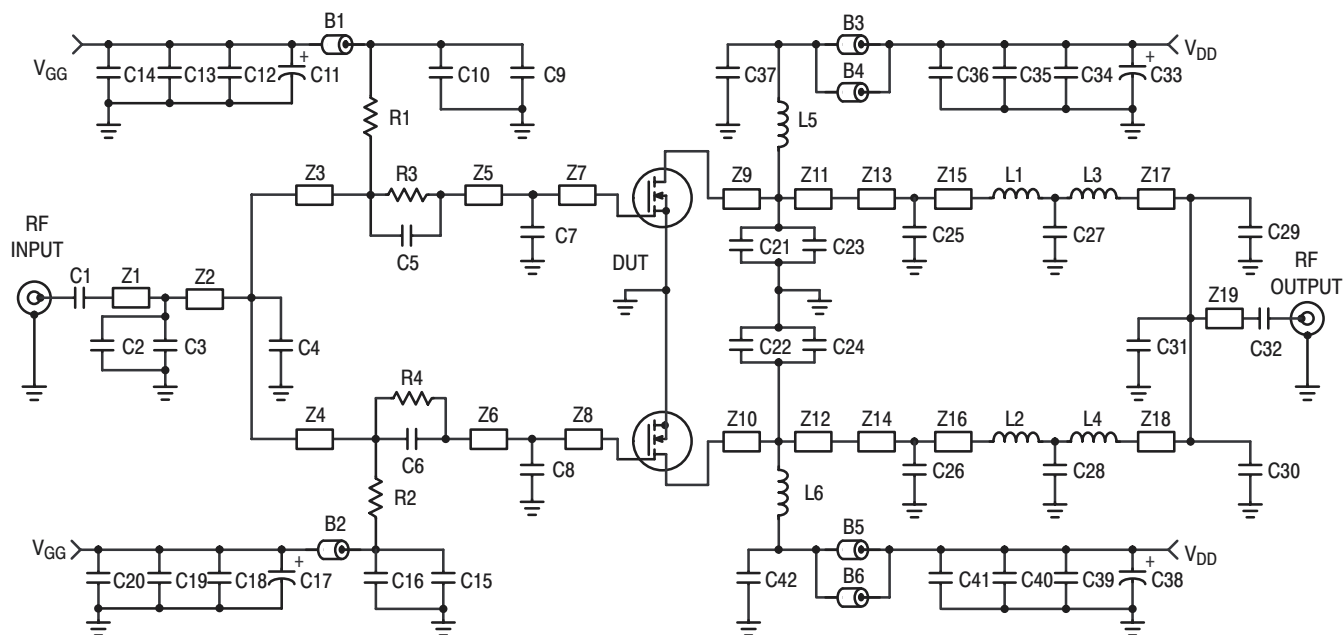


Figure 10. Drain Efficiency versus Supply Voltage



B1, B2, B3, B4, B5, B6 Long Ferrite Beads, Fair Rite Products
 C1, C9, C15, C32 270 pF, 100 mil Chip Capacitors
 C2, C3 7.5 pF, 100 mil Chip Capacitors
 C4 5.1 pF, 100 mil Chip Capacitor
 C5, C6 180 pF, 100 mil Chip Capacitors
 C7, C8 47 pF, 100 mil Chip Capacitors
 C10, C16, C37, C42 120 pF, 100 mil Chip Capacitors
 C11, C17, C33, C38 10 μ F, 50 V Electrolytic Capacitors
 C12, C18, C34, C39 470 pF, 100 mil Chip Capacitors
 C13, C19, C35, C40 1200 pF, 100 mil Chip Capacitors
 C14, C20, C36, C41 0.1 μ F, 100 mil Chip Capacitors
 C21, C22 33 pF, 100 mil Chip Capacitors
 C23, C24 27 pF, 100 mil Chip Capacitors
 C25, C26 15 pF, 100 mil Chip Capacitors
 C27, C28 2.2 pF, 100 mil Chip Capacitors
 C29, C30 6.2 pF, 100 mil Chip Capacitors
 C31 1.0 pF, 100 mil Chip Capacitor

L1, L2, L3, L4 1 Turn, #18 AWG, 0.085" ID Inductors
 L5, L6 2 Turn, #16 AWG, 0.165" ID Inductors
 N1, N2 Type N Flange Mounts
 R1, R2 25.5 Ω Chip Resistors (1206)
 R3, R4 10 Ω Chip Resistors (1206)
 Z1 0.240" x 0.080" Microstrip
 Z2 0.185" x 0.080" Microstrip
 Z3, Z4 1.500" x 0.080" Microstrip
 Z5, Z6 0.150" x 0.240" Microstrip
 Z7, Z8 0.140" x 0.240" Microstrip
 Z9, Z10 0.140" x 0.240" Microstrip
 Z11, Z12 0.150" x 0.240" Microstrip
 Z13, Z14 0.270" x 0.080" Microstrip
 Z15, Z16 0.680" x 0.080" Microstrip
 Z17, Z18 0.320" x 0.080" Microstrip
 Z19 0.380" x 0.080" Microstrip
 Board 31 mil Glass Teflon®

Figure 11. 400 – 470 MHz Broadband Test Circuit Schematic

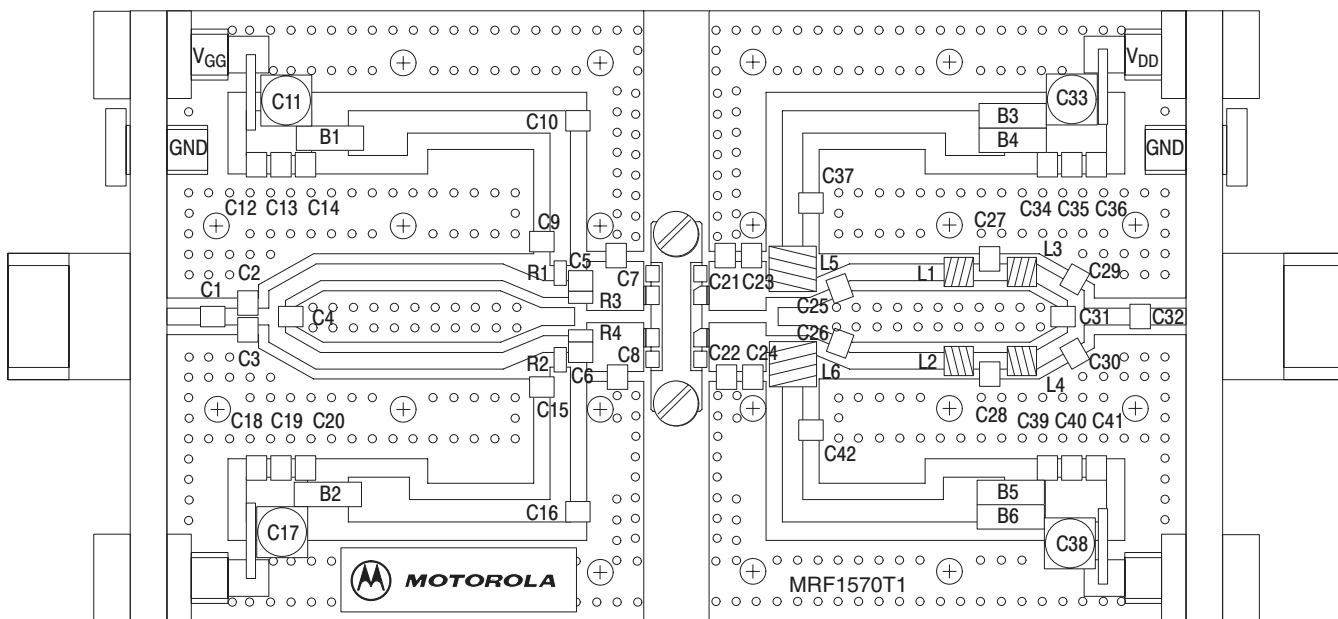


Figure 12. 400 – 470 MHz Broadband Test Circuit Component Layout

TYPICAL CHARACTERISTICS, 400 – 470 MHz

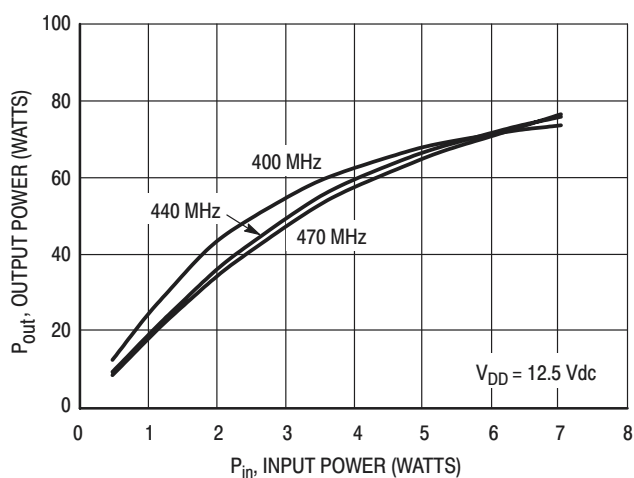


Figure 13. Output Power versus Input Power

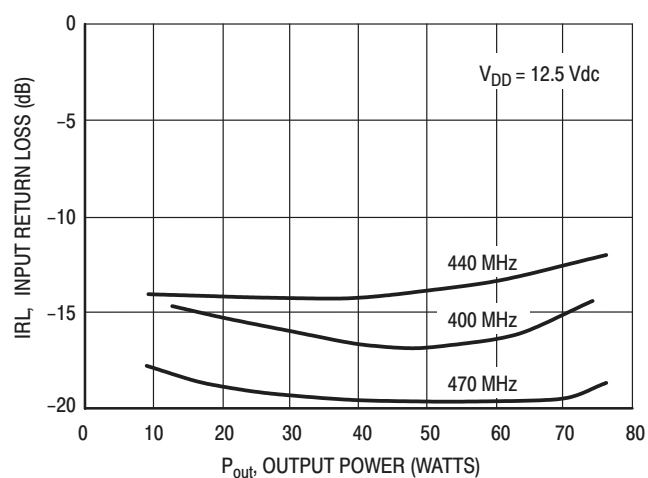


Figure 14. Input Return Loss versus Output Power

TYPICAL CHARACTERISTICS, 400 – 470 MHz

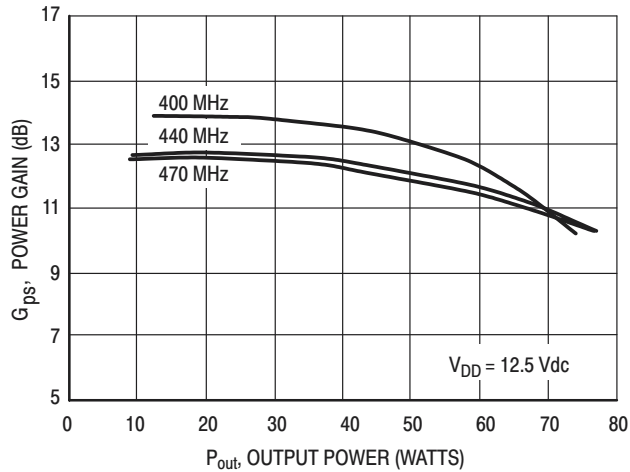


Figure 15. Gain versus Output Power

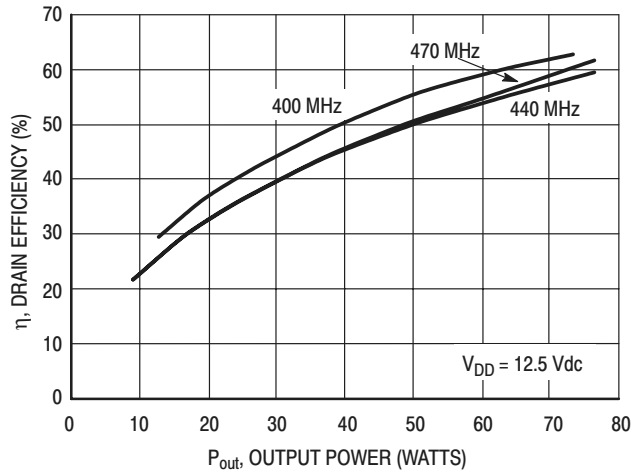


Figure 16. Drain Efficiency versus Output Power

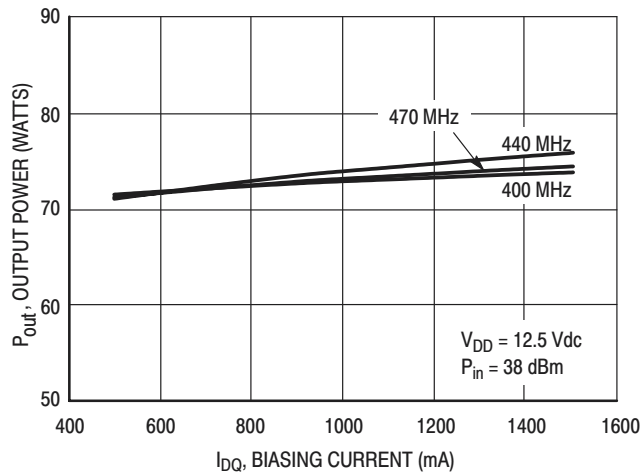


Figure 17. Output Power versus Biasing Current

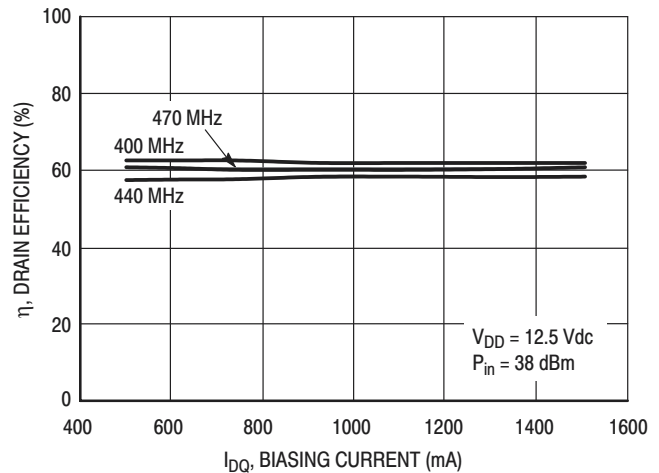


Figure 18. Drain Efficiency versus Biasing Current

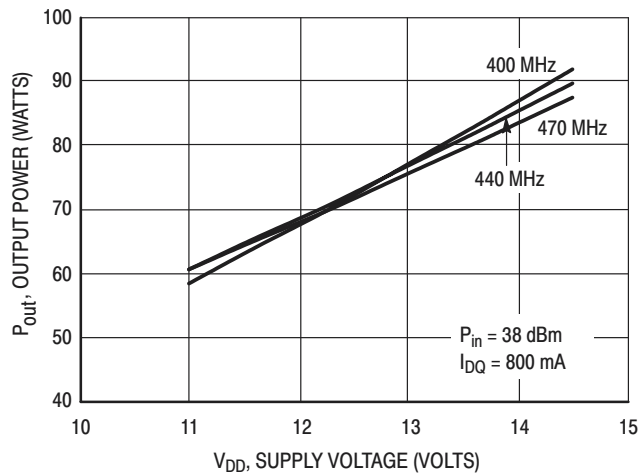


Figure 19. Output Power versus Supply Voltage

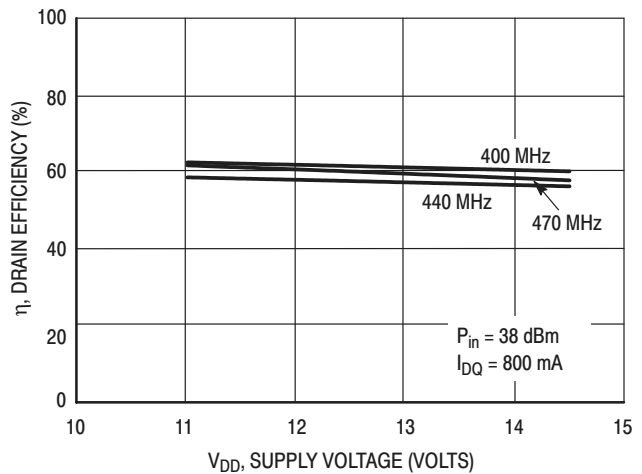
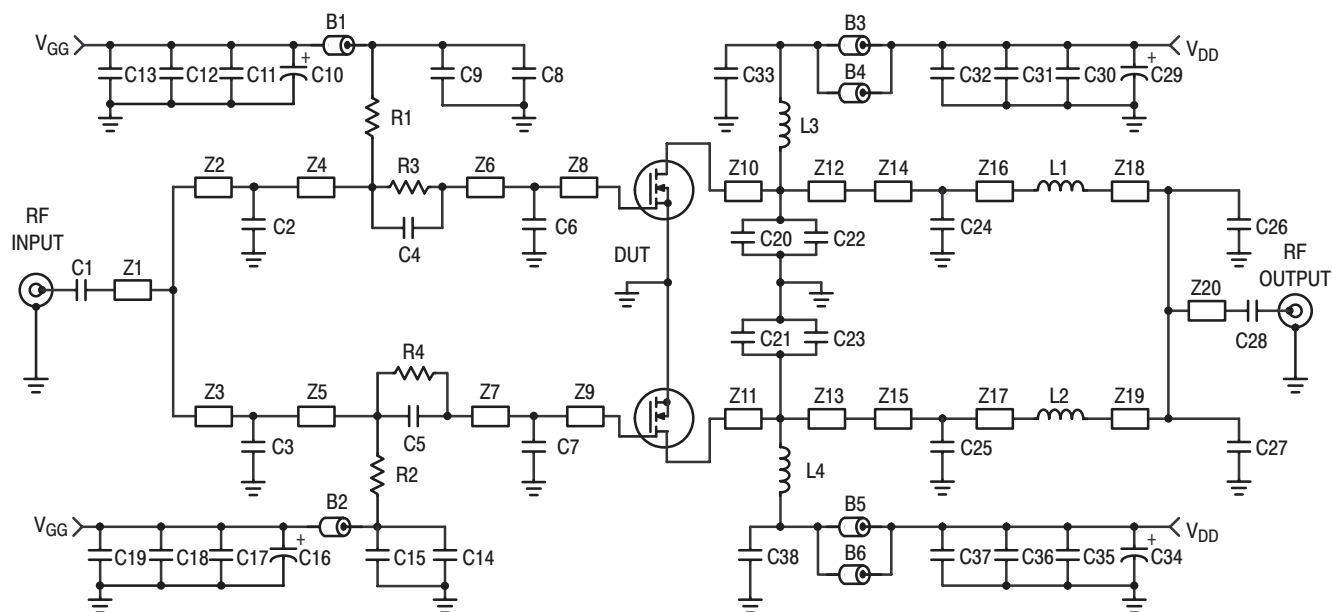


Figure 20. Drain Efficiency versus Supply Voltage



B1, B2, B3, B4, B5, B6	Long Ferrite Beads, Fair Rite Products	N1, N2	Type N Flange Mounts
C1, C8, C14, C28	270 pF, 100 mil Chip Capacitors	R1, R2	1.0 k Ω Chip Resistors (1206)
C2, C3	10 pF, 100 mil Chip Capacitors	R3, R4	10 Ω Chip Resistors (1206)
C4, C5	180 pF, 100 mil Chip Capacitors	Z1	0.40" x 0.080" Microstrip
C6, C7	47 pF, 100 mil Chip Capacitors	Z2, Z3	0.26" x 0.080" Microstrip
C9, C15, C33, C38	120 pF, 100 mil Chip Capacitors	Z4, Z5	1.35" x 0.080" Microstrip
C10, C16, C29, C34	10 μ F, 50 V Electrolytic Capacitors	Z6, Z7	0.17" x 0.240" Microstrip
C11, C17, C30, C35	470 pF, 100 mil Chip Capacitors	Z8, Z9	0.12" x 0.240" Microstrip
C12, C18, C31, C36	1200 pF, 100 mil Chip Capacitors	Z10, Z11	0.14" x 0.240" Microstrip
C13, C19, C32, C37	0.1 μ F, 100 mil Chip Capacitors	Z12, Z13	0.15" x 0.240" Microstrip
C20, C21	22 pF, 100 mil Chip Capacitors	Z14, Z15	0.18" x 0.172" Microstrip
C22, C23	20 pF, 100 mil Chip Capacitors	Z16, Z17	1.23" x 0.080" Microstrip
C24, C25, C26, C27	5.1 pF, 100 mil Chip Capacitors	Z18, Z19	0.12" x 0.080" Microstrip
L1, L2	1 Turn, #18 AWG, 0.115" ID Inductors	Z20	0.40" x 0.080" Microstrip
L3, L4	2 Turn, #16 AWG, 0.165" ID Inductors	Board	31 mil Glass Teflon [®]

Figure 21. 450 – 520 MHz Broadband Test Circuit Schematic

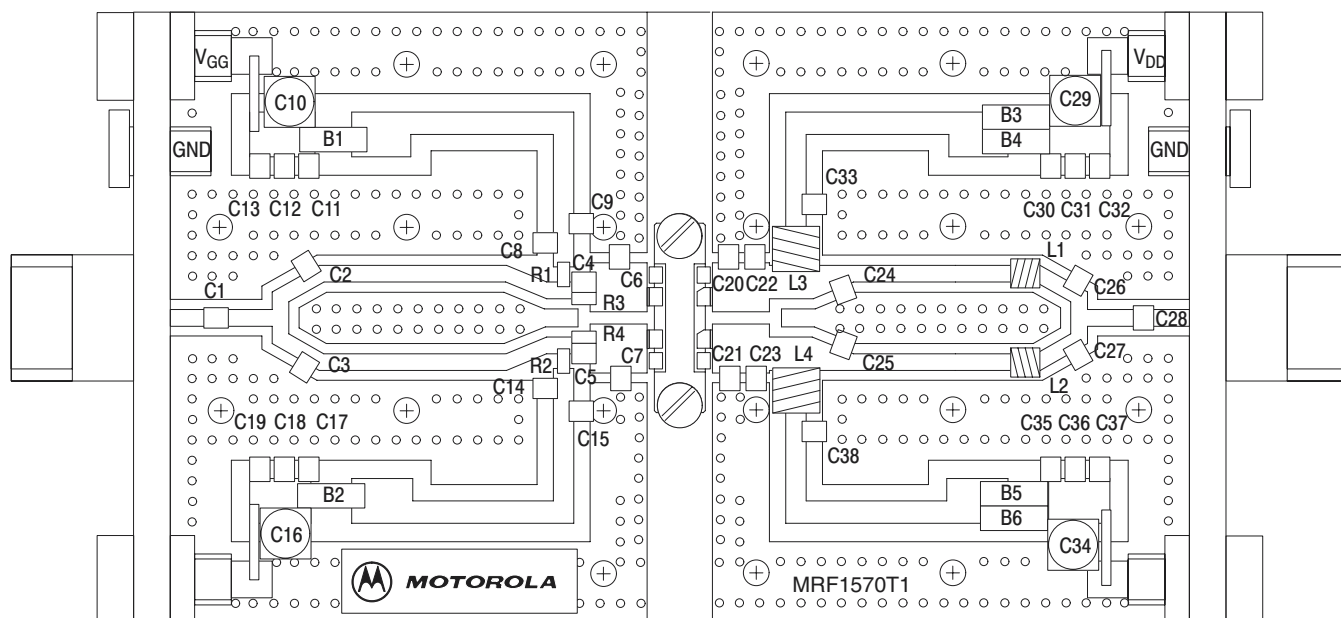


Figure 22. 450 – 520 MHz Broadband Test Circuit Component Layout

TYPICAL CHARACTERISTICS, 450 – 520 MHz

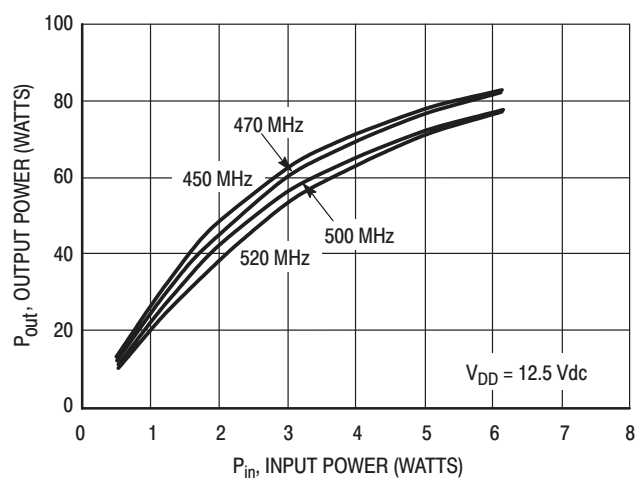


Figure 23. Output Power versus Input Power

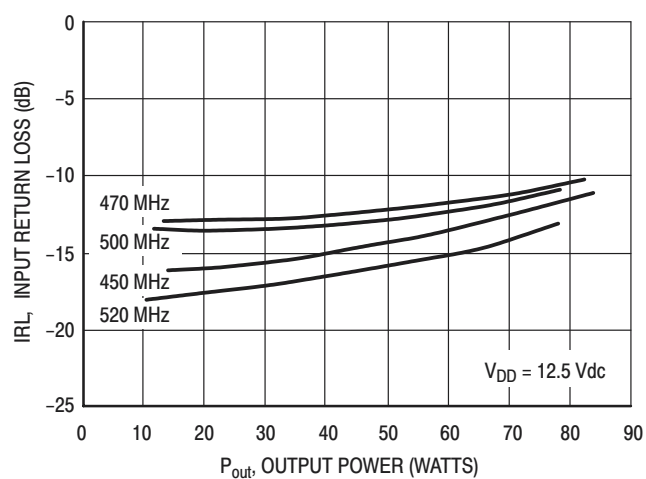


Figure 24. Input Return Loss versus Output Power

TYPICAL CHARACTERISTICS, 450 – 520 MHz

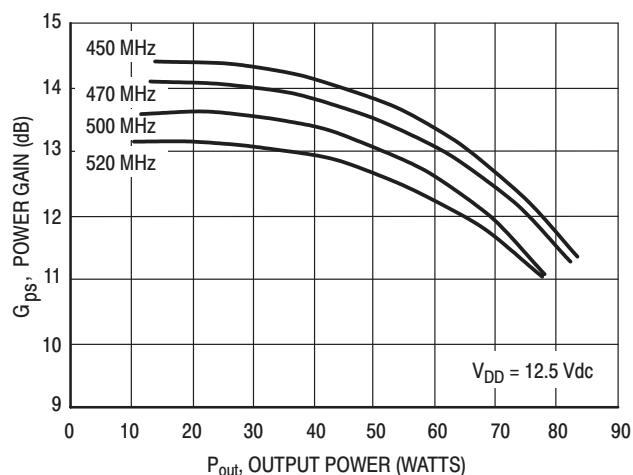


Figure 25. Gain versus Output Power

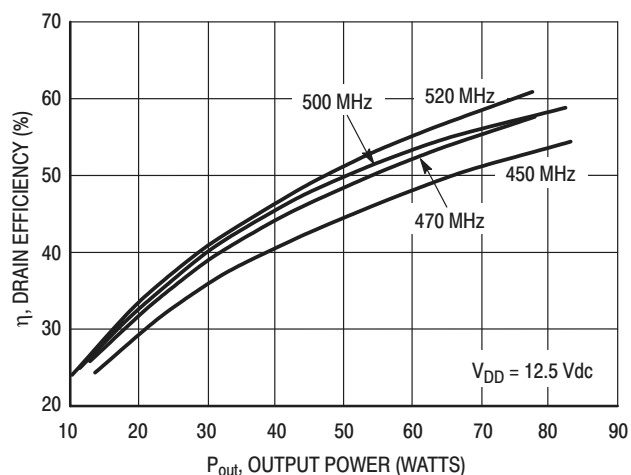


Figure 26. Drain Efficiency versus Output Power

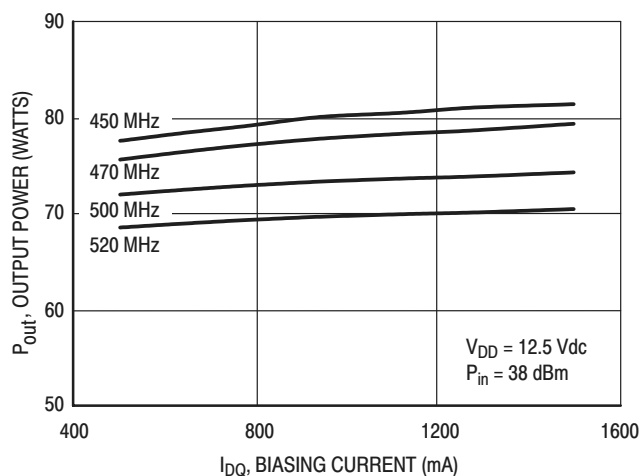


Figure 27. Output Power versus Biasing Current

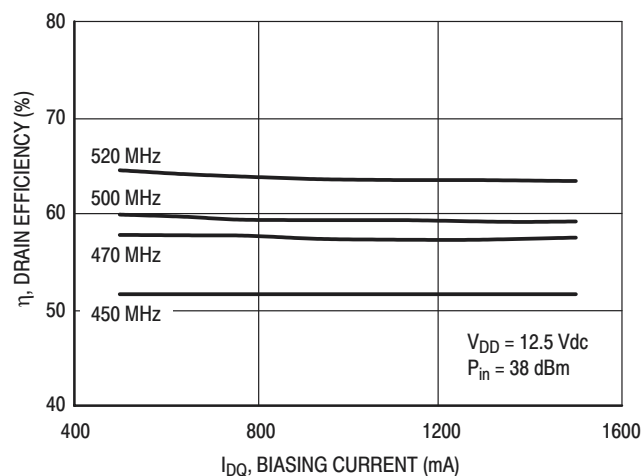


Figure 28. Drain Efficiency versus Biasing Current

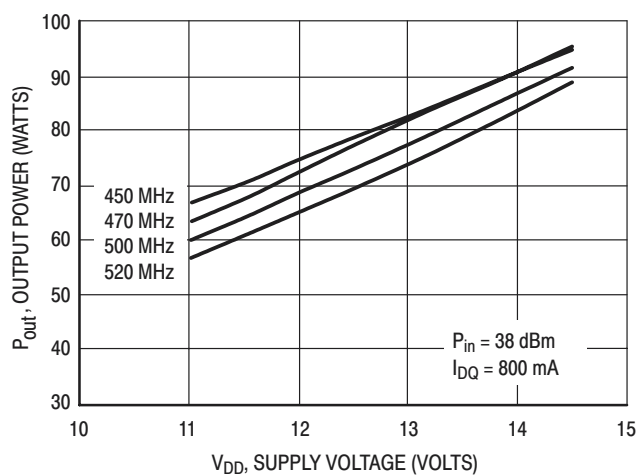


Figure 29. Output Power versus Supply Voltage

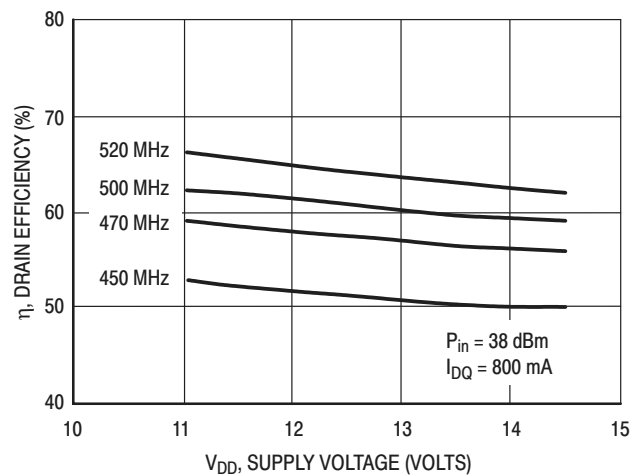
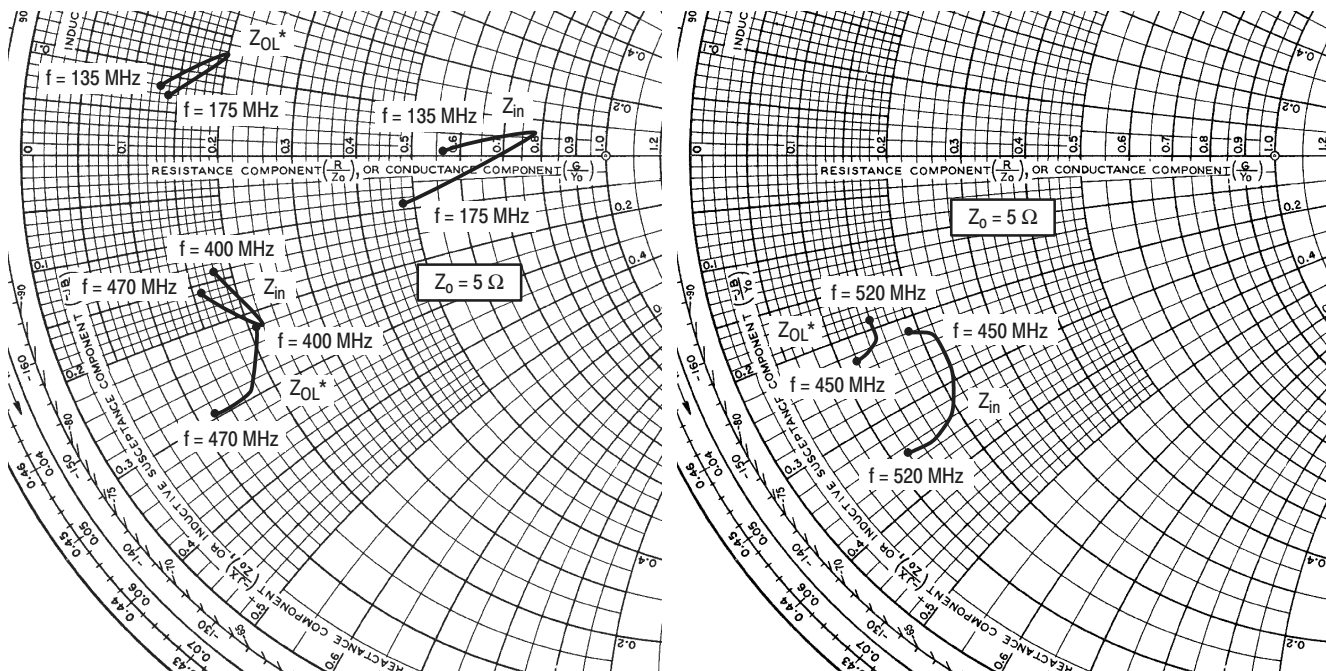


Figure 30. Drain Efficiency versus Supply Voltage



$V_{DD} = 12.5 \text{ V}$, $I_{DQ} = 0.8 \text{ A}$, $P_{out} = 70 \text{ W}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
135	$2.8 + j0.05$	$0.65 + j0.42$
155	$3.9 + j0.34$	$1.01 + j0.63$
175	$2.4 - j0.47$	$0.71 + j0.37$

$V_{DD} = 12.5 \text{ V}$, $I_{DQ} = 0.8 \text{ A}$, $P_{out} = 70 \text{ W}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
400	$0.92 - j0.71$	$1.05 - j1.10$
440	$1.12 - j1.11$	$0.83 - j1.45$
470	$0.82 - j0.79$	$0.59 - j1.43$

$V_{DD} = 12.5 \text{ V}$, $I_{DQ} = 0.8 \text{ A}$, $P_{out} = 70 \text{ W}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
450	$0.94 - j1.12$	$0.61 - j1.14$
470	$1.03 - j1.17$	$0.62 - j1.12$
500	$0.95 - j1.71$	$0.75 - j1.03$
520	$0.62 - j1.74$	$0.77 - j0.97$

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the load impedance at given output power, voltage, frequency, and $\eta_D > 50 \%$.

Notes: Impedance Z_{in} was measured with input terminated at 50Ω .
Impedance Z_{OL} was measured with output terminated at 50Ω .

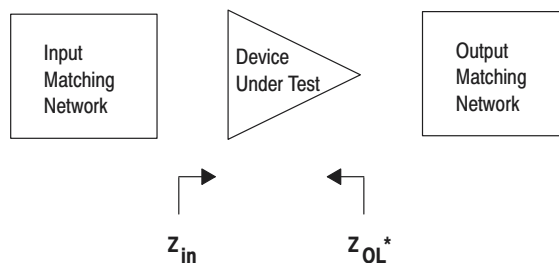


Figure 31. Series Equivalent Input and Output Impedance

DESIGN CONSIDERATIONS

This device is a common-source, RF power, N-Channel enhancement mode, Lateral Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET). Motorola Application Note AN211A, "FETs in Theory and Practice", is suggested reading for those not familiar with the construction and characteristics of FETs.

This surface mount packaged device was designed primarily for VHF and UHF mobile power amplifier applications. Manufacturability is improved by utilizing the tape and reel capability for fully automated pick and placement of parts. However, care should be taken in the design process to insure proper heat sinking of the device.

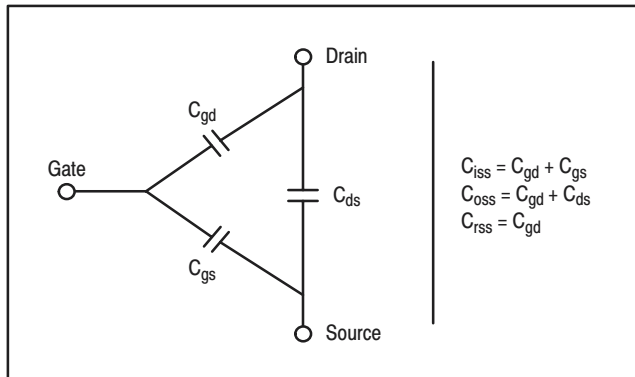
The major advantages of Lateral RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate-to-drain (C_{gd}), and gate-to-source (C_{gs}). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain-to-source (C_{ds}). These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, $R_{DS(on)}$, occurs in the linear region of the output characteristic and is specified at a specific gate-source voltage and drain current. The

drain-source voltage under these conditions is termed $V_{DS(on)}$. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

BV_{DSS} values for this device are higher than normally required for typical applications. Measurement of BV_{DSS} is not recommended and may result in possible damage to the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The DC input resistance is very high — on the order of $10^9 \Omega$ — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate-to-source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended. Using a resistor to keep the gate-to-source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device on.

DC BIAS

Since this device is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. RF power FETs operate optimally with a quiescent drain current (I_{DQ}), whose value is application dependent. This device was characterized at $I_{DQ} = 800 \text{ mA}$, which is the suggested value of bias current for typical applications. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of this device may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. This characteristic is very dependent on frequency and load line.

MOUNTING

The specified maximum thermal resistance of $0.75^{\circ}\text{C}/\text{W}$ assumes a majority of the $0.170'' \times 0.608''$ source contact on the back side of the package is in good contact with an appropriate heat sink. As with all RF power devices, the goal of the thermal design should be to minimize the temperature at the back side of the package. Refer to Motorola Application Note AN4005/D, "Thermal Management and Mounting Method for the PLD-1.5 RF Power Surface Mount Package," and Engineering Bulletin EB209/D, "Mounting Method for RF Power Leadless Surface Mount Transistor" for additional information.

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for this device. For examples

see Motorola Application Note AN721, "Impedance Matching Networks Applied to RF Power Transistors." Large-signal impedances are provided, and will yield a good first pass approximation.

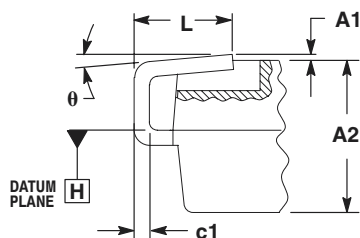
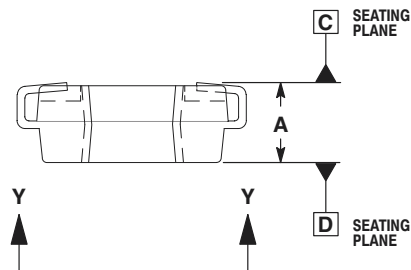
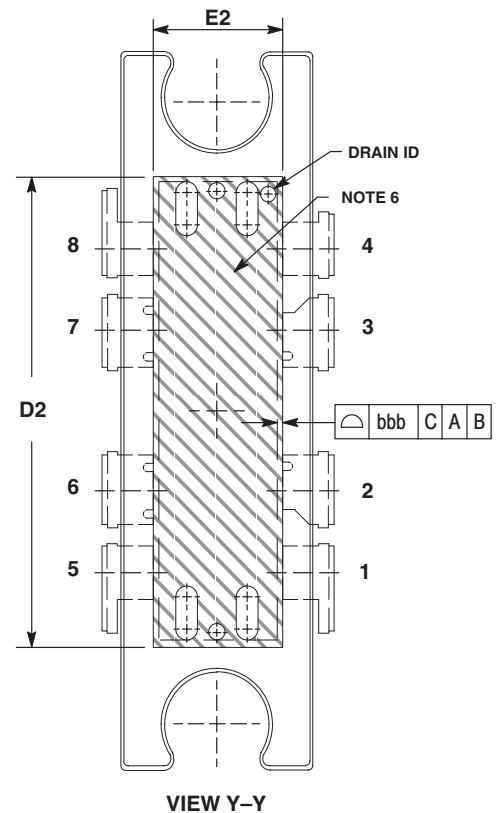
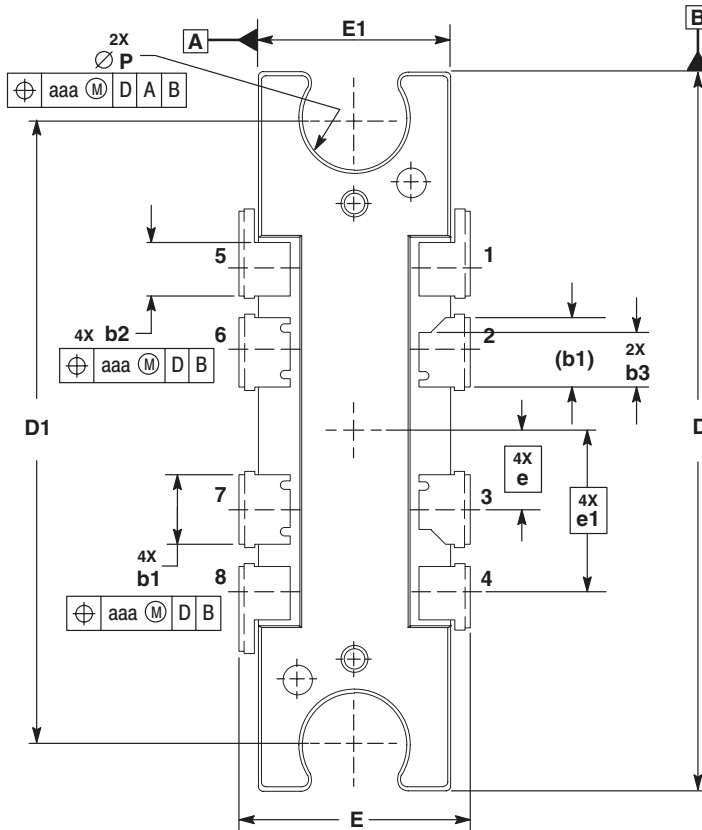
Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of this device yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. The RF test fixture implements a parallel resistor and capacitor in series with the gate, and has a load line selected for a higher efficiency, lower gain, and more stable operating region. See Motorola Application Note AN215A, "RF Small-Signal Design Using Two-Port Parameters" for a discussion of two port network theory and stability.

NOTES

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PACKAGE DIMENSIONS



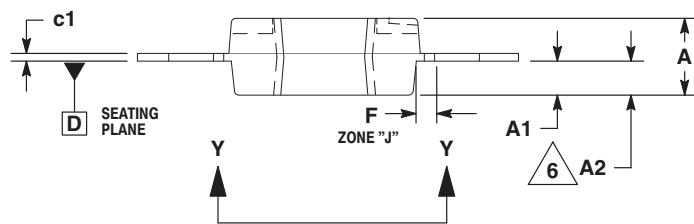
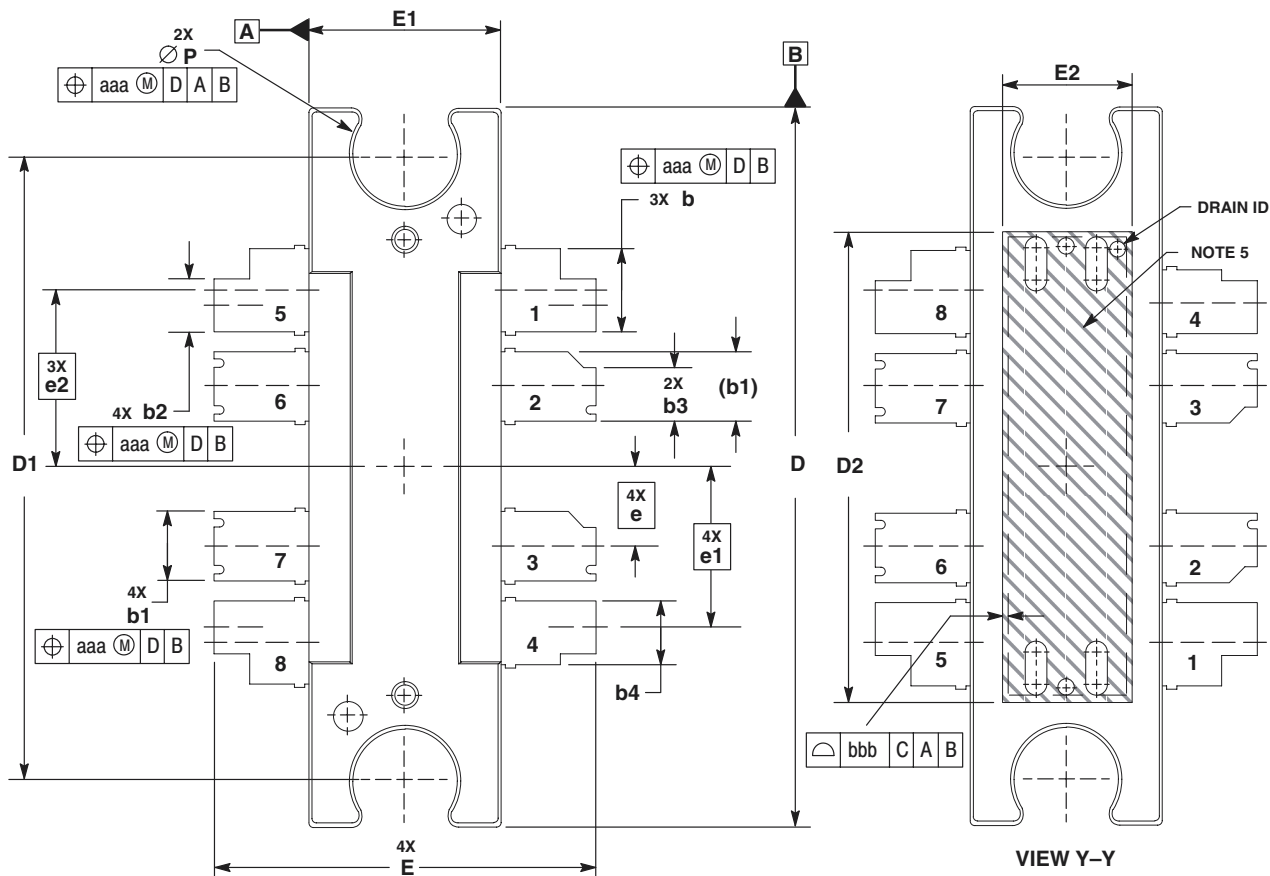
STYLE 1:
 PIN 1. SOURCE (COMMON)
 2. DRAIN
 3. DRAIN
 4. SOURCE (COMMON)
 5. SOURCE (COMMON)
 6. GATE
 7. GATE
 8. SOURCE (COMMON)

**CASE 1366-03
 ISSUE B
 TO-272 SPLIT LEAD
 PLASTIC
 MRF1570T1**

NOTES:

1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE -H- IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.006 PER SIDE. DIMENSION D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS b1 AND b2 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.005 TOTAL IN EXCESS OF THE b1 AND b2 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. CROSSHATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.098	0.110	2.49	2.79
A1	0.000	0.004	0.00	0.10
A2	0.098	0.106	2.49	2.69
D	0.926	0.934	23.52	23.72
D1	0.810 BSC		20.57 BSC	
D2	0.608 BSC		15.44 BSC	
E	0.296	0.304	7.52	7.72
E1	0.246	0.254	6.25	6.45
E2	0.170 BSC		4.32 BSC	
L	0.060	0.070	1.52	1.78
P	0.126	0.134	3.20	3.40
b1	0.088	0.094	2.24	2.39
b2	0.066	0.072	1.68	1.83
b3	0.067	0.073	1.70	1.85
c1	0.007	0.011	0.178	0.279
e	0.104 BSC		2.64 BSC	
e1	0.210 BSC		5.33 BSC	
θ	0°	6°	0°	6°
aaa	0.004		0.10	
bbb	0.008		0.20	



- NOTES:
1. CONTROLLING DIMENSION: INCH.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
 4. DIMENSIONS "b" AND "b1" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.005 TOTAL IN EXCESS OF THE "b1" AND "b2" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
 5. CROSSHATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.
 6. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.

- STYLE 1:
- PIN 1. SOURCE (COMMON)
 - DRAIN
 - DRAIN
 - SOURCE (COMMON)
 - SOURCE (COMMON)
 - GATE
 - GATE
 - SOURCE (COMMON)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.098	0.106	2.49	2.69
A1	0.038	0.044	0.96	1.12
A2	0.040	0.042	1.02	1.07
D	0.926	0.934	23.52	23.72
D1	0.810 BSC		20.57 BSC	
D2	0.608 BSC		15.44 BSC	
E	0.492	0.500	12.50	12.70
E1	0.246	0.254	6.25	6.45
E2	0.170 BSC		4.32 BSC	
F	0.025 BSC		0.64 BSC	
P	0.126	0.134	3.20	3.40
b	0.105	0.111	2.67	2.82
b1	0.088	0.094	2.24	2.39
b2	0.066	0.072	1.68	1.83
b3	0.067	0.073	1.70	1.85
b4	0.077	0.083	1.96	2.11
c1	0.007	0.011	0.178	0.279
e	0.104 BSC		2.64 BSC	
e1	0.210 BSC		5.33 BSC	
e2	0.229 BSC		5.82 BSC	
aaa	0.004		0.10	
bbb	0.008		0.20	

**CASE 1366A-02
ISSUE A
TO-272 STRAIGHT LEAD
PLASTIC
MRF1570FT1**

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MRF1570T1/D