National Semiconductor

January 2004

LM4990 Boomer® Audio Power Amplifier Series
2 Watt Audio Power Amplifier with Selectable Shutdown Logic Level

General Description

The LM4990 is an audio power amplifier primarily designed for demanding applications in mobile phones and other portable communication device applications. It is capable of delivering 1.25 watts of continuous average power to an 8Ω BTL load and 2 watts of continuous average power (LD and MH only) to a 4Ω BTL load with less than 1% distortion (THD+N+N) from a $5V_{DC}$ power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. The LM4990 does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for mobile phone and other low voltage applications where minimal power consumption is a primary requirement.

The LM4990 features a low-power consumption shutdown mode. To facilitate this, Shutdown may be enabled by either logic high or low depending on mode selection. Driving the shutdown mode pin either high or low enables the shutdown pin to be driven in a likewise manner to enable shutdown.

The LM4990 contains advanced pop & click circuitry which eliminates noise which would otherwise occur during turn-on and turn-off transitions.

The LM4990 is unity-gain stable and can be configured by external gain-setting resistors.

Key Specifications

- Improved PSRR at 217Hz & 1KHz 62dB
- Power Output at 5.0V, 1% THD+N, 4Ω (LD and MH only) 2W (typ)
- Power Output at 5.0V, 1% THD+N, 8Ω 1.25W (typ)
- Power Output at 3.0V, 1% THD+N, 4Ω 600mW (typ)
- Power Output at 3.0V, 1% THD+N, 8Ω 425mW (typ)
- Shutdown Current 0.1µA (typ)

Features

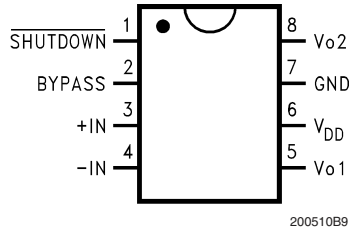
- Available in space-saving packages: LLP, Exposed-DAP TSSOP, MSOP, and ITL
- Ultra low current shutdown mode
- Improved pop & click circuitry eliminates noise during turn-on and turn-off transitions
- 2.2 - 5.5V operation
- No output coupling capacitors, snubber networks or bootstrap capacitors required
- Unity-gain stable
- External gain configuration capability
- User selectable shutdown High or Low logic Level

Applications

- Mobile Phones
- PDAs
- Portable electronic devices

Connection Diagrams

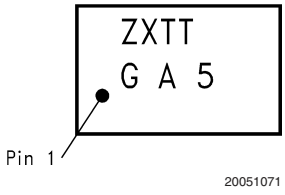
Mini Small Outline (MSOP) Package



200510B9

Top View
Order Number LM4990MM
See NS Package Number MUA08A

MSOP Marking



20051071

Top View
Z - Plant Code
X - Date Code
TT - Die Traceability
G - Boomer Family
A5 - LM4990MM

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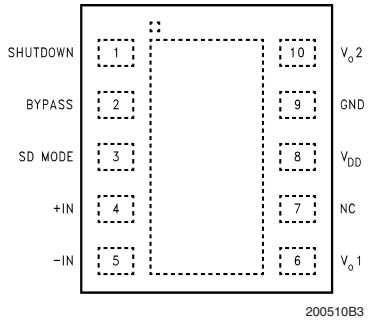
Connection Diagrams (Continued)

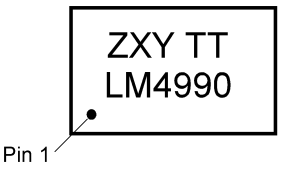
LLP Package



200510B3

Top View
Order Number LM4990LD
See NS Package Number LDA10B

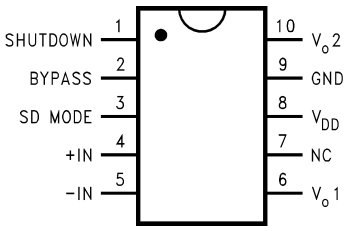
LLP Marking



200510B4

Top View
Z - Plant Code
XY - Date Code
TT - Die Traceability
Bottom Line - Part Number

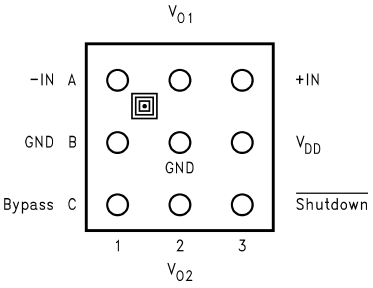
Exposed-DAP TSSOP Package



20051096

Top View
Order Number LM4990MH
See NS Package Number MXF10A

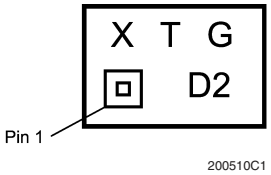
9 Bump micro SMD



200510C0

Top View
Order Number LM4990ITL, LM4990ITLX
See NS Package Number TLA09ZZA

9 Bump micro SMD Marking



200510C1

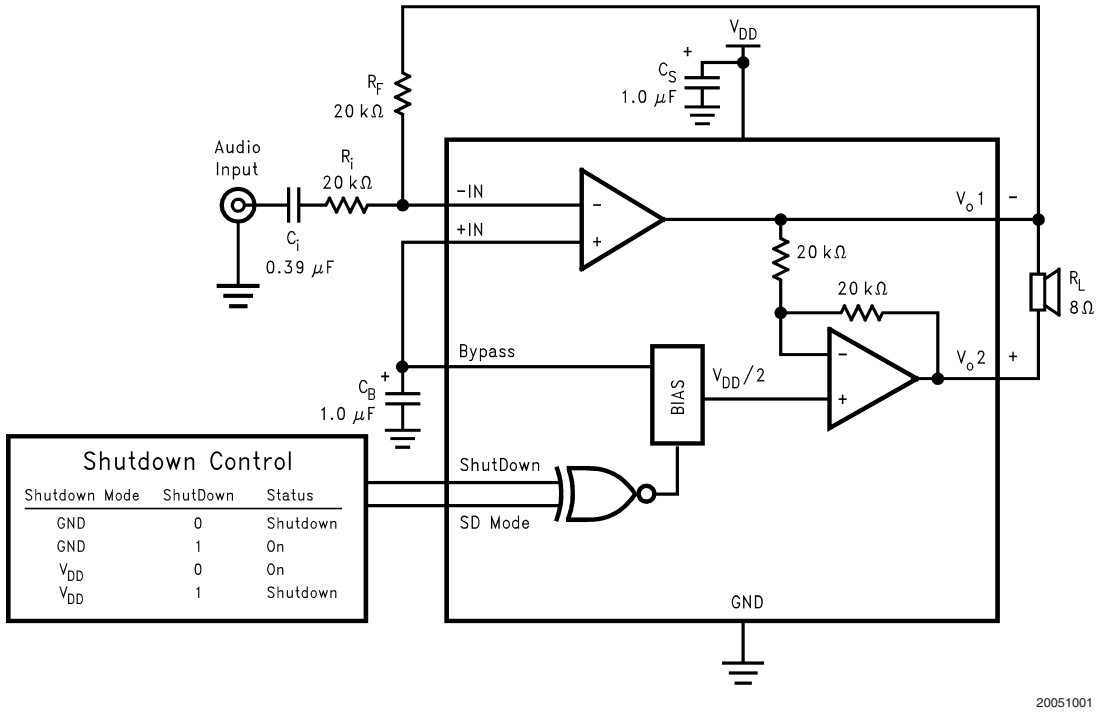
Top View
X — Date Code
T — Die Traceability
G — Boomer Family
D2 — LM4990ITL

Package	LD	MH	MM	ITL
Shutdown Mode	Selectable	Selectable	Low	Low
Typical Power Output at 5V, 1% THD+N	2W (R_L = 4Ω)	2W (R_L = 4Ω)	1.25W (R_L = 8Ω)	1.25W (R_L = 8Ω)

. A SD_MODE select pin determines the Shutdown Mode for the LD and MH packages, whether it is an Asserted High or an Asserted Low device, to activate shutdown.

. The SD_MODE select pin is not available with the MM and ITL packaged devices. Shutdown occurs only with a low assertion.

Typical Application



Note: MM and ITL packaged devices are active low only; Shutdown Mode pin is internally tied to GND.

FIGURE 1. Typical Audio Amplifier Application Circuit (LD and MH)

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 11)	6.0V
Storage Temperature	−65˚C to +150˚C
Input Voltage	−0.3V to V_{DD} +0.3V
Power Dissipation (Notes 3, 12)	Internally Limited
ESD Susceptibility (Note 4)	2000V
ESD Susceptibility (Note 5)	200V
Junction Temperature	150˚C
Thermal Resistance	
θ_{JC} (MSOP)	56˚C/W
θ_{JA} (MSOP)	190˚C/W
θ_{JA} (9 Bump micro SMD) (Note 15)	180˚C/W
θ_{JA} (LLP)	63˚C/W (Note 13)
θ_{JC} (LLP)	12˚C/W (Note 13)
Soldering Information	
See AN-1187 "Leadless Leadframe Package (LLP)."	

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-40˚C \le T_A \le 85˚C$
Supply Voltage	$2.2V \le V_{DD} \le 5.5V$

Electrical Characteristics V_{DD} = 5V (Notes 1, 2)

The following specifications apply for the circuit shown in Figure 1, unless otherwise specified. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4990		Units (Limits)
			Typical (Note 6)	Limit (Notes 7, 9)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_o = 0A, No Load	3	7	mA (max)
		V_{IN} = 0V, I_o = 0A, 8Ω Load	4	10	mA (max)
I_{SD}	Shutdown Current	$V_{SD} = V_{SD\ Mode}$ (Note 8)	0.1	2.0	µA (max)
V_{SDIH}	Shutdown Voltage Input High	$V_{SD\ MODE} = V_{DD}$	1.5		V
V_{SDIL}	Shutdown Voltage Input Low	$V_{SD\ MODE} = V_{DD}$	1.3		V
V_{SDIH}	Shutdown Voltage Input High	$V_{SD\ MODE}$ = GND	1.5		V
V_{SDIL}	Shutdown Voltage Input Low	$V_{SD\ MODE}$ = GND	1.3		V
V_{OS}	Output Offset Voltage		7	50	mV (max)
R_{OUT}	Resistor Output to GND (Note 10)		8.5	9.7	kΩ (max)
				7.0	kΩ (min)
P_o	Output Power (8Ω)	THD+N = 1% (max); f = 1kHz	1.25	0.9	W (min)
	(4Ω) (Notes 13, 14)	THD+N = 1% (max); f = 1kHz	2		W
T_{WU}	Wake-up time		100		ms
THD+N+N	Total Harmonic Distortion+Noise	P_o = 0.5Wrms; f = 1kHz	0.2		%
PSRR	Power Supply Rejection Ratio	V_{ripple} = 200mV sine p-p Input terminated with 10Ω	60 (f = 217Hz) 64 (f = 1kHz)	55	dB (min)

Electrical Characteristics V_{DD} = 3V (Notes 1, 2)

The following specifications apply for the circuit shown in Figure 1, unless otherwise specified. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4990		Units (Limits)
			Typical (Note 6)	Limit (Notes 7, 9)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_o = 0A, No Load	2	7	mA (max)
		V_{IN} = 0V, I_o = 0A, 8Ω Load	3	9	mA (max)
I_{SD}	Shutdown Current	$V_{SD} = V_{SD\ Mode}$ (Note 8)	0.1	2.0	µA (max)
V_{SDIH}	Shutdown Voltage Input High	$V_{SD\ MODE} = V_{DD}$	1.1		V
V_{SDIL}	Shutdown Voltage Input Low	$V_{SD\ MODE} = V_{DD}$	0.9		V
V_{SDIH}	Shutdown Voltage Input High	$V_{SD\ MODE}$ = GND	1.3		V
V_{SDIL}	Shutdown Voltage Input Low	$V_{SD\ MODE}$ = GND	1.0		V
V_{OS}	Output Offset Voltage		7	50	mV (max)
R_{OUT}	Resistor Output to GND (Note 10)		8.5	9.7	kΩ (max)
				7.0	kΩ (min)

Electrical Characteristics V_{DD} = 3V (Notes 1, 2)

The following specifications apply for the circuit shown in Figure 1, unless otherwise specified. Limits apply for T_A = 25˚C. (Continued)

Symbol	Parameter	Conditions	LM4990		Units (Limits)
			Typical	Limit	
			(Note 6)	(Notes 7, 9)	
P_o	Output Power (8Ω)	THD+N = 1% (max); f = 1kHz	425		mW
	(4Ω)	THD+N = 1% (max); f = 1kHz	600		mW
T_{WU}	Wake-up time		75		ms
THD+N+N	Total Harmonic Distortion+Noise	P_o = 0.25Wrms; f = 1kHz	0.1		%
PSRR	Power Supply Rejection Ratio	V_{ripple} = 200mV sine p-p Input terminated with 10Ω	62 (f = 217Hz) 68 (f = 1kHz)	55	dB (min)

Electrical Characteristics V_{DD} = 2.6V (Notes 1, 2)

The following specifications apply for the circuit shown in Figure 1, unless otherwise specified. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4990		Units (Limits)
			Typical	Limit	
			(Note 6)	(Notes 7, 9)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_o = 0A, No Load	2.0		mA
		V_{IN} = 0V, I_o = 0A, 8Ω Load	3.0		mA
I_{SD}	Shutdown Current	V_{SD} = $V_{SD\ Mode}$ (Note 8)	0.1		µA
V_{SDIH}	Shutdown Voltage Input High	$V_{SD\ MODE}$ = V_{DD}	1.0		V
V_{SDIL}	Shutdown Voltage Input Low	$V_{SD\ MODE}$ = V_{DD}	0.9		V
V_{SDIH}	Shutdown Voltage Input High	$V_{SD\ MODE}$ = GND	1.2		V
V_{SDIL}	Shutdown Voltage Input Low	$V_{SD\ MODE}$ = GND	1.0		V
V_{OS}	Output Offset Voltage		5	50	mV (max)
R_{OUT}	Resistor Output to GND (Note 10)		8.5	9.7	kΩ (max)
				7.0	kΩ (min)
P_o	Output Power (8Ω)	THD+N = 1% (max); f = 1kHz	300		mW
	(4Ω)	THD+N = 1% (max); f = 1kHz	400		
T_{WU}	Wake-up time		70		ms
THD+N+N	Total Harmonic Distortion+Noise	P_o = 0.15Wrms; f = 1kHz	0.1		%
PSRR	Power Supply Rejection Ratio	V_{ripple} = 200mV sine p-p Input terminated with 10Ω	51 (f = 217Hz) 51 (f = 1kHz)		dB

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX}–T_A)/\theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4990, see power derating curves for additional information.

Note 4: Human body model, 100pF discharged through a 1.5kΩ resistor.

Note 5: Machine Model, 220pF – 240pF discharged through all pins.

Note 6: Typicals are measured at 25˚C and represent the parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: For micro SMD only, shutdown current is measured in a Normal Room Environment. Exposure to direct sunlight will increase I_{SD} by a maximum of 2µA.

Note 9: Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

Note 10: R_{ROUT} is measured from the output pin to ground. This value represents the parallel combination of the 10kΩ output resistors and the two 20kΩ resistors.

Note 11: If the product is in Shutdown mode and V_{DD} exceeds 6V (to a max of 8V V_{DD}), then most of the excess current will flow through the ESD protection circuits. If the source impedance limits the current to a max of 10mA, then the device will be protected. If the device is enabled when V_{DD} is greater than 5.5V and less than 6.5V, no damage will occur, although operation life will be reduced. Operation above 6.5V with no current limit will result in permanent damage.

Note 12: Maximum power dissipation in the device (P_{DMAX}) occurs at an output power level significantly below full output power. P_{DMAX} can be calculated using Equation 1 shown in the **Application Information** section. It may also be obtained from the power dissipation graphs.

Electrical Characteristics V_{DD} = 2.6V (Notes 1, 2)

The following specifications apply for the circuit shown in Figure 1, unless otherwise specified. Limits apply for T_A = 25˚C. (Continued)

Note 13: The Exposed-DAP of the LDA10B package should be electrically connected to GND or an electrically isolated copper area. the LM4990LD demo board has the Exposed-DAP connected to GND with a PCB area of 86.7mils x 585mils (2.02mm x 14.86mm) on the copper top layer and 550mils x 710mils (13.97mm x 18.03mm) on the copper bottom layer.

Note 14: The thermal performance of the LLP and exposed-DAP TSSOP packages when used with the exposed-DAP connected to a thermal plane is sufficient for driving 4Ω loads. The MSOP and ITL packages do not have the thermal performance necessary for driving 4Ω loads with a 5V supply and is not recommended for this application.

Note 15: All bumps have the same thermal resistance and contribute equally when used to lower thermal resistance. All bumps must be connected to achieve specified thermal resistance.

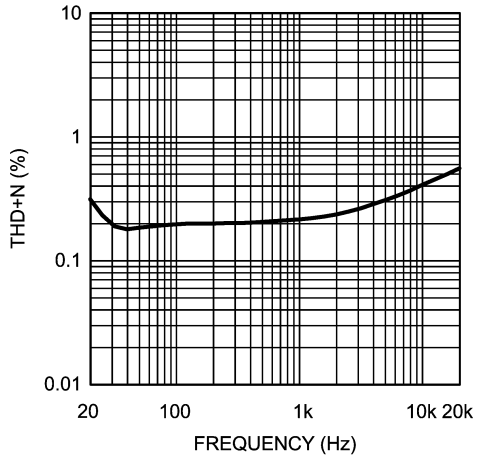
External Components Description

See (*Figure 1*)

Components		Functional Description
1.	R_i	Inverting input resistance which sets the closed-loop gain in conjunction with R_f. This resistor also forms a high pass filter with C_i at $f_C = 1/(2\pi R_i C_i)$.
2.	C_i	Input coupling capacitor which blocks the DC voltage at the amplifiers input terminals. Also creates a highpass filter with R_i at $f_c = 1/(2\pi R_i C_i)$. Refer to the section, **Proper Selection of External Components**, for an explanation of how to determine the value of C_i.
3.	R_f	Feedback resistance which sets the closed-loop gain in conjunction with R_i.
4.	C_S	Supply bypass capacitor which provides power supply filtering. Refer to the **Power Supply Bypassing** section for information concerning proper placement and selection of the supply bypass capacitor.
5.	C_B	Bypass pin capacitor which provides half-supply filtering. Refer to the section, **Proper Selection of External Components**, for information concerning proper placement and selection of C_B.

Typical Performance Characteristics
LD and MH Specific Characteristics

THD+N+N vs Frequency
V_{DD} = 5V, R_L = 4Ω, and P_O = 1W



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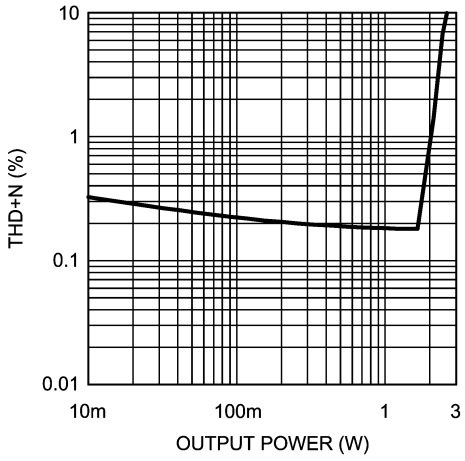
THD+N+N vs Output Power
V_{DD} = 5V, R_L = 4Ω, and f = 1 kHz



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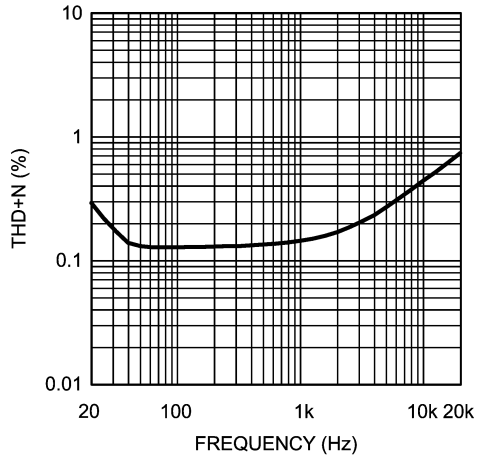
Typical Performance Characteristics

THD+N+N vs Frequency
V_{DD} = 5V, R_L = 8Ω, and P_O = 500mW



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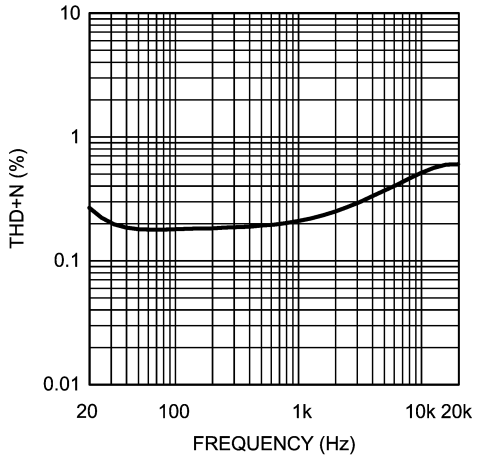
THD+N+N vs Frequency
V_{DD} = 3V, R_L = 4Ω, and P_O = 500mW



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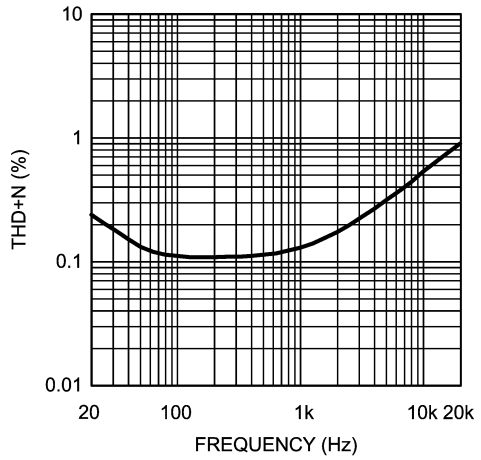
THD+N+N vs Frequency
V_{DD} = 3V, R_L = 8Ω, and P_O = 250mW



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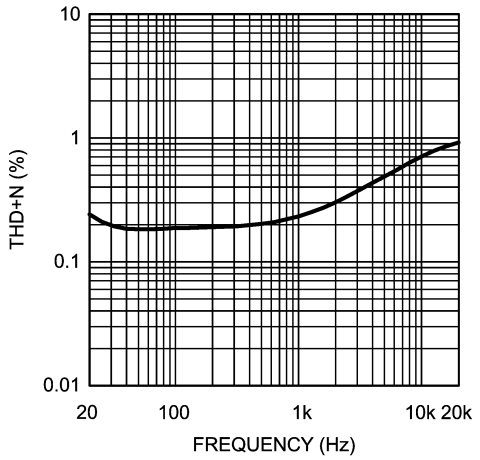
THD+N+N vs Frequency
V_{DD} = 2.6V, R_L = 4Ω, and P_O = 150mW



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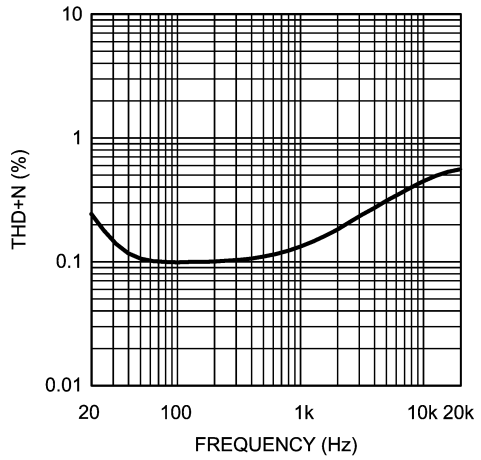
THD+N+N vs Output Power
V_{DD} = 2.6V, R_L = 8Ω, and P_O = 150mW



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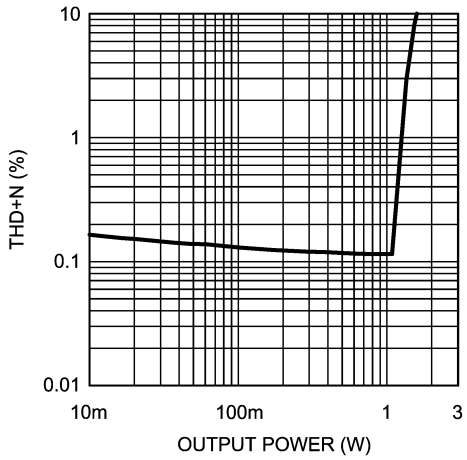
THD+N+N vs Output Power
V_{DD} = 5V, R_L = 8Ω, and f = 1kHz



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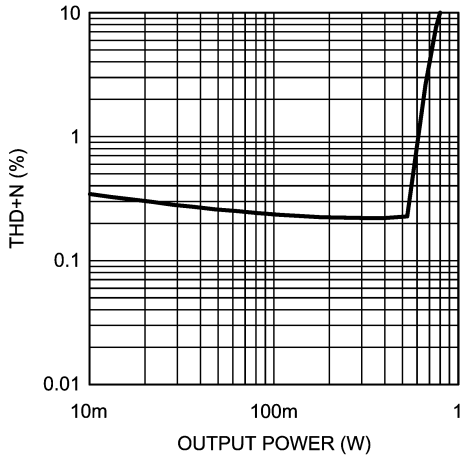
Typical Performance Characteristics (Continued)

THD+N+N vs Output Power
V_{DD} = 3V, R_L = 4Ω, and f = 1kHz



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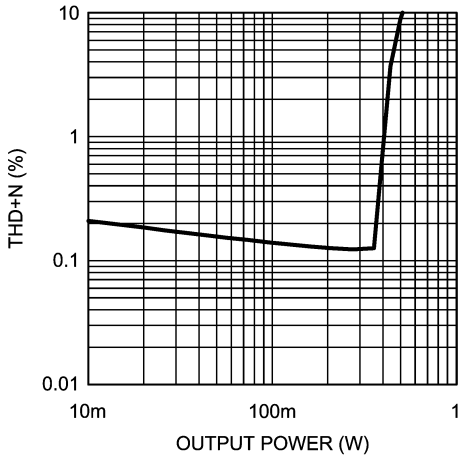
THD+N+N vs Output Power
V_{DD} = 3V, R_L = 8Ω, and f = 1kHz



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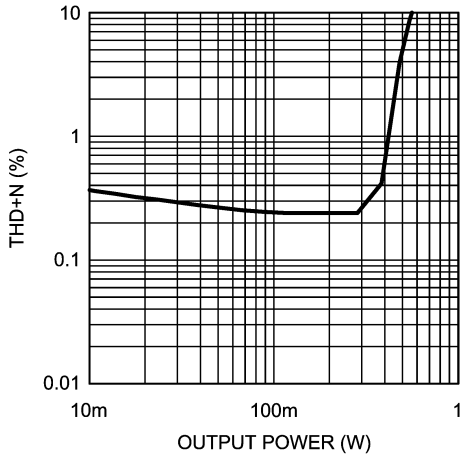
THD+N+N vs Output Power
V_{DD} = 2.6V, R_L = 4Ω, and f = 1kHz



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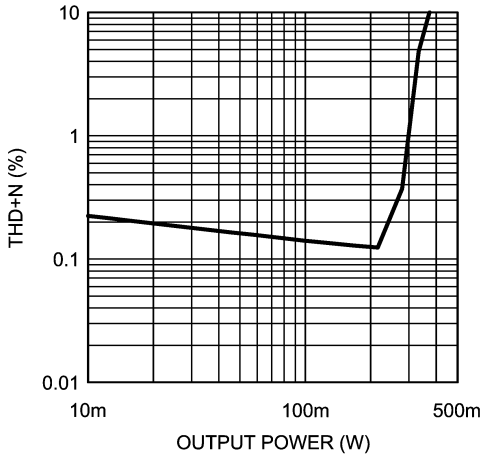
THD+N+N vs Output Power
V_{DD} = 2.6V, R_L = 8Ω, and f = 1kHz



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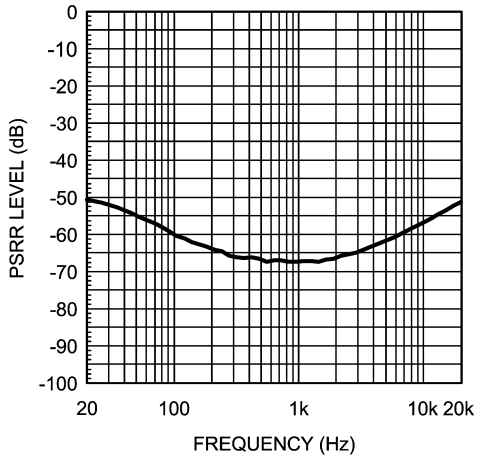
Power Supply Rejection Ratio (PSRR) vs Frequency
V_{DD} = 5V, R_L = 8Ω, input 10Ω terminated



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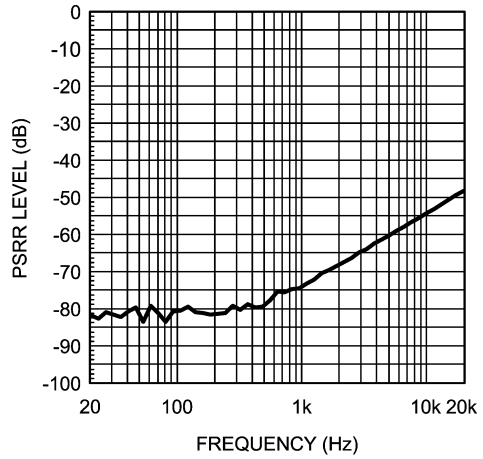
Power Supply Rejection Ratio (PSRR) vs Frequency
V_{DD} = 5V, R_L = 8Ω, input floating



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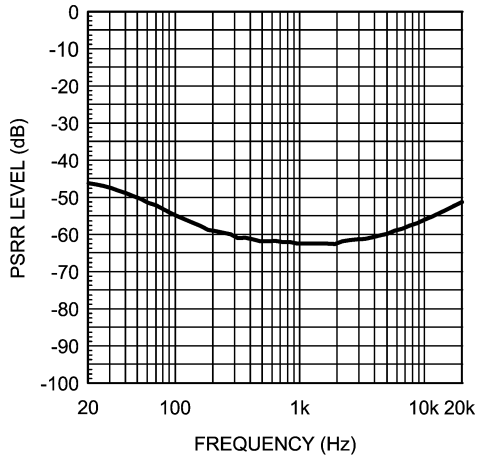
Typical Performance Characteristics (Continued)

Power Supply Rejection Ratio (PSRR) vs Frequency
V_{DD} = 3V, R_L = 8Ω, input 10Ω terminated



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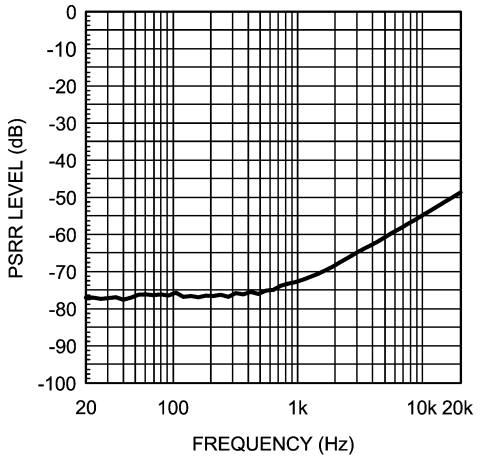
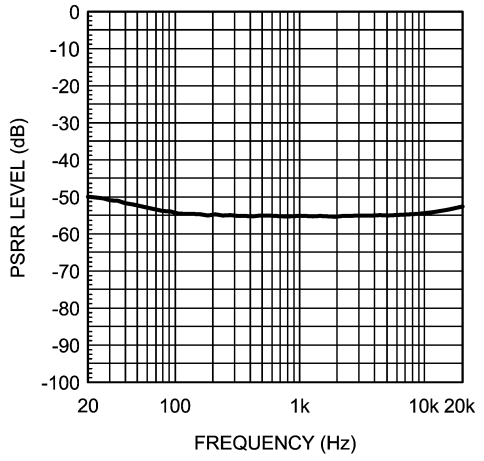
Power Supply Rejection Ratio (PSRR) vs Frequency
V_{DD} = 3V, R_L = 8Ω, input floating



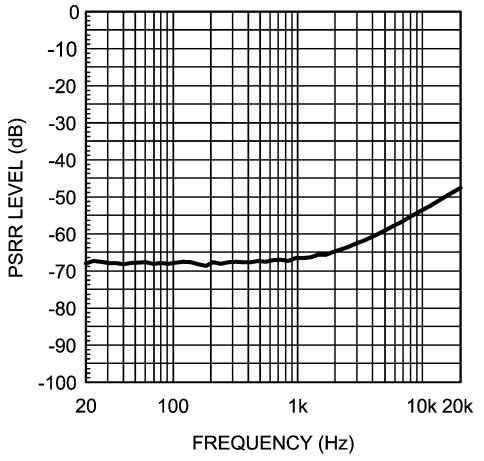
20051087

Power Supply Rejection Ratio (PSRR) vs Frequency
V_{DD} = 2.6V, R_L = 8Ω, input 10Ω terminated



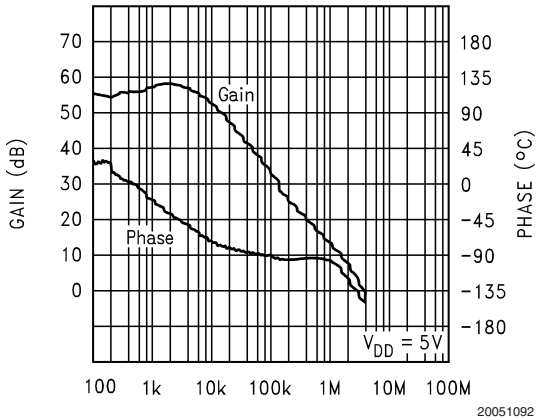
20051088

Power Supply Rejection Ratio (PSRR) vs Frequency
V_{DD} = 2.6V, R_L = 8Ω, Input Floating



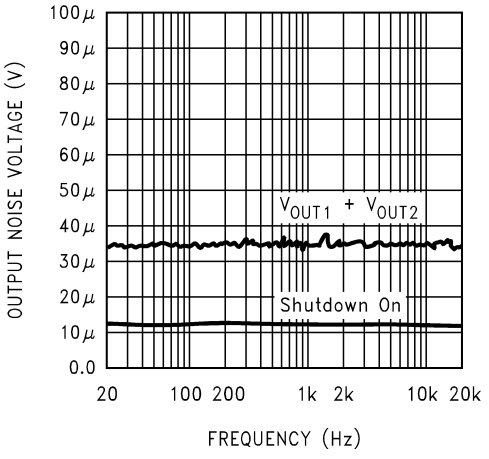
20051089

Open Loop Frequency Response, 5V



20051092

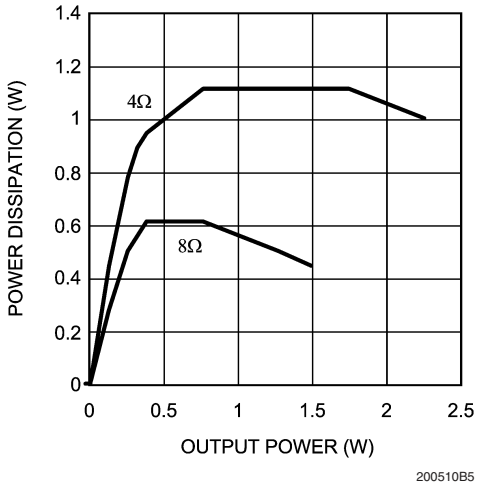
Noise Floor, 5V, 8Ω
80kHz Bandwidth, Input to GND



20051095

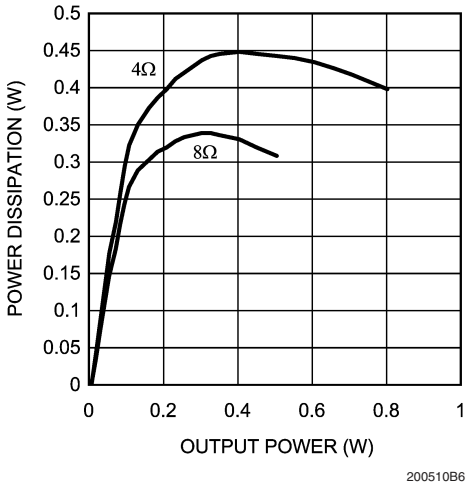
Typical Performance Characteristics (Continued)

Power Dissipation vs Output Power, V_{DD} = 5V



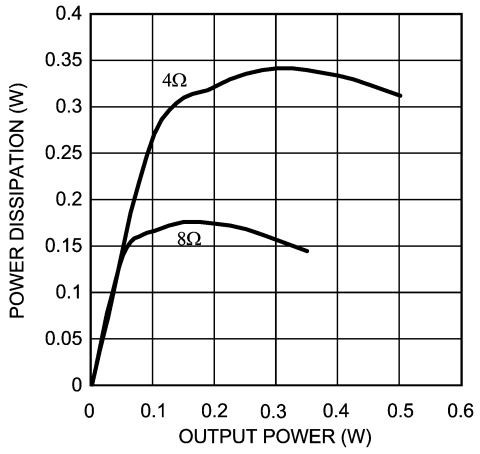
200510B5

Power Dissipation vs Output Power, V_{DD} = 3V



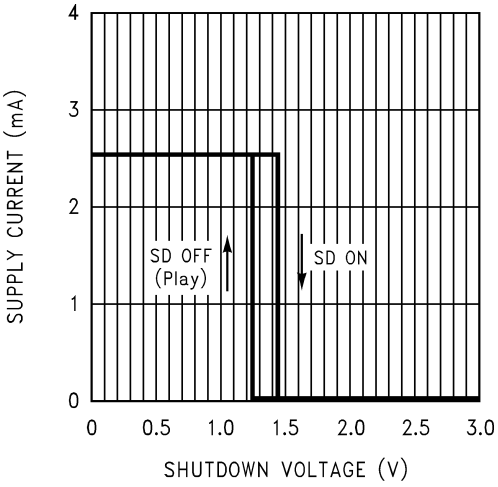
200510B6

Power Dissipation vs Output Power, V_{DD} = 2.6V



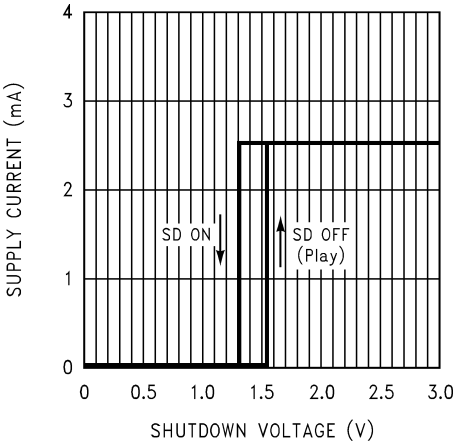
200510B7

Shutdown Hysteresis Voltage V_{DD} = 5V, SD Mode = V_{DD}



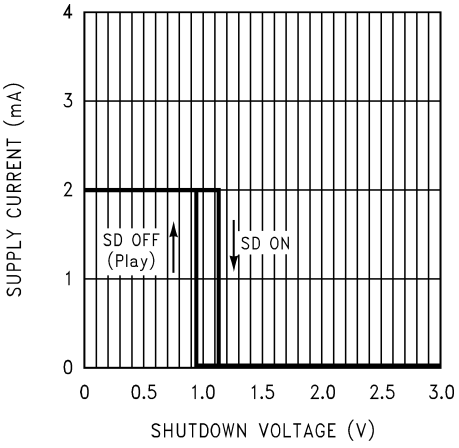
200510A0

Shutdown Hysteresis Voltage V_{DD} = 5V, SD Mode = GND



200510A1

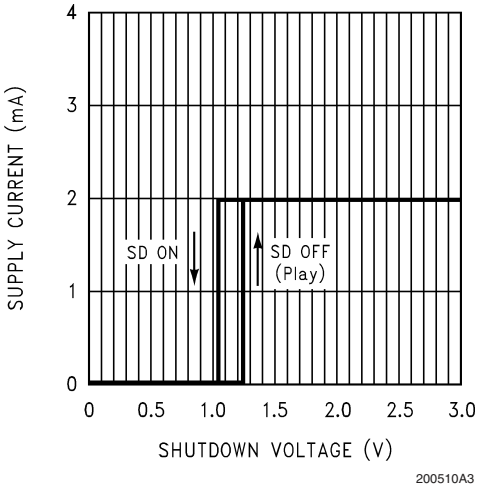
Shutdown Hysteresis Voltage V_{DD} = 3V, SD Mode = V_{DD}



200510A2

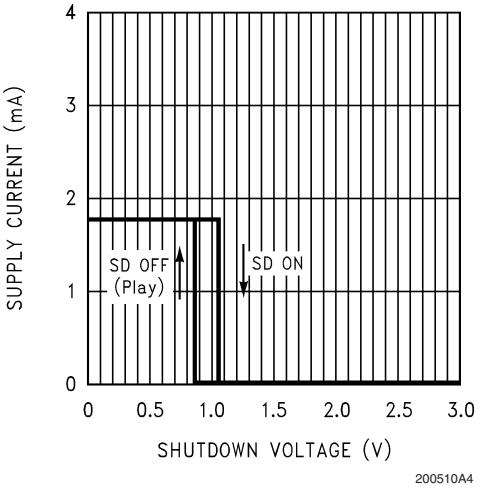
Typical Performance Characteristics (Continued)

Shutdown Hysteresis Voltage
V_{DD} = 3V, SD Mode = GND



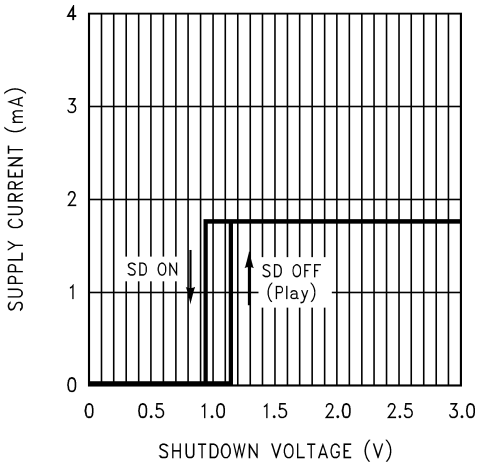
200510A3

Shutdown Hysteresis Voltage
V_{DD} = 2.6V, SD Mode = V_{DD}



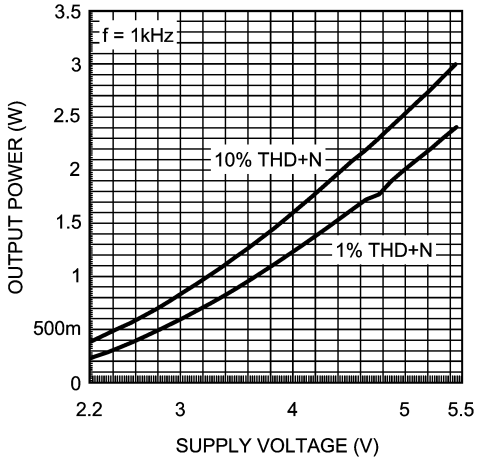
200510A4

Shutdown Hysteresis Voltage
V_{DD} = 2.6V, SD Mode = GND



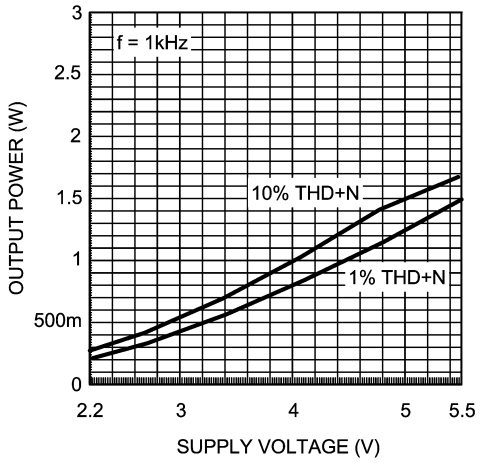
200510A5

Output Power vs
Supply Voltage, R_L = 4Ω



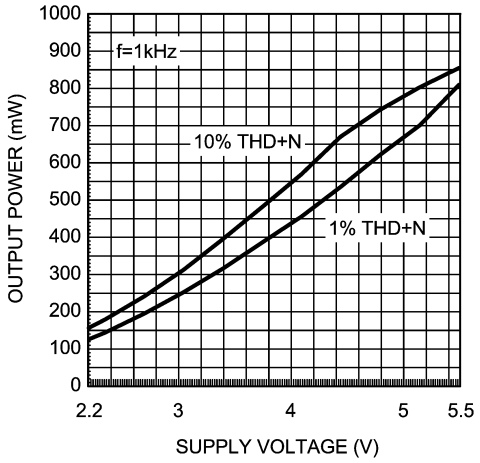
200510B8

Output Power vs
Supply Voltage, R_L = 8Ω



200510A6

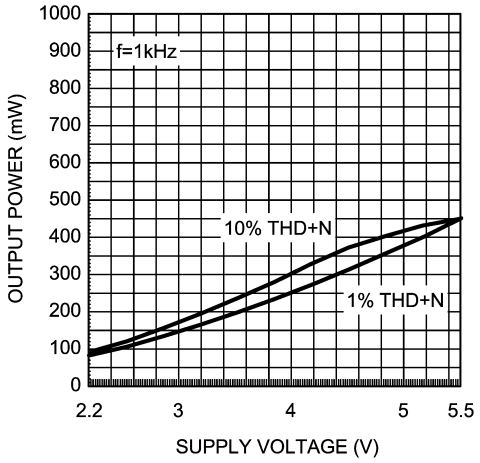
Output Power vs
Supply Voltage, R_L = 16Ω



200510A7

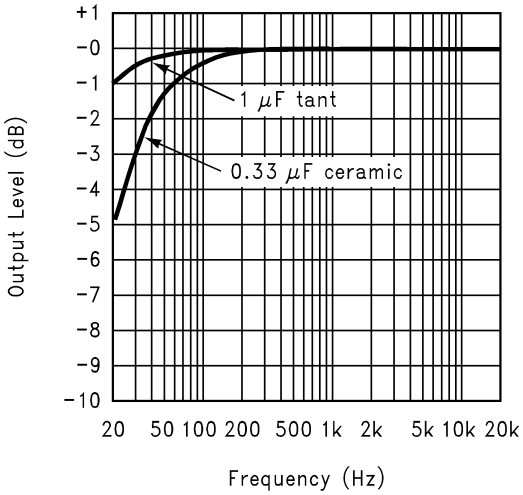
Typical Performance Characteristics (Continued)

Output Power vs Supply Voltage, R_L = 32Ω



200510A8

Frequency Response vs Input Capacitor Size



20051054

Application Information

BRIDGE CONFIGURATION EXPLANATION

As shown in *Figure 1*, the LM4990 has two internal operational amplifiers. The first amplifier's gain is externally configurable, while the second amplifier is internally fixed in a unity-gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of R_f to R_i while the second amplifier's gain is fixed by the two internal 20kΩ resistors. *Figure 1* shows that the output of amplifier one serves as the input to amplifier two which results in both amplifiers producing signals identical in magnitude, but out of phase by 180˚. Consequently, the differential gain for the IC is

$$A_{VD} = 2 * (R_f / R_i)$$

By driving the load differentially through outputs Vo1 and Vo2, an amplifier configuration commonly referred to as "bridged mode" is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of the load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive clipping, please refer to the **Audio Power Amplifier Design** section.

A bridge configuration, such as the one used in LM4990, also creates a second advantage over single-ended amplifiers. Since the differential outputs, Vo1 and Vo2, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor, the half-supply bias across the load would result in both increased internal IC power dissipation and also possible loudspeaker damage.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Since the LM4990 has two operational amplifiers in one package, the maximum internal power dissipation is 4 times that of a single-ended amplifier. The maximum power dissipation for a given application can be derived from the power dissipation graphs or from Equation 1.

$$P_{DMAX} = 4*(V_{DD})^2/(2\pi^2 R_L) \quad (1)$$

It is critical that the maximum junction temperature T_{JMAX} of 150˚C is not exceeded. T_{JMAX} can be determined from the power derating curves by using P_{DMAX} and the PC board foil area. By adding copper foil, the thermal resistance of the application can be reduced from the free air value of θ_{JA}, resulting in higher P_{DMAX} values without thermal shutdown protection circuitry being activated. Additional copper foil can be added to any of the leads connected to the LM4990. It is especially effective when connected to V_{DD}, GND, and the output pins. Refer to the application information on the LM4990 reference design board for an example of good heat sinking. If T_{JMAX} still exceeds 150˚C, then additional changes must be made. These changes can include reduced supply voltage, higher load impedance, or reduced ambient temperature. Internal power dissipation is a function of output power. Refer to the **Typical Performance Characteristics** curves for power dissipation information for different output powers and output loading.

POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. Typical applications employ a 5V regulator with 10µF tantalum or electrolytic capacitor and a ceramic bypass capacitor which aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the LM4990. The selection of a bypass capacitor, especially C_B, is dependent upon PSRR requirements, click and pop performance (as explained in the section, **Proper Selection of External Components**), system cost, and size constraints.

SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the LM4990 contains shutdown circuitry that is used to turn off the amplifier's bias circuitry. In addition, the LM4990 contains a Shutdown Mode pin (LD and MH packages only), allowing the designer to designate whether the part will be driven into shutdown with a high level logic signal or a low level logic signal. This allows the designer maximum flexibility in device use, as the Shutdown Mode pin may simply be tied permanently to either V_{DD} or GND to set the LM4990 as either a "shutdown-high" device or a "shutdown-low" device, respectively. The device may then be placed into shutdown mode by toggling the Shutdown pin to the same state as the Shutdown Mode pin. For simplicity's sake, this is called "shutdown same", as the LM4990 enters shutdown mode whenever the two pins are in the same logic state. The MM package lacks this Shutdown Mode feature, and is permanently fixed as a 'shutdown-low' device. The trigger point for either shutdown high or shutdown low is shown as a typical value in the Supply Current vs Shutdown Voltage graphs in the **Typical Performance Characteristics** section. It is best to switch between ground and supply for maximum performance. While the device may be disabled with shutdown voltages in between ground and supply, the idle current may be greater than the typical value of 0.1µA. In either case, the shutdown pin should be tied to a definite voltage to avoid unwanted state changes.

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry, which provides a quick, smooth transition to shutdown. Another solution is to use a single-throw switch in conjunction with an external pull-up resistor (or pull-down, depending on shutdown high or low application). This scheme guarantees that the shutdown pin will not float, thus preventing unwanted state changes.

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical to optimize device and system performance. While the LM4990 is tolerant of

Application Information (Continued)

external component combinations, consideration to component values must be used to maximize overall system quality.

The LM4990 is unity-gain stable which gives the designer maximum system flexibility. The LM4990 should be used in low gain configurations to minimize THD+N+N values, and maximize the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1Vrms are available from sources such as audio codecs. Please refer to the section, **Audio Power Amplifier Design**, for a more complete explanation of proper gain selection.

Besides gain, one of the major considerations is the closed-loop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in *Figure 1*. The input coupling capacitor, C_i, forms a first order high pass filter which limits low frequency response. This value should be chosen based on needed frequency response for a few distinct reasons.

Selection of Input Capacitor Size

Large input capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is needed to couple in low frequencies without severe attenuation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100Hz to 150Hz. Thus, using a large input capacitor may not increase actual system performance.

In addition to system cost and size, click and pop performance is effected by the size of the input coupling capacitor, C_i. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally 1/2 V_{DD}). This charge comes from the output via the feedback and is apt to create pops upon device enable. Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized.

Besides minimizing the input capacitor size, careful consideration should be paid to the bypass capacitor value. Bypass capacitor, C_B, is the most critical component to minimize turn-on pops since it determines how fast the LM4990 turns on. The slower the LM4990's outputs ramp to their quiescent DC voltage (nominally 1/2 V_{DD}), the smaller the turn-on pop. Choosing C_B equal to 1.0µF along with a small value of C_i (in the range of 0.1µF to 0.39µF), should produce a virtually clickless and popless shutdown function. While the device will function properly, (no oscillations or motorboating), with C_B equal to 0.1µF, the device will be much more susceptible to turn-on clicks and pops. Thus, a value of C_B equal to 1.0µF is recommended in all but the most cost sensitive designs.

AUDIO POWER AMPLIFIER DESIGN

A 1W/8Ω Audio Amplifier

Given:

Power Output	1Wrms
Load Impedance	8Ω
Input Level	1Vrms
Input Impedance	20kΩ
Bandwidth	100Hz–20kHz ± 0.25dB

A designer must first determine the minimum supply rail to obtain the specified output power. By extrapolating from the Output Power vs Supply Voltage graphs in the **Typical Performance Characteristics** section, the supply rail can be easily found.

5V is a standard voltage in most applications, it is chosen for the supply rail. Extra supply voltage creates headroom that allows the LM4990 to reproduce peaks in excess of 1W without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the **Power Dissipation** section.

Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation 2.

$$A_{VD} \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (2)$$

$$R_f/R_i = A_{VD}/2$$

From Equation 2, the minimum A_{VD} is 2.83; use A_{VD} = 3.

Since the desired input impedance was 20kΩ, and with a A_{VD} impedance of 2, a ratio of 1.5:1 of R_f to R_i results in an allocation of R_i = 20kΩ and R_f = 30kΩ. The final design step is to address the bandwidth requirements which must be stated as a pair of –3dB frequency points. Five times away from a –3dB point is 0.17dB down from passband response which is better than the required ±0.25dB specified.

f_L = 100Hz/5 = 20Hz

f_H = 20kHz * 5 = 100kHz

As stated in the **External Components** section, R_i in conjunction with C_i create a highpass filter.

$C_i \geq 1/(2\pi * 20k\Omega * 20Hz) = 0.397\mu F$; use 0.39µF

The high frequency pole is determined by the product of the desired frequency pole, f_H, and the differential gain, A_{VD}. With a A_{VD} = 3 and f_H = 100kHz, the resulting GBWP = 300kHz which is much smaller than the LM4990 GBWP of 2.5MHz. This figure displays that if a designer has a need to design an amplifier with a higher differential gain, the LM4990 can still be used without running into bandwidth limitations.

Application Information (Continued)

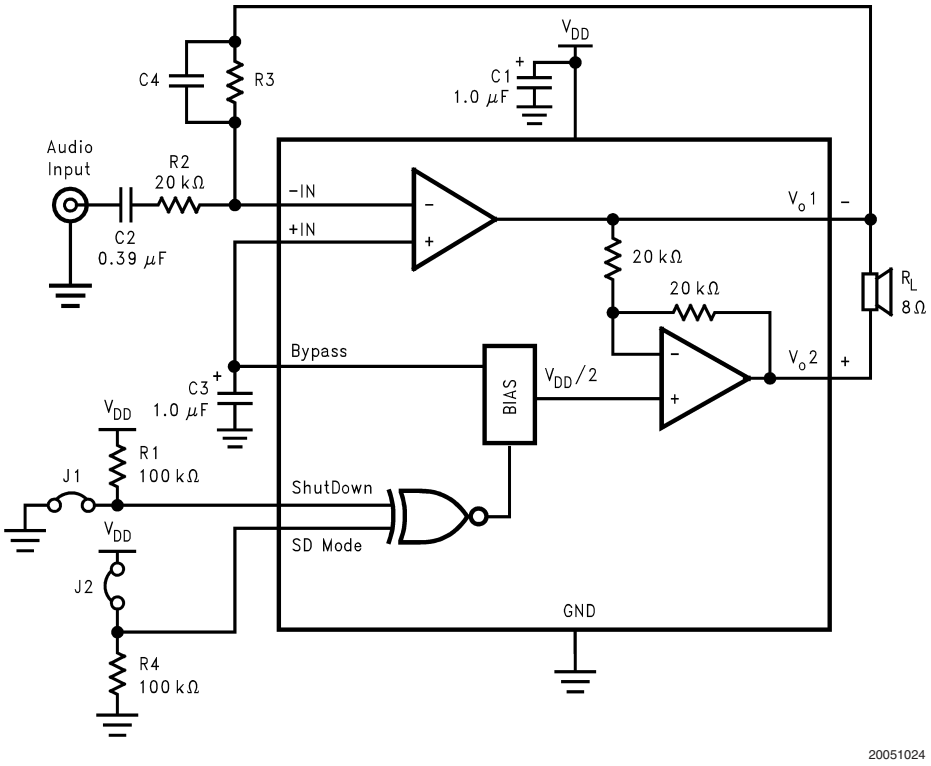


FIGURE 2. HIGHER GAIN AUDIO AMPLIFIER

The LM4990 is unity-gain stable and requires no external components besides gain-setting resistors, an input coupling capacitor, and proper supply bypassing in the typical application. However, if a closed-loop differential gain of greater than 10 is required, a feedback capacitor (C4) may be needed as shown in Figure 2 to bandwidth limit the amplifier. This feedback capacitor creates a low pass filter that eliminates possible high frequency oscillations. Care should be taken when calculating the -3dB frequency in that an incorrect combination of R_3 and C_4 will cause rolloff before 20kHz. A typical combination of feedback resistor and capacitor that will not produce audio band high frequency rolloff is R_3 = 20kΩ and C_4 = 25pf. These components result in a -3dB point of approximately 320kHz.

Application Information (Continued)

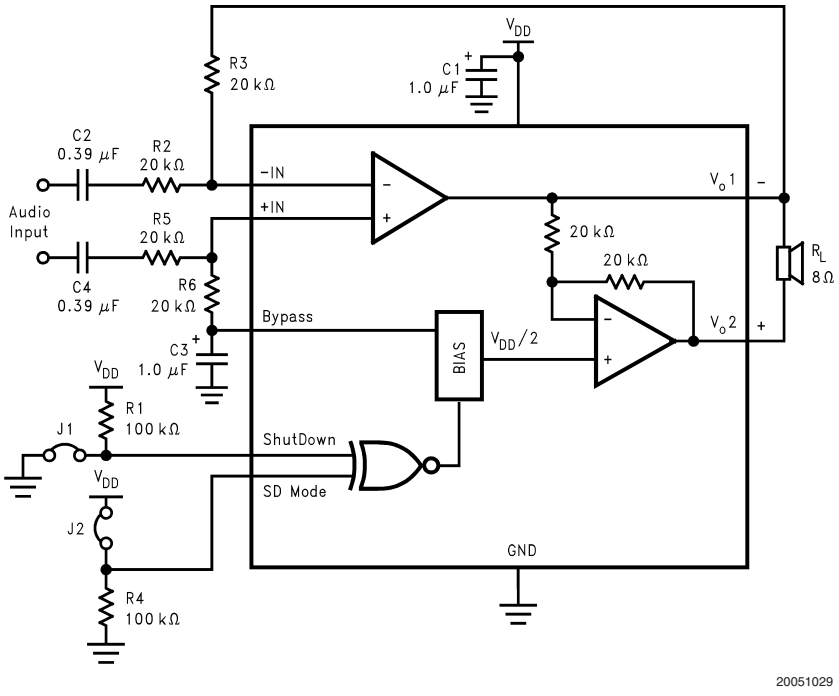


FIGURE 3. DIFFERENTIAL AMPLIFIER CONFIGURATION FOR LM4990

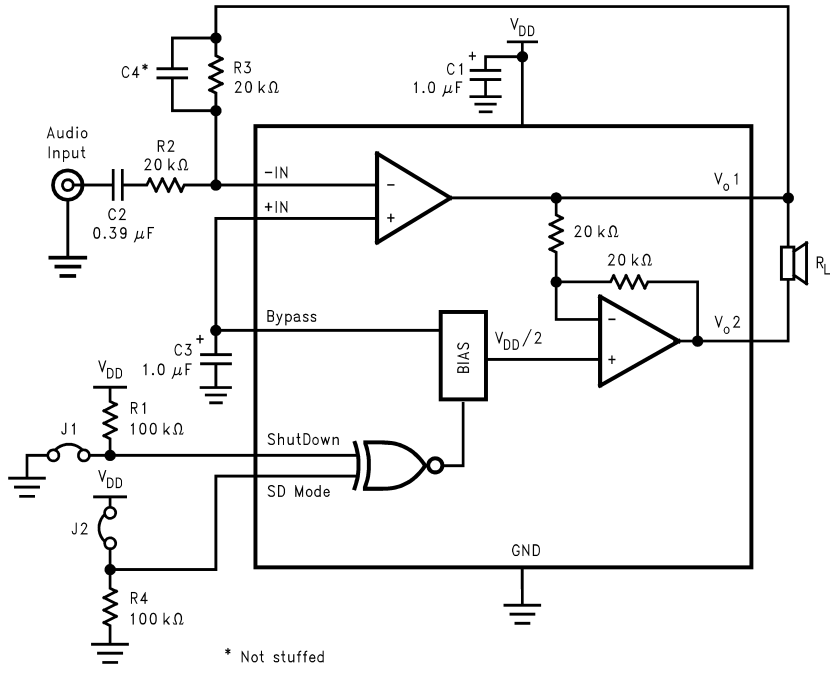
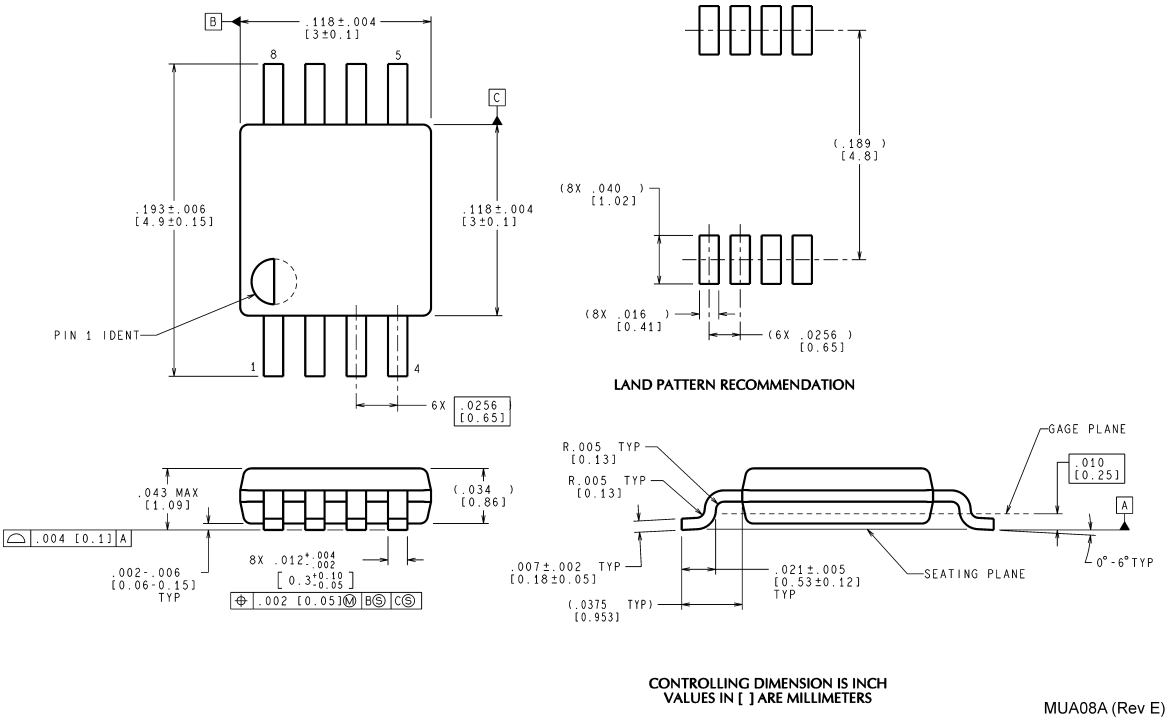


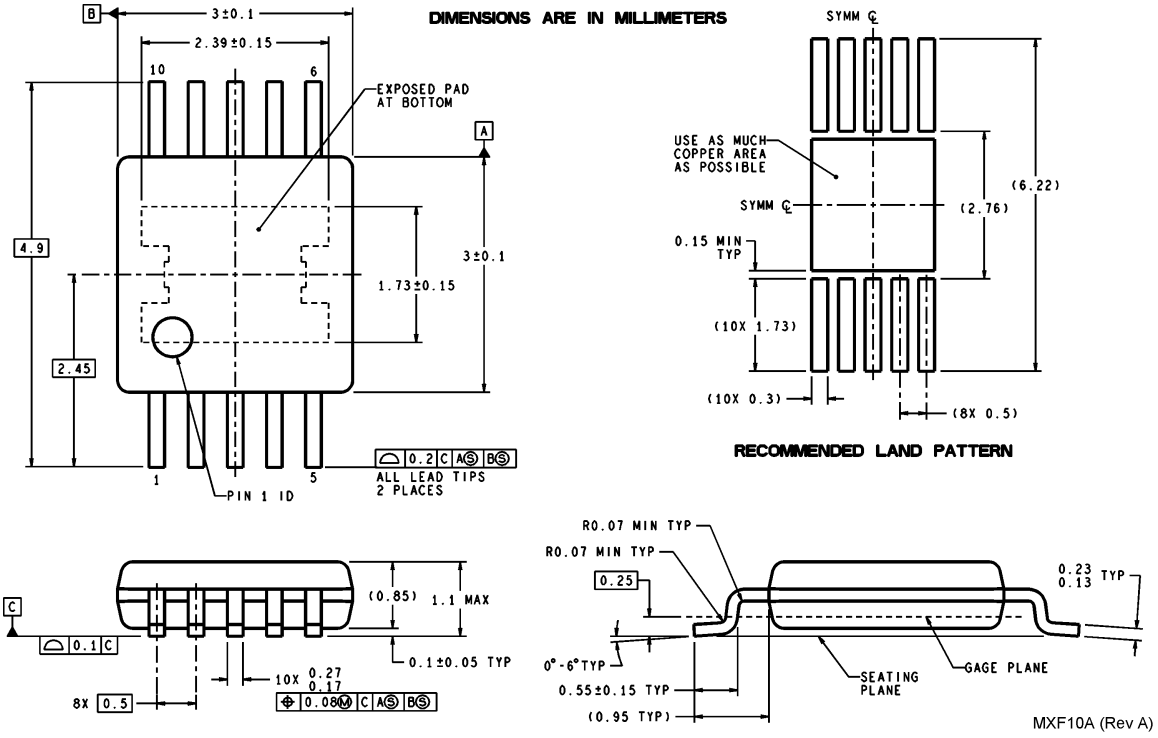
FIGURE 4. REFERENCE DESIGN BOARD SCHEMATIC

Physical Dimensions inches (millimeters) unless otherwise noted



MUA08A (Rev E)

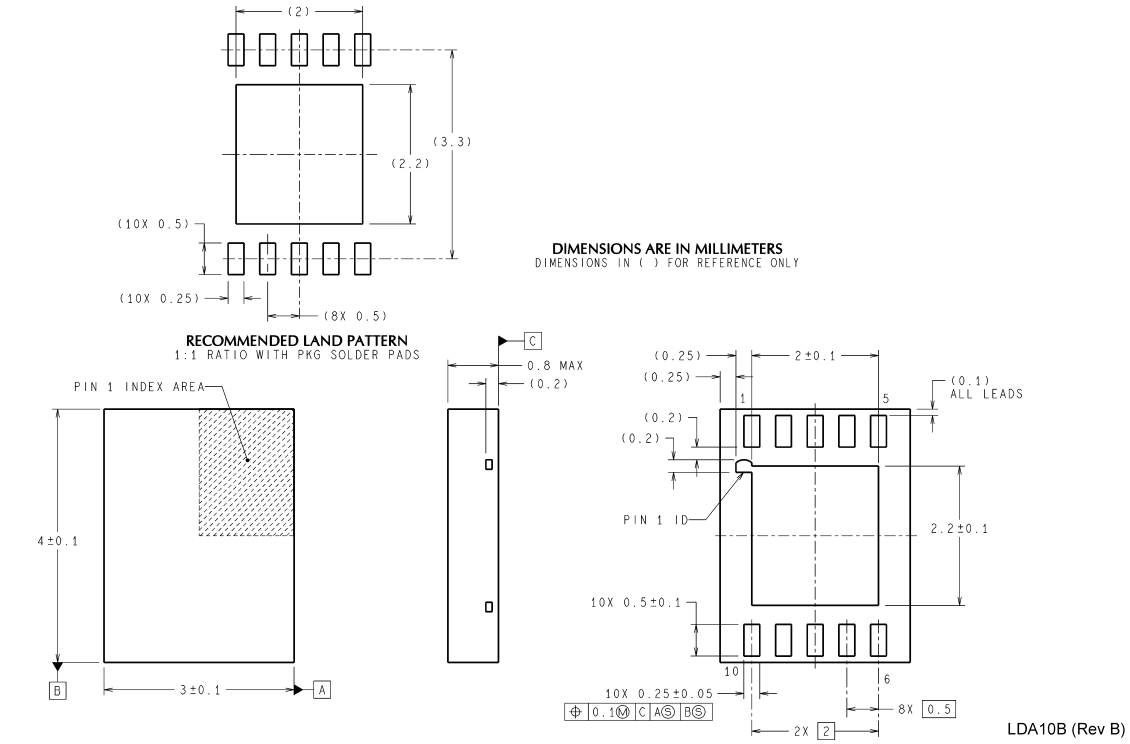
MSOP
Order Number LM4990MM
NS Package Number MUA08A



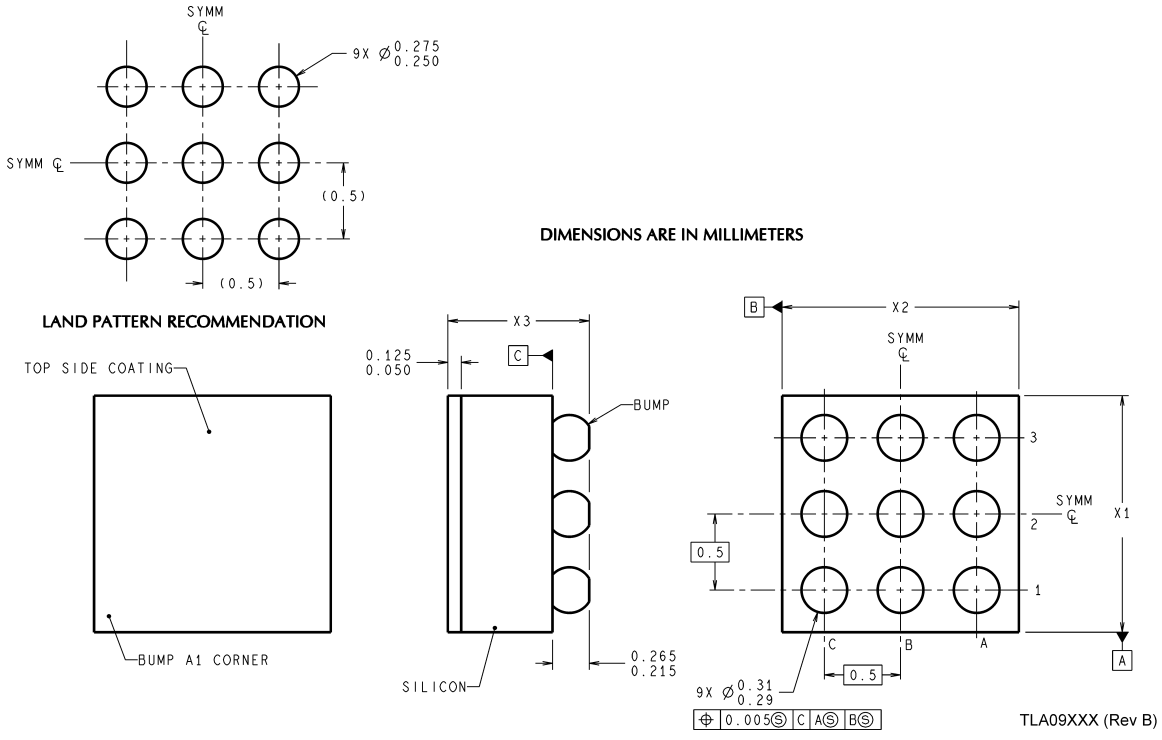
MXF10A (Rev A)

Exposed-DAP TSSOP
Order Number LM4990MH
NS Package Number MXF10A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LLP
Order Number LM4990LD
NS Package Number LDA10B



9–Bump micro SMD
Order Number LM4990ITL, LM4990ITLX
NS Package Number TLA09ZZA
X1 = 1.463±0.03 X2 = 1.463±0.03 X3 = 0.600±0.075

Notes

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