

**PROTECTION PRODUCTS**
**Description**

The SFC2280-68 is a low pass filter array with integrated TVS diodes. It is designed to provide bidirectional filtering of EMI/RFI signals and electrostatic discharge (ESD) protection in portable electronic equipment. This state-of-the-art device utilizes solid-state silicon-avalanche technology for superior clamping performance and DC electrical characteristics. They have been optimized for use on a speaker port in cellular phones and other portable electronics.

The device has very low insertion loss in the pass band (to approximately 10MHz) and high attenuation at frequencies ranging from 800MHz to 3GHz. Each line features two stages of TVS diode protection. The TVS diodes provide effective suppression of ESD voltages in excess of  $\pm 15\text{kV}$  (air discharge) and  $\pm 8\text{kV}$  (contact discharge) per IEC 61000-4-2, level 4. The TVS diodes are bidirectional for supporting bipolar audio signals without distortion.

The SFC2280-68 is a 6-bump, 0.5mm pitch flip chip array with a 3x2 bump grid. It measures 1.5 x 1.0 x 0.65mm. This small outline makes the device especially well suited for portable applications. The flip chip design results in lower inductance for optimized filter and ESD clamping performance.

**Features**

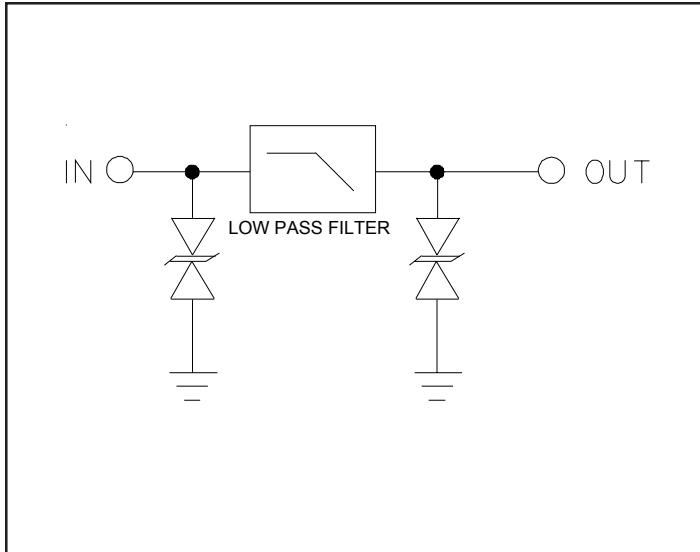
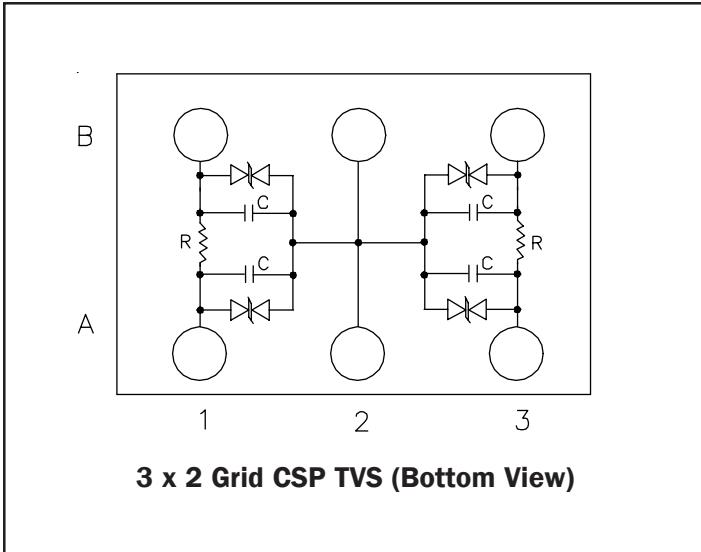
- ◆ Flip Chip bidirectional EMI/RFI filter with integrated ESD protection
- ◆ ESD protection to  
**IEC 61000-4-2 (ESD)  $\pm 15\text{kV}$  (air),  $\pm 8\text{kV}$  (contact)**  
**IEC 61000-4-4 (EFT) 40A (5/50ns)**
- ◆ Filter performance: 20dB attenuation at 800MHz
- ◆ Small chip scale package requires less board space
- ◆ Low profile ( $< 0.65\text{mm}$ )
- ◆ Bidirectional TVS to support negative voltages in audio applications
- ◆ Maximum Dimensions: 1.5 x 1.0 x 0.65 mm
- ◆ TVS Working voltage: 5V
- ◆ Series Resistor:  $68\Omega$
- ◆ Solid-state technology

**Mechanical Characteristics**

- ◆ JEDEC MO-211, 0.50 mm Pitch Flip Chip Package
- ◆ Non-conductive top side coating
- ◆ Marking : Marking Code and orientation mark
- ◆ Packaging : Tape and Reel

**Applications**

- ◆ Cell Phone Handsets and Accessories
- ◆ Personal Digital Assistants (PDA's)
- ◆ Notebook and Hand Held Computers
- ◆ Digital Camcorders
- ◆ MP3 Players

**Circuit Diagram (Each Line)**

**Schematic & PIN Configuration**


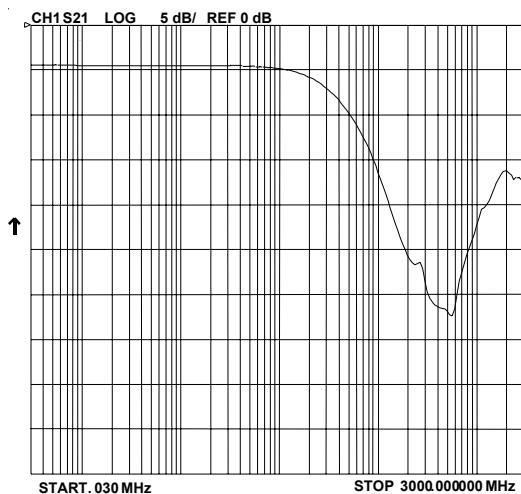
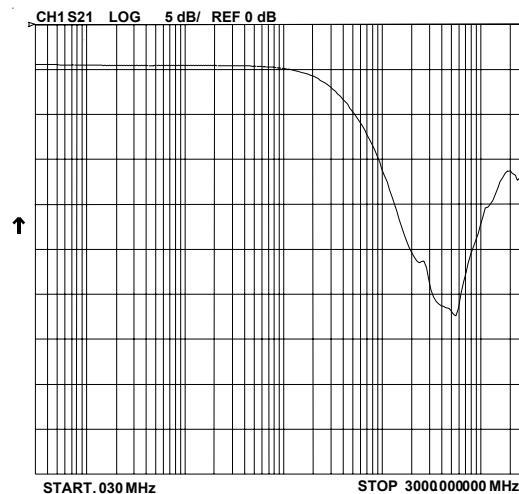
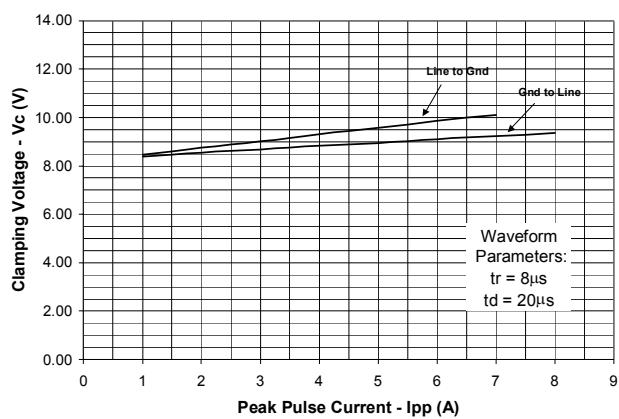
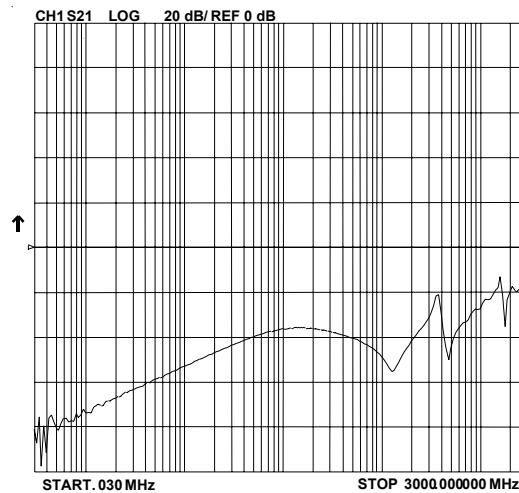
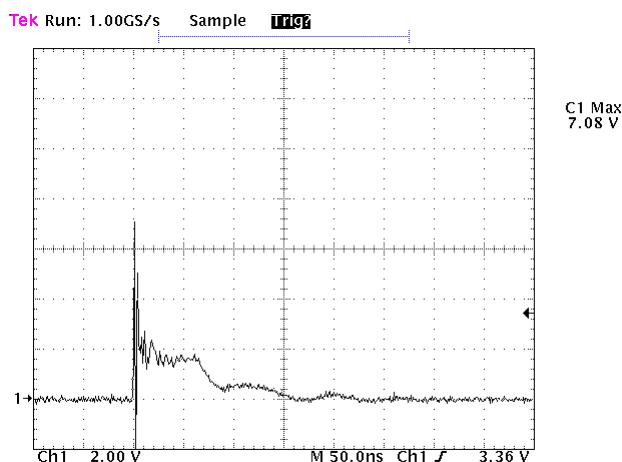
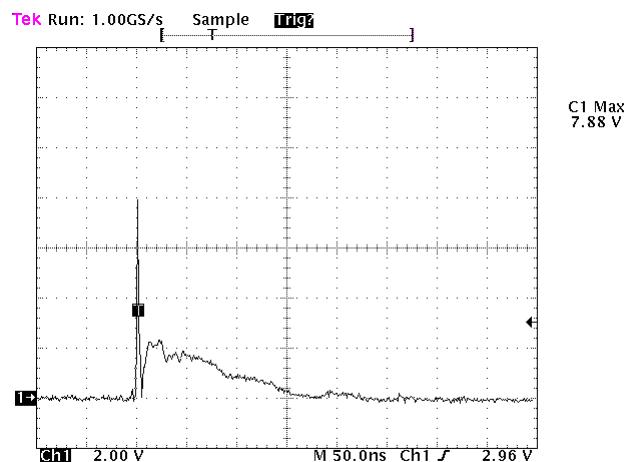
## PROTECTION PRODUCTS

### Absolute Maximum Rating

| Rating   | Symbol    | Value       | Units |
|--|-----------|-------------|-------|
| Steady-State Power   | $P_{ss}$  | 100         | mW    |
| ESD per IEC 61000-4-2 (Air)<br>ESD per IEC 61000-4-2 (Contact) | $V_{ESD}$ | >16<br>>10  | kV    |
| Operating Temperature  | $T_J$     | -55 to +125 | °C    |
| Storage Temperature  | $T_{STG}$ | -55 to +150 | °C    |

### Electrical Characteristics

| SFC2280-68                       |             |  |         |         |         |       |
|----------------------------------|-------------|--|---------|---------|---------|-------|
| Parameter                        | Symbol      | Conditions   | Minimum | Typical | Maximum | Units |
| TVS Reverse Stand-Off Voltage    | $V_{RWM}$   |  |         |         | 5       | V     |
| TVS Reverse Breakdown Voltage    | $V_{BR}$    | $I_t = 1\text{mA}$   | 6       |         |         | V     |
| TVS Reverse Leakage Current      | $I_R$       | $V_{RWM} = 5\text{V}$ , $T=25\text{ }^\circ\text{C}$         |         |         | 5       | µA    |
| Resistor Temperature Coefficient | $T_{COEFF}$ | Each Line  |         |         | 400     | ppm   |
| Series Resistance                | R           | Each Line  | 61      | 68      | 75      | Ω     |
| TVS Capacitance                  | $C_{TVS}$   | Each Individual TVS<br>$V_R = 0\text{V}$ , $f = 1\text{MHz}$ |         | 30      |         | pF    |
| Total Capacitance                | $C_{TOT}$   | Any I/O to Ground<br>$V_R = 0\text{V}$ , $f = 1\text{MHz}$   |         | 160     |         | pF    |

**PROTECTION PRODUCTS**
**Typical Characteristics**
**Typical Insertion loss (A1-B1 to Gnd)**

**Typical Insertion loss (A3-B3 to Gnd)**

**Clamping Voltage vs. Peak Pulse Current**

**Analog Crosstalk (B1 to A3)**

**ESD Clamping (8kV Contact)**

**ESD Clamping (15kV Air)**


## PROTECTION PRODUCTS

### Applications Information

#### Device Connection Options

The SFC2280-68 has solder bumps located in a  $3 \times 2$  matrix layout on the active side of the device. The bumps are designated by the numbers 1 - 3 along the horizontal axis and letters A - B along the vertical axis. The lines to be protected are connected at bumps A1, B1, A3, and B3. Bumps A2 and B2 are connected to ground. All path lengths should be kept as short as possible to minimize the effects of parasitic inductance in the board traces.

#### Flip Chip TVS

Flip chip TVS devices are wafer level chip scale packages. They eliminate external plastic packages and leads and thus result in a significant board space savings. Manufacturing costs are minimized since they do not require an intermediate level interconnect or interposer layer for reliable operation. They are compatible with current pick and place equipment further reducing manufacturing costs. Certain precautions and design considerations have to be observed however for maximum solder joint reliability. These include solder pad definition, board finish and assembly parameters.

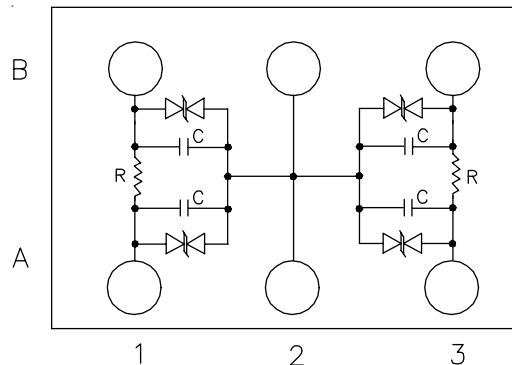
#### Printed Circuit Board Mounting

Non-solder mask defined (NSMD) land patterns are recommended for mounting the SFC2280-68. Solder mask defined (SMD) pads produce stress points near the solder mask on the PCB side that can result in solder joint cracking when exposed to extreme fatigue conditions. The recommended pad size is  $0.225 \pm 0.010$  mm with a solder mask opening of  $0.350 \pm 0.025$  mm.

#### Grid Courtyard

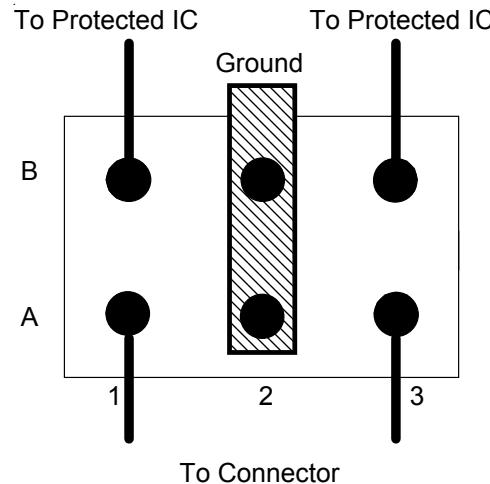
The recommended grid placement courtyard is  $1.3 \times 1.8$  mm. The grid courtyard is intended to encompass the land pattern and the component body that is centered in the land pattern. When placing parts on a PCB, the highest recommended density is when one courtyard touches another.

#### Pin Identification and Configuration (Bottom View)



| Pin | Identification                |
|-----|-------------------------------|
| A1  | Line 1 In (From Microphone)   |
| B1  | Line 1 Out (To Audio Circuit) |
| A3  | Line 2 In (From Microphone)   |
| B3  | Line 2 Out (To Audio Circuit) |
| A2  | Ground                        |
| B2  | Ground                        |

#### Layout Example



## PROTECTION PRODUCTS

### Applications Information (Continued)

#### Printed Circuit Board Finish

A uniform board finish is critical for good assembly yield. Two finishes that provide uniform surface coatings are immersion nickel gold and organic surface protectant (OSP). A non-uniform finish such as hot air solder leveling (HASL) can lead to mounting problems and should be avoided.

#### Stencil Design

A properly designed stencil is key to achieving adequate solder volume without compromising assembly yields. A 0.100mm thick, laser cut, electro-polished stencil with 0.275mm square apertures and rounded corners is recommended.

#### Reflow Profile

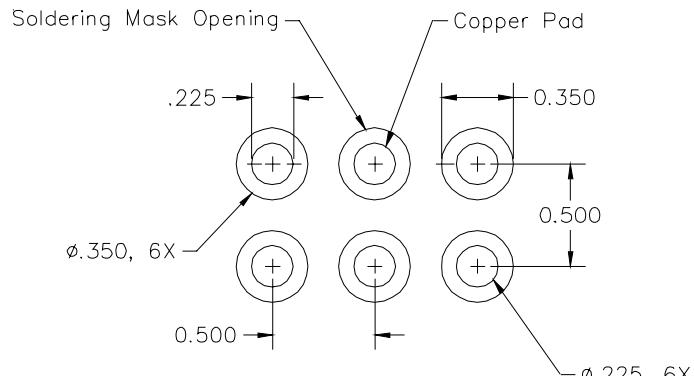
The flip chip TVS can be assembled using the reflow requirements for IPC/JEDEC standard J-STD-020 for assembly of small body components. During reflow, the component will self-align itself on the pad.

#### Assembly Guideline for Pb-Free Soldering

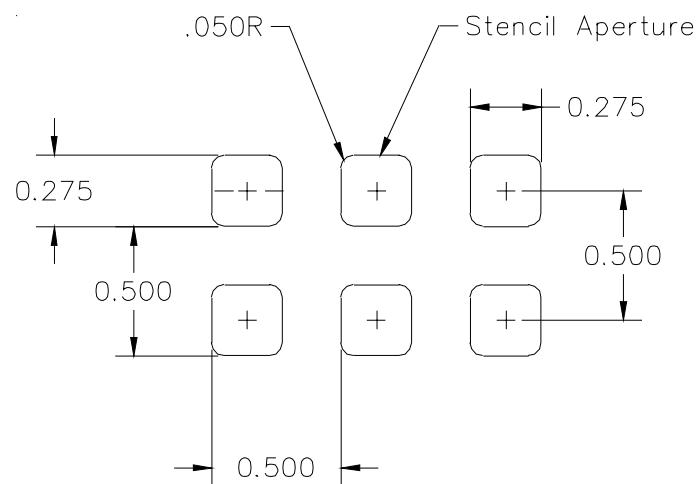
The following are recommendations for the assembly of this device:

| Assembly Parameter       | Recommendation                |
|--------------------------|-------------------------------|
| Solder Ball Composition  | 95.5Sn/3.8Ag/0.7Cu            |
| Solder Stencil Design    | Same as the SnPb design       |
| Solder Stencil Thickness | 0.100 mm (0.004")             |
| Solder Paste Composition | Sn Ag (3-4) Cu (0.5-0.9)      |
| Solder Paste Type        | Type 4 size sphere or smaller |
| Solder Reflow Profile    | per JEDEC J-STD-020           |
| PCB Solder Pad Design    | Same as the SnPb Design       |
| PCB Pad Finish           | OSP or AuNi                   |

#### NSMD Package Footprint



#### Stencil Design



## PROTECTION PRODUCTS

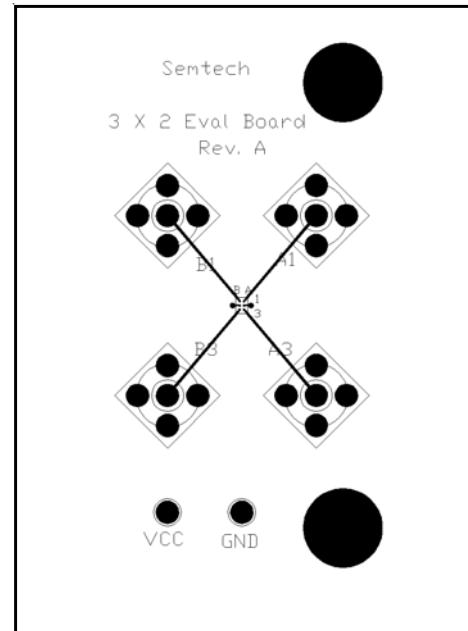
### Applications Information

#### Insertion Loss

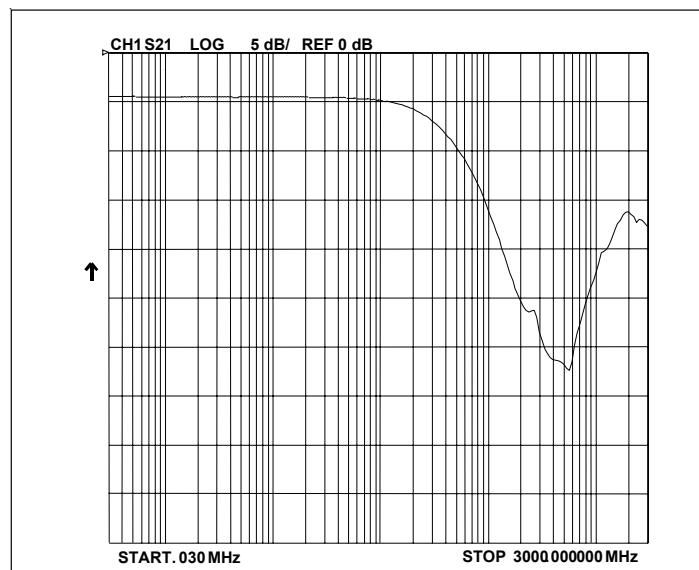
The insertion loss of the device is the ratio of the power delivered to the load with and without the filter in the circuit. This parameter is dependent upon the impedance of the source and the load. The standard impedance of test equipment that is used to measure filter frequency response is  $50\Omega$ . In order to obtain an accurate measurement of the filter performance, an evaluation board with  $50\Omega$  transmission lines is used. The evaluation board for the SFC2280-68 is shown in Figure 1. The board is specifically designed for frequency response analysis. The evaluation board contains SMA connectors at each of the circuits inputs and outputs. The connections are made with  $50\Omega$  traces. An HP 8753E network analyzer with an internal spectrum analyzer and tracking generator is used. This equipment has the capability to sweep the device from 3kHz to 3GHz. The analyzer's source ( $R_s$ ) impedance is equal to the load ( $R_L$ ) impedance which is equal to  $50\Omega$ .

Pins A1, A3, B1, and B3 of the device are connected to SMA connectors via the  $50\Omega$  traces. Pins A1 and A3 are the data line inputs and pins B1 and B3 are the outputs. Pin A2 is connected to the test point marked  $V_{cc}$ . Pin B2 is connected to GND. Since pin A2 and B2 are connected internally within the device, a  $V_{cc}$  connection is not necessary.

A typical insertion loss characteristic is shown in Figure 2. As shown, the device has very low insertion loss in the pass band (to approximately 10MHz) and good attenuation at high frequencies (approximately 100MHz to 3GHz).



**Figure 1 - SFC2280-68 Evaluation Board**



**Figure 2 - Typical Insertion Loss S21**

## PROTECTION PRODUCTS

### Applications Information (Continued)

#### Voltage Clamping Characteristics.

The clamping characteristics of the SFC2280-68 are optimized by the use of two TVS diodes in the protection circuit (Figure 3). An ESD strike on the protected line will be initially suppressed by the first TVS diode. The voltage across the TVS will be the clamping voltage of the device ( $V_{c1}$ ) given by:

$$V_{c1} = V_{br} + R_D * I_{PP}$$

where

$V_{br}$  = Breakdown voltage of the TVS

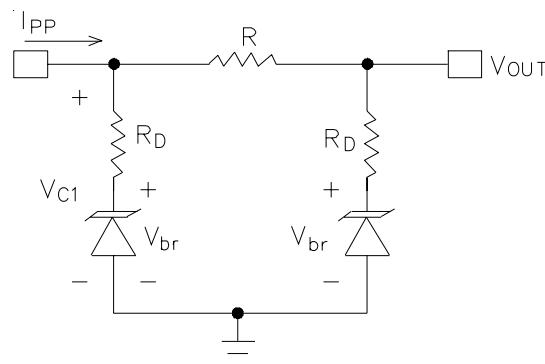
$R_D$  = Dynamic resistance of the TVS

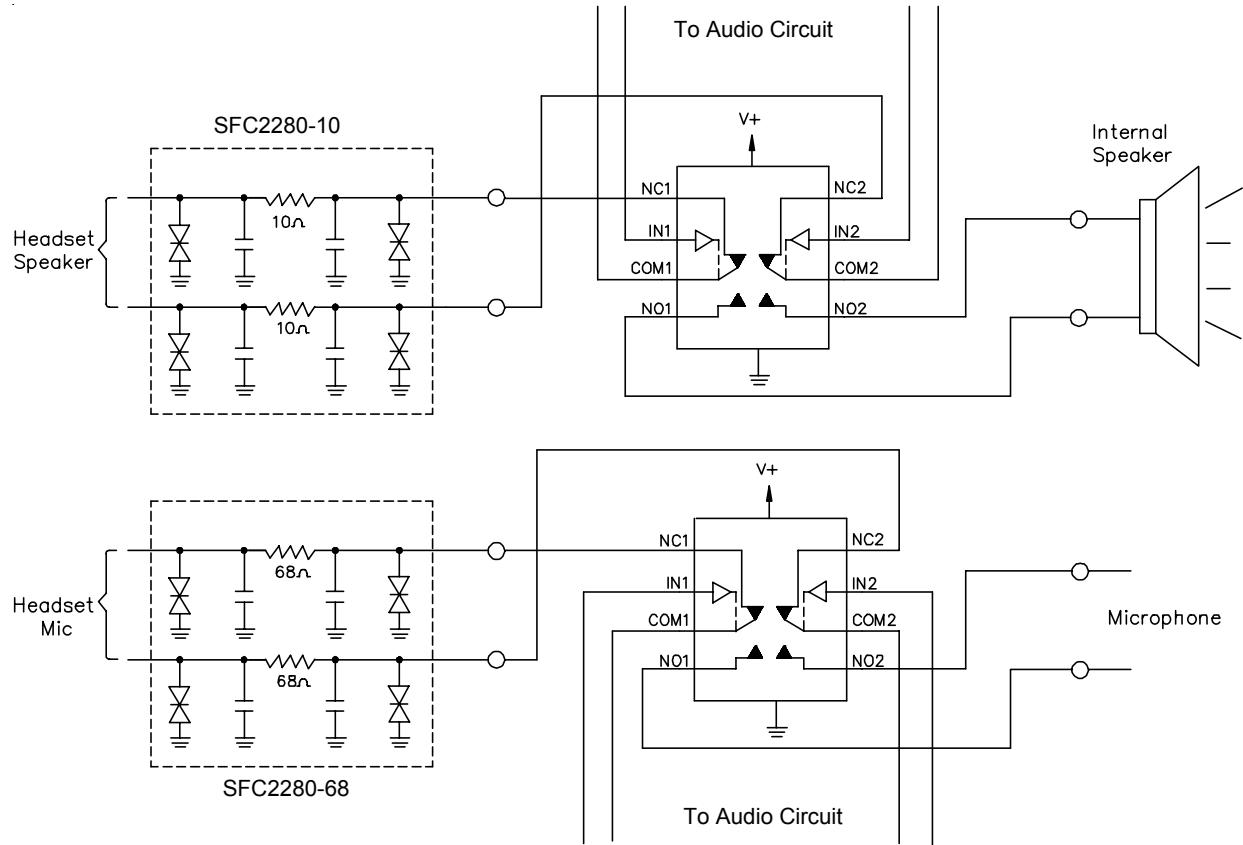
$I_{PP}$  = Peak pulse (ESD) current

The dynamic resistance of the TVS is very small, typically  $< 0.5\Omega$ .

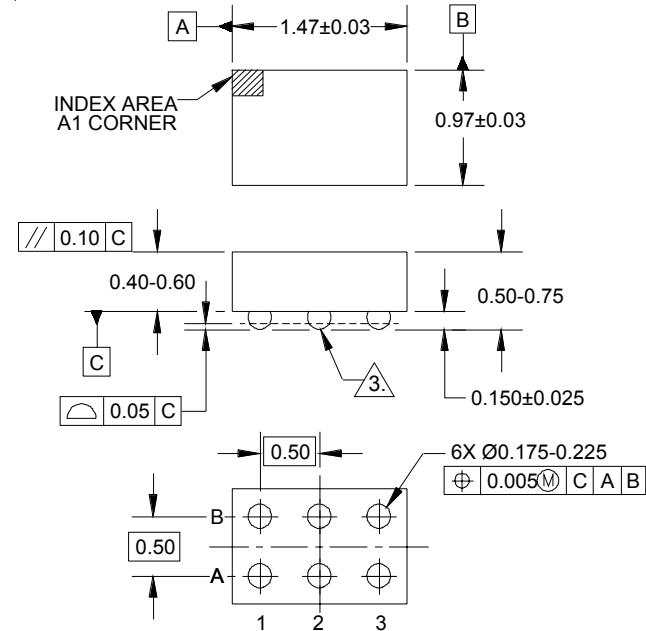
The second TVS will be subjected to  $V_{c1}$  through the voltage divider formed by the series resistor (R) and the dynamic resistance of the TVS. Since  $R \gg R_D$  then by the voltage divider theorem, the voltage seen by the protected IC will be a slightly above the breakdown voltage ( $V_{br}$ ) of the second TVS.

**Figure 3 - Clamping Characteristic Model**



**PROTECTION PRODUCTS**
**Applications Information (Continued)**


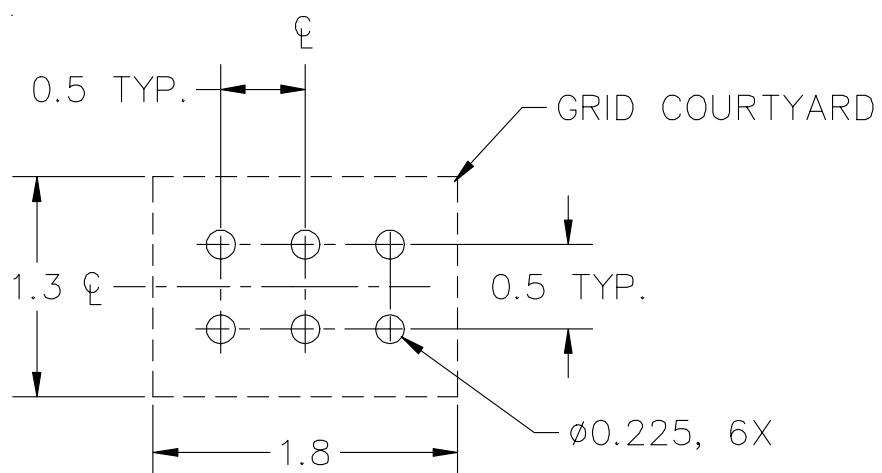
**Figure 4 - Cell Phone Headset Audio Port Protection**

**PROTECTION PRODUCTS**
**Outline Drawing - 3x2 Grid Flip Chip**

**NOTES:**

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS

2. REFERENCE JEDEC REGISTRATION MO-211.

3. Sn63/Pb37 FOR STANDARD DEVICES OR SN95.5/Ag3.8/Cu0.7  
FOR Pb-FREE DEVICES

**Land Pattern - 3x2 Grid Flip Chip**


1. Dimensions in millimeters.

## PROTECTION PRODUCTS

### Marking Codes

| Part Number | Marking Code |
|-------------|--------------|
| SFC2280-68  | 2280         |

**Top Coating:** The top (non-bump side) of the device is a white non-conductive coating. The coating is laser markable and increases mechanical durability. This material is compliant with UL 94V-0 flammability requirements.

### Ordering Information

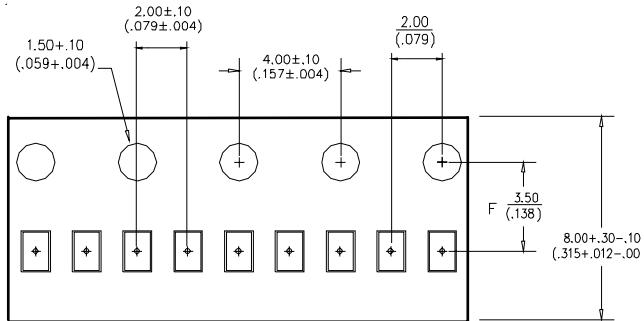
| Part Number                   | Pitch Option | Qty per Reel | Reel Size |
|-------------------------------|--------------|--------------|-----------|
| SFC2280-68.WC                 | 2mm          | 3,000        | 7 Inch    |
| SFC2280-68.WCT <sup>(1)</sup> | 2mm          | 3,000        | 7 Inch    |

#### Notes

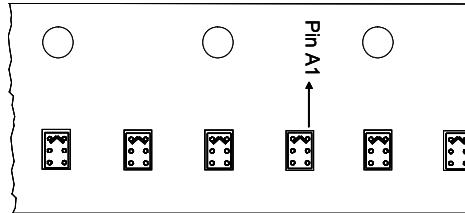
##### (1) Lead Free Solder Balls

ChipClamp is a mark of Semtech Corporation

### Tape and Reel Specification



**Tape Specifications**



**Device Orientation**

### Contact Information

Semtech Corporation  
 Protection Products Division  
 200 Flynn Rd., Camarillo, CA 93012  
 Phone: (805)498-2111 FAX (805)498-3804