



Is Now Part of



ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

74VHC273

Octal D-Type Flip-Flop

Features

- High Speed: $f_{MAX} = 165\text{MHz}$ (typ) at $V_{CC} = 5\text{V}$
- Low power dissipation: $I_{CC} = 4\mu\text{A}$ (max) at $T_A = 25^\circ\text{C}$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min)
- Power down protection is provided on all inputs
- Low noise: $V_{OLP} = 0.9\text{V}$ (max)
- Pin and function compatible with 74HC273
- Leadless DQFN Package

General Description

The VHC273 is an advanced high speed CMOS Octal D-type flip-flop fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The register has a common buffered Clock (CP) which is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The Master Reset (MR) input will clear all flip-flops simultaneously. All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the MR input.

An input protection circuit insures that 0V to 7V can be applied to the inputs pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

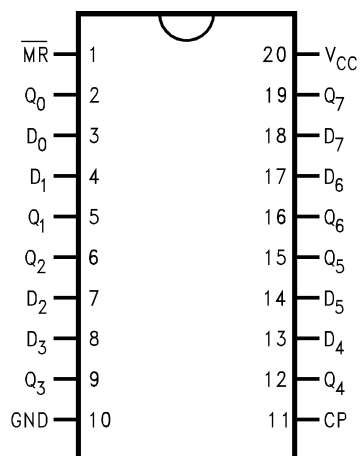
Ordering Information

Order Number	Package Number	Package Description
74VHC273M	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74VHC273SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC273BQ (Preliminary)	MLP020B (Preliminary)	20-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 4.5mm
74VHC273MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

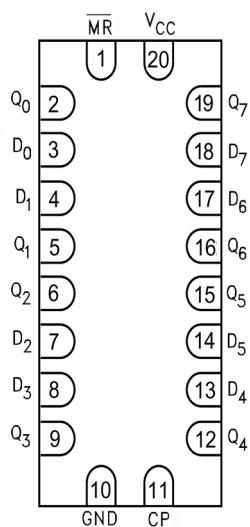
Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering number. Pb-Free package per JEDEC J-STD-020B.

Connection Diagrams

Pin Assignments for
PDIP, SOIC, SOP, and TSSOP



Pad Assignments for DQFN

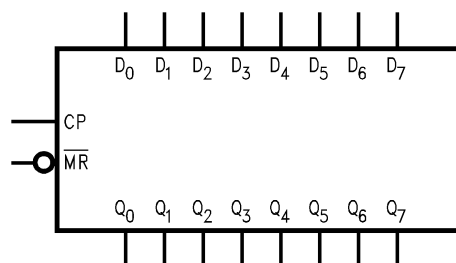


(Top Through View)

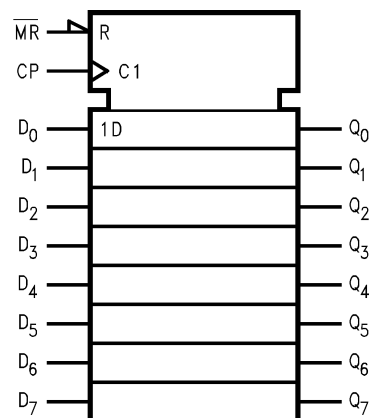
Pin Descriptions

Pin Names	Description
D ₀ –D ₇	Data Inputs
MR	Master Reset
CP	Clock Pulse Input
Q ₀ –Q ₇	Data Outputs

Logic Symbols



IEEE/IEC



Function Table

Operating Mode	Inputs			Outputs
	MR	CP	D _n	Q _n
Reset (Clear)	L	X	X	L
Load '1'	H	↗	H	H
Load '0'	H	↗	L	L

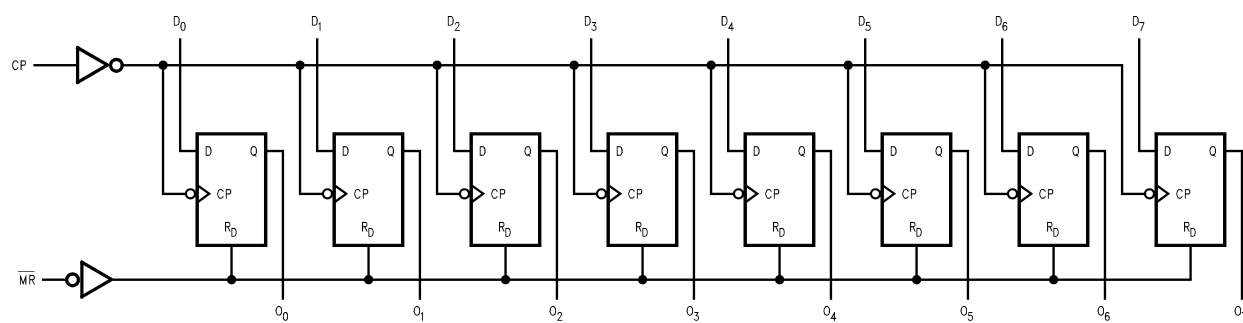
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

↗ = LOW-to-HIGH Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 1.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	−0.5V to +7.0V
V_{IN}	DC Input Voltage	−0.5V to +7.0V
V_{OUT}	DC Output Voltage	−0.5V to $V_{CC} + 0.5V$
I_{IK}	Input Diode Current	−20mA
I_{OK}	Output Diode Current	±20mA
I_{OUT}	DC Output Current	±25mA
I_{CC}	DC V_{CC} /GND Current	±75mA
T_{STG}	Storage Temperature	−65°C to +150°C
T_L	Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions⁽¹⁾

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	2.0V to +5.5V
V_{IN}	Input Voltage	0V to +5.5V
V_{OUT}	Output Voltage	0V to V_{CC}
T_{OPR}	Operating Temperature	−40°C to +85°C
t_r, t_f	Input Rise and Fall Time, $V_{CC} = 3.3V \pm 0.3V$ $V_{CC} = 5.0V \pm 0.5V$	0ns/V ~ 100ns/V 0ns/V ~ 20ns/V

Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	Conditions		T _A =					Units		
					25°C			–40°C to +85°C				
					Min.	Typ.	Max.	Min.	Max.			
V _{IH}	HIGH Level Input Voltage	2.0			1.50			1.50		V		
		3.0–5.5			0.7 x V _{CC}			0.7 x V _{CC}				
V _{IL}	LOW Level Input Voltage	2.0					0.50		0.50	V		
		3.0–5.5					0.3 x V _{CC}		0.3 x V _{CC}			
V _{OH}	HIGH Level Output Voltage	2.0	V _{IN} = V _{IH} or V _{IL}	I _{OH} = –50μA	1.9	2.0		1.9		V		
		3.0			2.9	3.0		2.9				
		4.5			4.4	4.5		4.4				
		3.0				I _{OH} = –4mA	2.58				2.48	
		4.5				I _{OH} = –8mA	3.94				3.80	
V _{OL}	LOW Level Output Voltage	2.0	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50μA		0.0	0.1		0.1	V		
		3.0				0.0	0.1		0.1			
		4.5				0.0	0.1		0.1			
		3.0				I _{OL} = 4mA			0.36			0.44
		4.5				I _{OL} = 8mA			0.36			0.44
I _{IN}	Input Leakage Current	0–5.5	V _{IN} = 5.5V or GND				±0.1		±1.0	μA		
I _{CC}	Quiescent Supply Current	5.5	V _{IN} = V _{CC} or GND				4.0		40.0	μA		

Noise Characteristics

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = 25°C		Units
				Typ.	Limits	
V _{OLP} ⁽²⁾	Quiet Output Maximum Dynamic V _{OL}	5.0	C _L = 50pF	0.6	0.9	V
V _{OLV} ⁽²⁾	Quiet Output Minimum Dynamic V _{OL}	5.0	C _L = 50pF	–0.6	–0.9	V
V _{IHD} ⁽²⁾	Minimum HIGH Level Dynamic Input Voltage	5.0	C _L = 50pF		3.5	V
V _{ILD} ⁽²⁾	Maximum LOW Level Dynamic Input Voltage	5.0	C _L = 50pF		1.5	V

Note:

2. Parameter guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = 25°C			T _A = -40°C to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
f _{MAX}	Maximum Clock Frequency	3.3 ± 0.3	C _L = 15pF	75	120		65		MHz
			C _L = 50pF	50	75		45		
		5.0 ± 0.5	C _L = 15pF	120	165		100		MHz
			C _L = 50pF	80	110		70		
t _{PLH} , t _{PHL}	Propagation Delay Time (CK – Q)	3.3 ± 0.3	C _L = 15pF		8.7	13.6	1.0	16.0	ns
			C _L = 50pF		11.2	17.1	1.0	19.5	
		5.0 ± 0.5	C _L = 15pF		5.8	9.0	1.0	10.5	ns
			C _L = 50pF		7.3	11.0	1.0	12.5	
t _{PHL}	Propagation Delay Time (MR – Q)	3.3 ± 0.3	C _L = 15pF		8.9	13.6	1.0	16.0	ns
			C _L = 50pF		11.4	17.1	1.0	19.5	
		5.0 ± 0.5	C _L = 15pF		5.2	8.5	1.0	10.0	ns
			C _L = 50pF		6.7	10.5	1.0	12.0	
t _{OSLH} , t _{OSHL}	Output to Output Skew	3.3 ± 0.3	(3) C _L = 50pF			1.5		1.5	ns
		5.0 ± 0.5	C _L = 50pF			1.0		1.0	
C _{IN}	Input Capacitance		V _{CC} = Open		4.0	10.0		10.0	pF
C _{PD}	Power Dissipation Capacitance		(4)		31				pF

Notes:

3. Parameter guaranteed by design $t_{OSLH} = |t_{PLHmax} - t_{PLHmin}|$; $t_{OSHL} = |t_{PHLmax} - t_{PHLmin}|$.
4. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained from the equation:
 $I_{CC} (opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8$ (per F/F). The total C_{PD} when n pieces of the Flip-Flop operates can be calculated by the equation: C_{PD} (total) = 22 + 9n.

AC Operating Requirements

Symbol	Parameter	V _{CC} (V) ⁽⁵⁾	T _A = 25°C		T _A = −40°C to +85°C		Units
			Typ.	Guaranteed Minimum			
t _W (L), t _W (H)	Minimum Pulse Width (CK)	3.3		5.5	6.5		ns
		5.0		5.0	5.0		
t _W (L)	Minimum Pulse Width ($\overline{MR}$)	3.3		5.0	6.0		ns
		5.0		5.0	5.0		
t _S	Minimum Setup Time	3.3		5.5	6.5		ns
		5.0		4.5	4.5		
t _H	Minimum Hold Time	3.3		1.0	1.0		ns
		5.0		1.0	1.0		
t _{REC}	Minimum Removal Time ($\overline{MR}$)	3.3		2.5	2.5		ns
		5.0		2.0	2.0		

Note:

5. V_{CC} is 3.3 ± 0.3V or 5.0 ± 0.5V

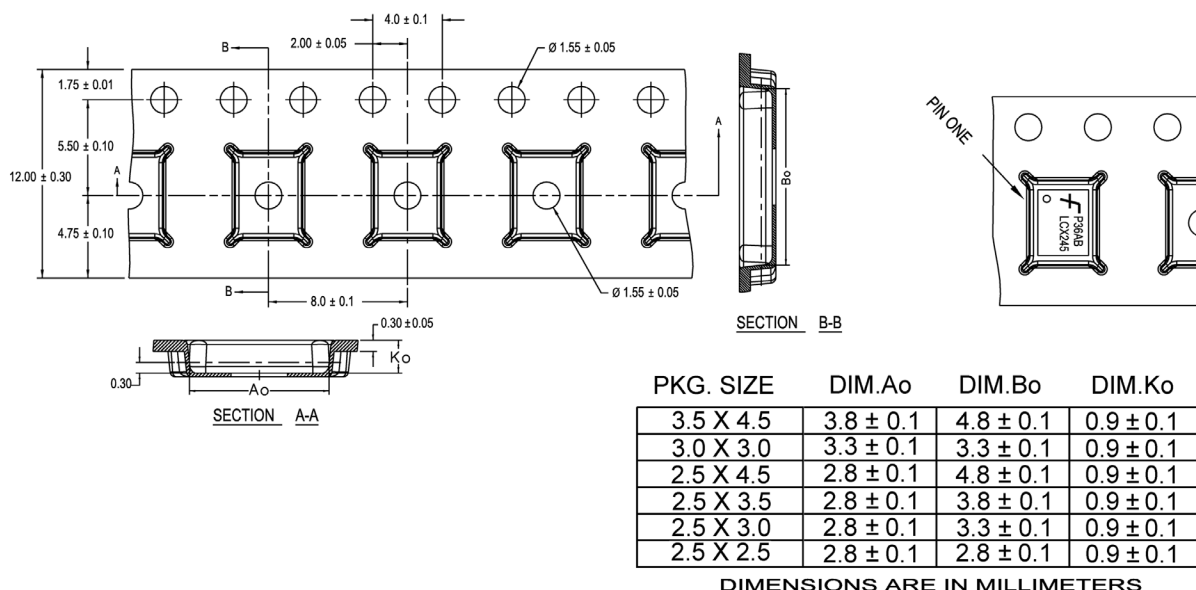
Tape and Reel Specification

Tape Format for DQFN

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
BQ	Leader (Start End)	125 (typ.)	Empty	Sealed
	Carrier	2500/3000	Filled	Sealed
	Trailer (Hub End)	75 (typ.)	Empty	Sealed

Tape Dimensions

Dimensions are in millimeters unless otherwise noted.



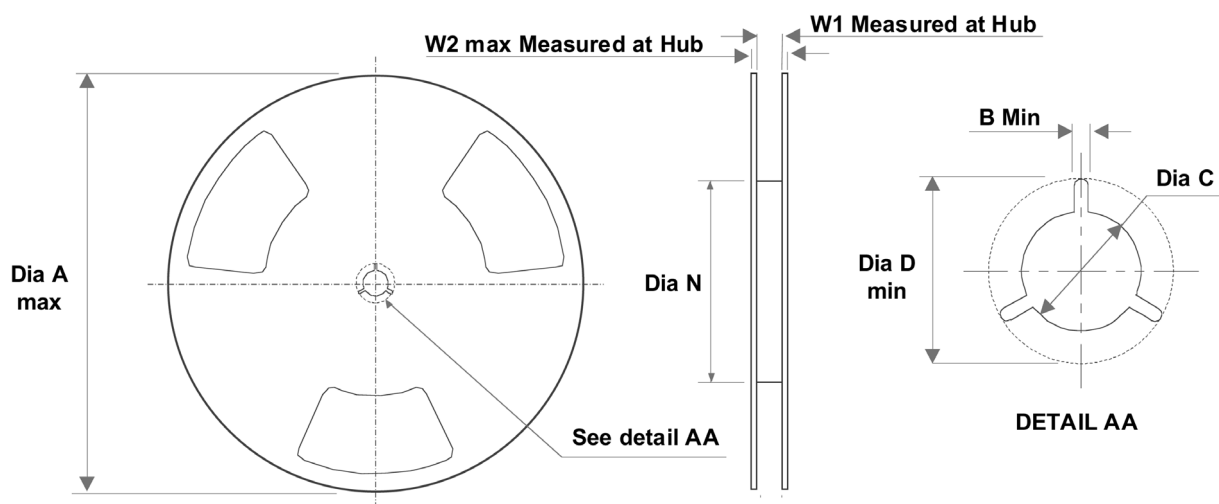
NOTES: unless otherwise specified

1. Cumulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is $\pm 0.002[0.05]$ for these dimensions on all 12mm tapes.
5. Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Dimension in inches rounded.

Figure 2.

Tape and Reel Specification (Continued)**Reel Dimensions for DQFN**

Dimensions are in inches (millimeters) unless otherwise noted.



Tape Size	A	B	C	D	N	W1	W2
12mm	13.0 (330)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	7.008 (178)	0.488 (12.4)	0.724 (18.4)

Figure 3.

Physical Dimensions

Dimensions are in inches (millimeters) unless otherwise noted.

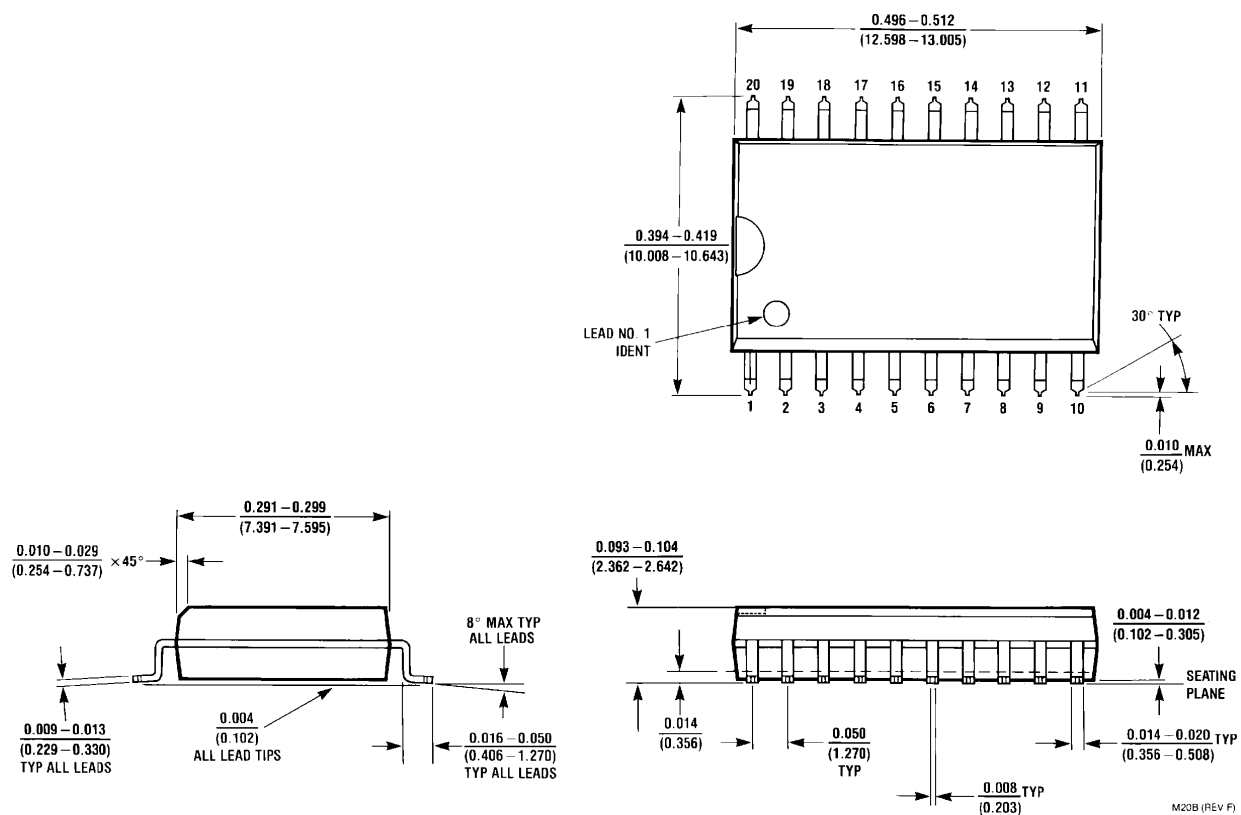
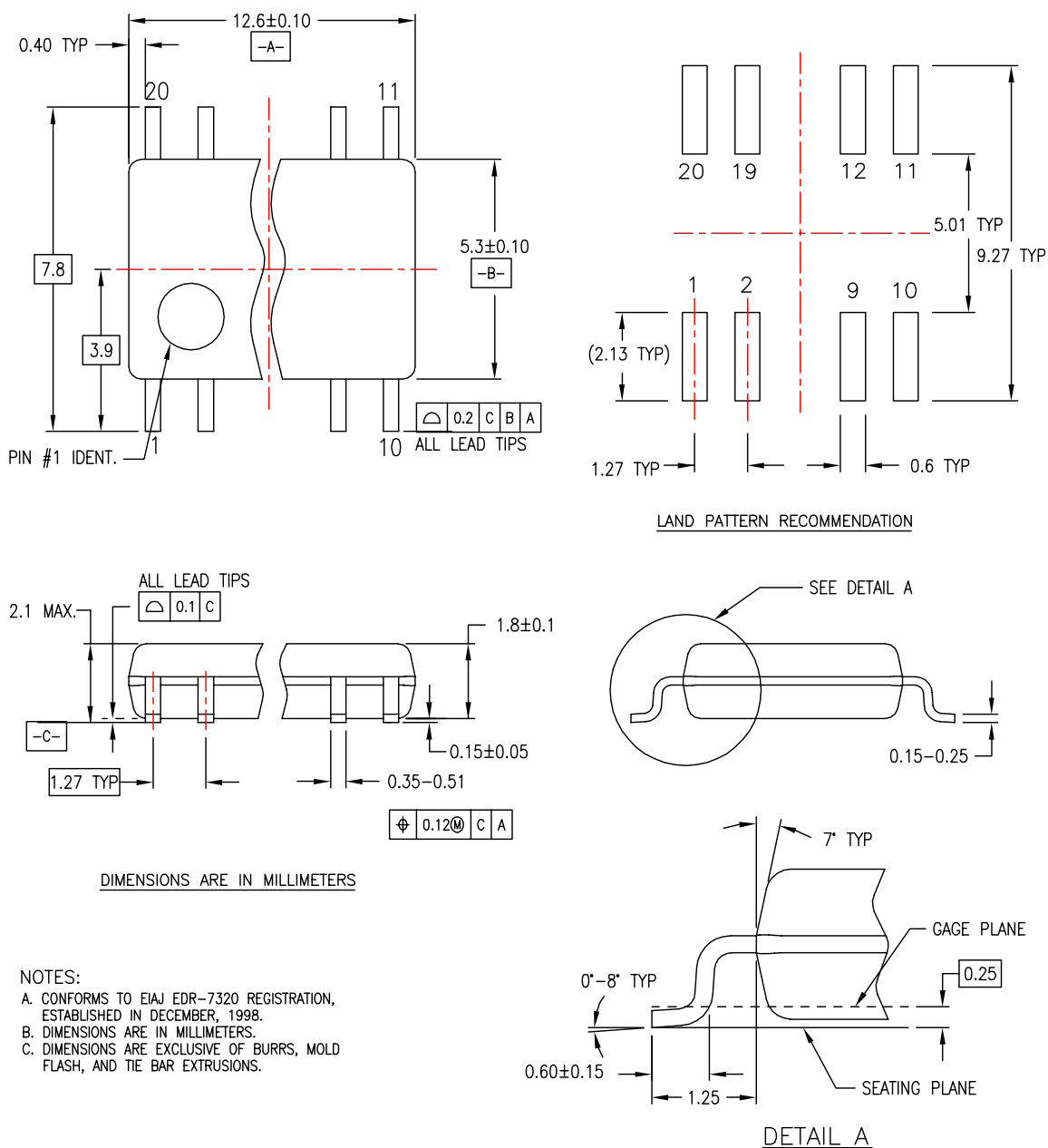


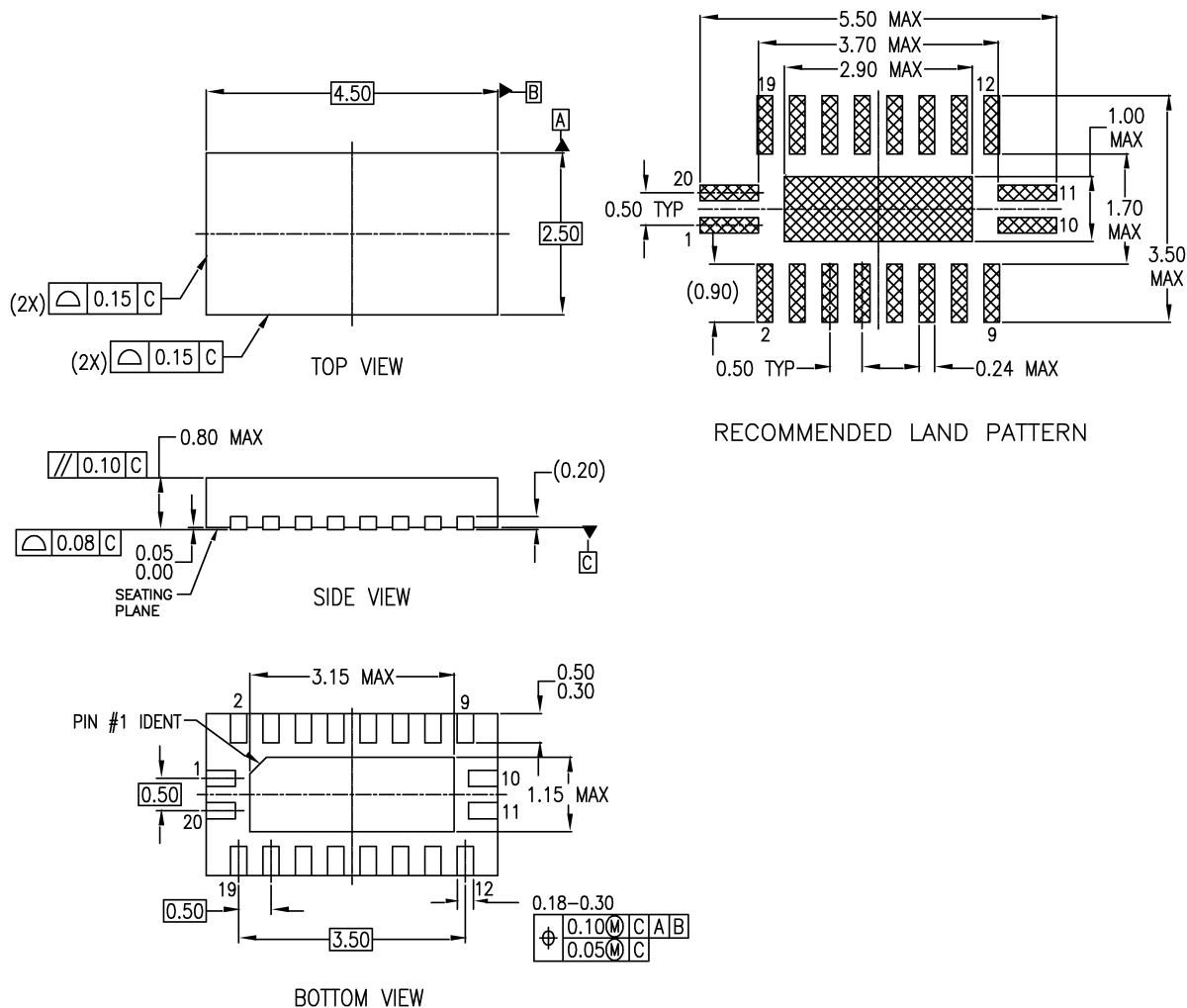
Figure 4. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Dimensions are in millimeters unless otherwise noted.



Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.

**NOTES:**

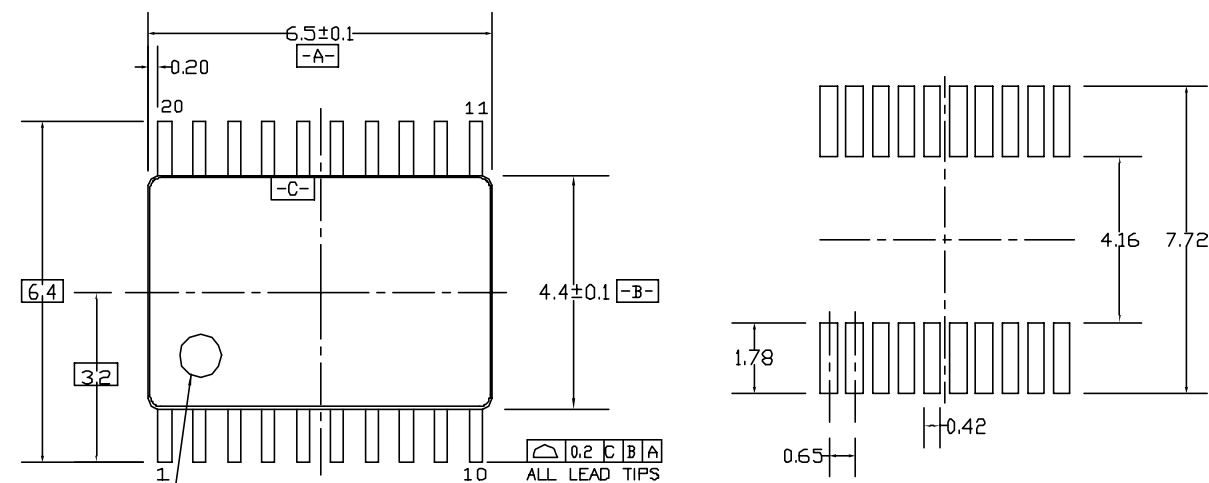
- A. CONFORMS TO JEDEC REGISTRATION MO-241, VARIATION AC
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP020BrevA

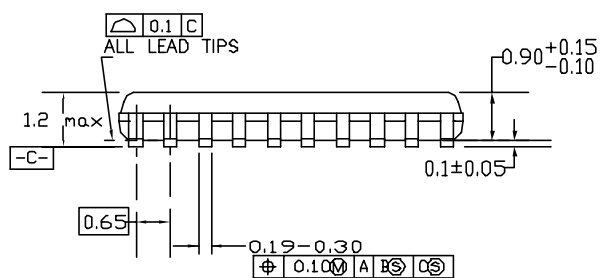
Figure 6. 20-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 4.5mm Package Number MLP020B (Preliminary)

Physical Dimensions (Continued)

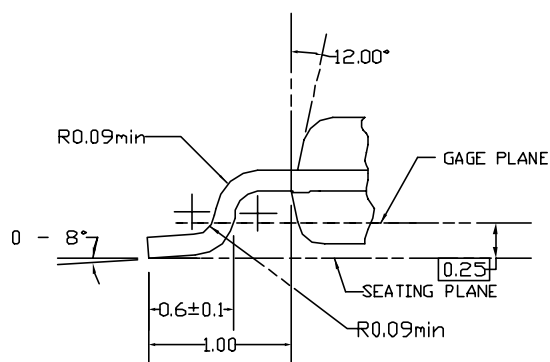
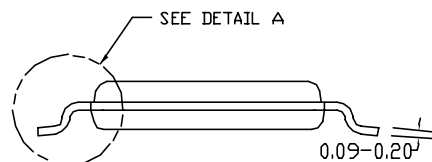
Dimensions are in millimeters unless otherwise noted.



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REV D1

**Figure 7. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20**

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACE ^x	HiSeC TM	Programmable Active Droop TM	TinyLogic [®]
Across the board. Around the world. TM	<i>i-Lo</i> TM	QFET [®]	TINYOPTO TM
ActiveArray TM	ImpliedDisconnect TM	QS TM	TinyPower TM
Bottomless TM	IntelliMAX TM	QT Optoelectronics TM	TinyWire TM
Build it Now TM	ISOPLANAR TM	Quiet Series TM	TruTranslation TM
CoolFET TM	MICROCOUPLER TM	RapidConfigure TM	μSerDes TM
CROSSVOLT TM	MicroPak TM	RapidConnect TM	UHC [®]
CTL TM	MICROWIRE TM	ScalarPump TM	UniFET TM
Current Transfer Logic TM	MSX TM	SMART START TM	VCX TM
DO TM	MSXPro TM	SPM [®]	Wire TM
E ² CMOS TM	OCX TM	STEALTH TM	
EcoSPARK [®]	OCXPro TM	SuperFET TM	
EnSigna TM	OPTOLOGIC [®]	SuperSOT TM -3	
FACT Quiet Series TM	OPTOPLANAR [®]	SuperSOT TM -6	
FACT [®]	PACMAN TM	SuperSOT TM -8	
FAST [®]	POP TM	SyncFET TM	
FASTr TM	Power220 [®]	TCM TM	
FPS TM	Power247 [®]	The Power Franchise [®]	
FRFET [®]	PowerEdge TM	 TM	
GlobalOptoisolator TM	PowerSaver TM	TinyBoost TM	
GTO TM	PowerTrench [®]	TinyBuck TM	

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. 124

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local
Sales Representative