BGS13GA14

SP3T Diversity Antenna Switch with GPIO Interface

Data Sheet

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Revision History

Document No.: BGS13GA14__v3.1.pdf	
Revision History: Rev. v3.1	
Previous Version: 3.0	
Page	**Subjects (major changes since last revision)**
7	Ambient temperature range updated in Table 4
8	Ambient temperature range updated in Table 6

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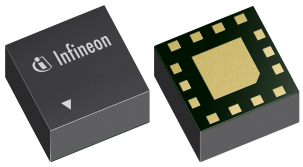
BGS13GA14

1 Features



- 3 high-linearity, interchangeable RX ports
- Low insertion loss
- Low harmonic generation
- High port-to-port-isolation
- Suitable for Edge / C2K / LTE / WCDMA Applications
- LTE TX Power handling capabilities
- 0.1 to 6.0 GHz coverage
- No decoupling capacitors required if no DC applied on RF lines
- On chip control logic including ESD protection
- General Purpose Input-Output (GPIO) Interface
- Small form factor 2.0 mm x 2.0 mm
- No power supply blocking required
- High EMI robustness
- RoHS and WEEE compliant package

2 Product Description

The BGS13GA14 is a Single Pole Three Throw (SP3T) Diversity Switch optimized for wireless applications up to 6.0 GHz. It is part of SP3T-SP8T diversity switch family designed to meet the requirements of chipset reference designs. The module comes in a miniature ATSLP package and comprises of a CMOS SP3T switch with integrated GPIO interface. This RF switch is a perfect solution for multimode handsets based on LTE and WCDMA. The switch device configuration is shown in Fig. 1.
The switch is controlled via a GPIO interface. It features DC-free RF ports and unlike GaAs technology, external DC blocking capacitors at the RF ports are only required if DC voltage is applied externally.

Table 1: Ordering Information

Type	Package	Marking
BGS13GA14	ATSLP-14	G3

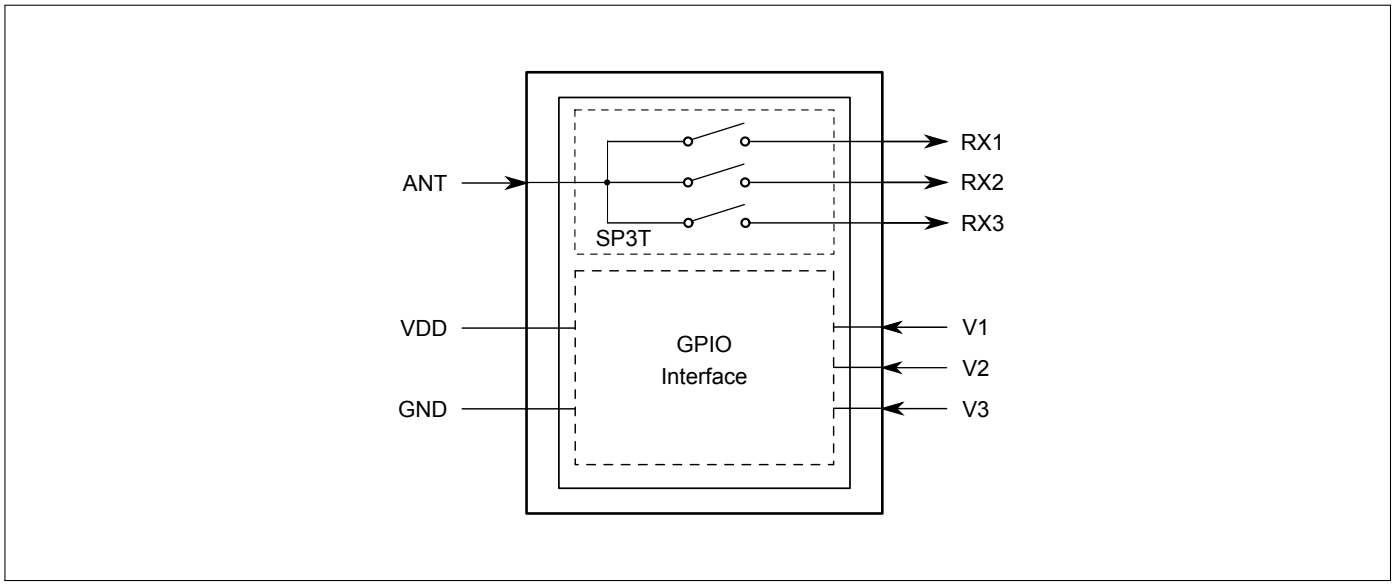


Figure 1: BGS13GA14 block diagram

3 Maximum Ratings

Table 2: Maximum Ratings, Table I at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency Range	f	0.1	–	–	GHz	1)
Supply voltage	V_{dd}	-0.5	–	3.6	V	–
Storage temperature range	T_{STG}	-55	–	150	°C	–
Junction temperature	T_j	–	–	125	°C	–
RF input power at all Rx ports	P_{RF_Rx}	–	–	32	dBm	CW
ESD capability, CDM 2)	$V_{ESD_{CDM}}$	−500	–	+500	V	All pins
ESD capability, HBM 3)	$V_{ESD_{HBM}}$	−1	–	+1	kV	Digital, digital versus RF
		−1	–	+1	V	RF
ESD capability, system level 4)	$V_{ESD_{ANT}}$	−8	–	+8	kV	ANT versus system GND, with 27 nH shunt inductor

1) There is also a DC connection between switched paths. The DC voltage at RF ports V_{RFDC} has to be 0V.
2) Field-Induced Charged-Device Model JESD22-C101. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.
3) Human Body Model ANSI/ESDA/JEDEC JS-001-2012 (R = 1.5 kΩ, C = 100 pF).
4) IEC 61000-4-2 (R = 330 Ω, C = 150 pF), contact discharge.

Table 3: Maximum Ratings, Table II at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance junction - soldering point	R_{thJS}	–	60	–	K/W	–
Maximum DC-voltage on RF-Ports and RF-Ground	V_{RFDC}	0	–	0	V	No DC voltages allowed on RF-Ports
GPIO control voltage levels	V_{Ctrlx}	-0.7	–	V_{dd}+0.7	V	–

4 Operation Ranges

Table 4: Operation Ranges

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{dd}	2.4	3.0	3.4	V	–
Supply current	I_{dd}	–	75	200	µA	–
GPIO control voltage high	V_{Ctrl_H}	1.35	–	V_{dd}	V	–
GPIO control voltage low	V_{Ctrl_L}	0	–	0.45	V	–
GPIO control input capacitance	C_{Ctrl}	–	–	2	pF	–
Ambient temperature	T_A	-40	25	85	°C	–

Table 5: RF Input Power

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rx ports (50 Ω)	P_{RF_Rx}	–	–	28	dBm	–

5 RF Characteristics

Table 6: RF Characteristics at T_A = −40 °C...85 °C, P_{IN} = 0 dBm, Supply Voltage V_{DD}= 2.4 V...3.4 V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion Loss[1]						
All Rx Ports	IL	–	0.30	0.45	dB	698–960 MHz
		–	0.40	0.55	dB	1428–1990 MHz
		–	0.40	0.55	dB	1920–2170 MHz
		–	0.45	0.60	dB	2170–2690 MHz
		–	0.55	0.70	dB	3400–3600 MHz
		–	0.55	0.70	dB	3600–3800 MHz
		–	0.65	0.75	dB	5000–6000 MHz
Return Loss[1]						
All Rx Ports	RL	19	22	–	dB	698–960 MHz
		17	20	–	dB	1428–1990 MHz
		16	19	–	dB	1920–2170 MHz
		15	18	–	dB	2170–2690 MHz
		14	16	–	dB	3400–3600 MHz
		13	15	–	dB	3600–3800 MHz
		13	15	–	dB	5000–6000 MHz
Isolation[1]						
All Rx Ports	ISO	32	45	–	dB	698–960 MHz
		25	42	–	dB	1428–1990 MHz
		24	40	–	dB	1920–2170 MHz
		23	38	–	dB	2170–2690 MHz
		20	35	–	dB	3400–3600 MHz
		19	33	–	dB	3600–3800 MHz
		18	27	–	dB	5000–6000 MHz
Harmonic Generation (UMTS Band 1, Band 5)[1]						
2^{nd} harmonic generation	P_{H2}	90	100	–	dBc	25 dBm, 50 Ω, CW mode
3^{rd} harmonic generation	P_{H3}	80	90	–	dBc	25 dBm, 50 Ω, CW mode
Intermodulation Distortion (UMTS Band 1, Band 5)[1]						
2^{nd} order intermodulation	IMD2 low	–	-105	-100	dBm	IMT, US Cell (see Tab. 8)
3^{rd} order intermodulation	IMD3	–	-110	-105	dBm	IMT, US Cell (see Tab. 9)
2^{nd} order intermodulation	IMD2 high	–	-115	-110	dBm	IMT, US Cell (see Tab. 8)

[1] On application board without any matching components.

Table 7: Switching Time at T_A = 25 °C, P_{IN} = 0 dBm, Supply Voltage V_{DD}= 2.4 V–3.4 V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switching Time						
RF Rise Time	t_{RT}	–	–	2	µs	10 % to 90 % RF signal
Switching Time	t_{ST}	–	2	4	µs	50 % Ctrl signal to 90 % RF signal
Power Up Settling Time	t_{Pup}	–	10	25	µs	After power down mode

Table 8: IMD2 Testcases

Band	CW tone 1 (MHz)	CW tone 1 (dBm)	CW tone 2 (MHz)	CW tone 2 (dBm)
IMT	1950	20	190 (IMD2 low)	-15
			4090 (IMD2 high)	
US Cell	835	20	45 (IMD2 low)	-15
			1715 (IMD2 high)	

Table 9: IMD3 Testcases

Band	CW tone 1 (MHz)	CW tone 1 (dBm)	CW tone 2 (MHz)	CW tone 2 (dBm)
IMT	1950	20	1760	-15
US Cell	835	20	790	-15

6 GPIO Specification

Table 10: Modes of Operation (Truth Table)

		Control Inputs		
State	Mode	V1	V2	V3
1	RX1-ANT	0	0	0
2	RX2-ANT	0	0	1
3	RX3-ANT	0	1	0
4	Isolation	0	1	1
5	Isolation	1	0	0
6	50Ω	1	0	1
7	Isolation	1	1	0
8	Shutdown	1	1	1

7 Package related information

The switch has a package size of 2000 µm in x-dimension and 2000 µm in y-dimension with a maximum deviation of ±50 µm in each dimension. Fig. 2 shows the footprint from top view. The definition of each pin can be found in Tab. 12. In addition a recommendation for the land pattern is displayed in Fig. 4 followed by information regarding laser marking (see Fig. 5).

Table 11: Mechanical Data

Parameter	Symbol	Value	Unit
Package X-Dimension	X	2000 ± 50	µm
Package Y-Dimension	Y	2000 ± 50	µm
Package Height	H	0.65 max	µm

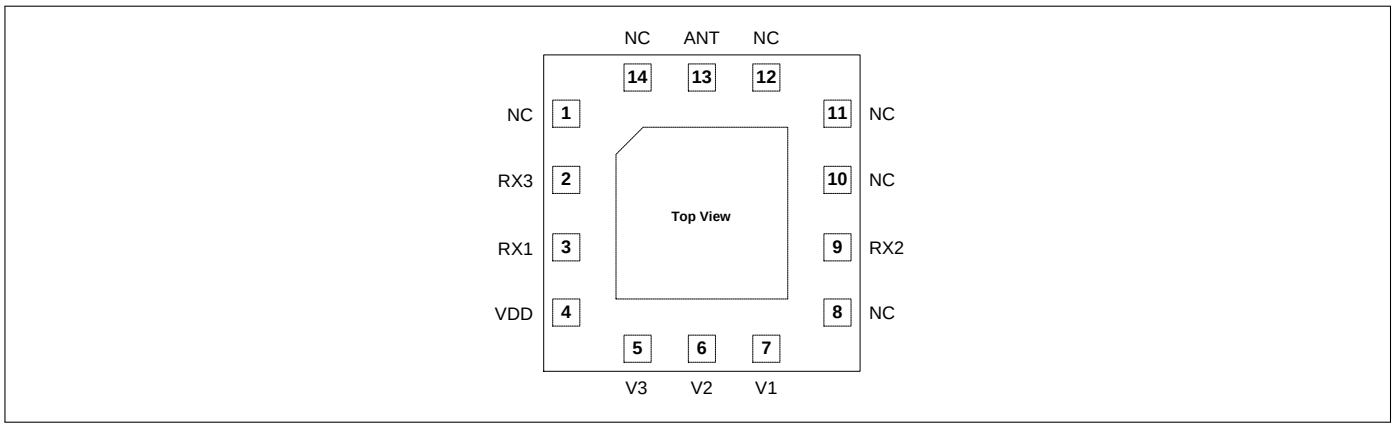


Figure 2: Footprint, top view

Table 12: Pin Definition

No.	Name	Pin Type	Function
0	GND	GND	RF ground; die pad
1	NC		Not connected
2	RX3	I/O	RX port 3
3	RX1	I/O	RX port 1
4	VDD	PWR	V_{DD} supply
5	V3	I	GPIO control pin
6	V2	I	GPIO control pin
7	V1	I	GPIO control pin
8	NC		Not connected
9	RX2	I/O	RX port 2
10	NC		Not connected
11	NC		Not connected
12	NC		Not connected
13	ANT	I/O	Antenna port
14	NC		Not connected

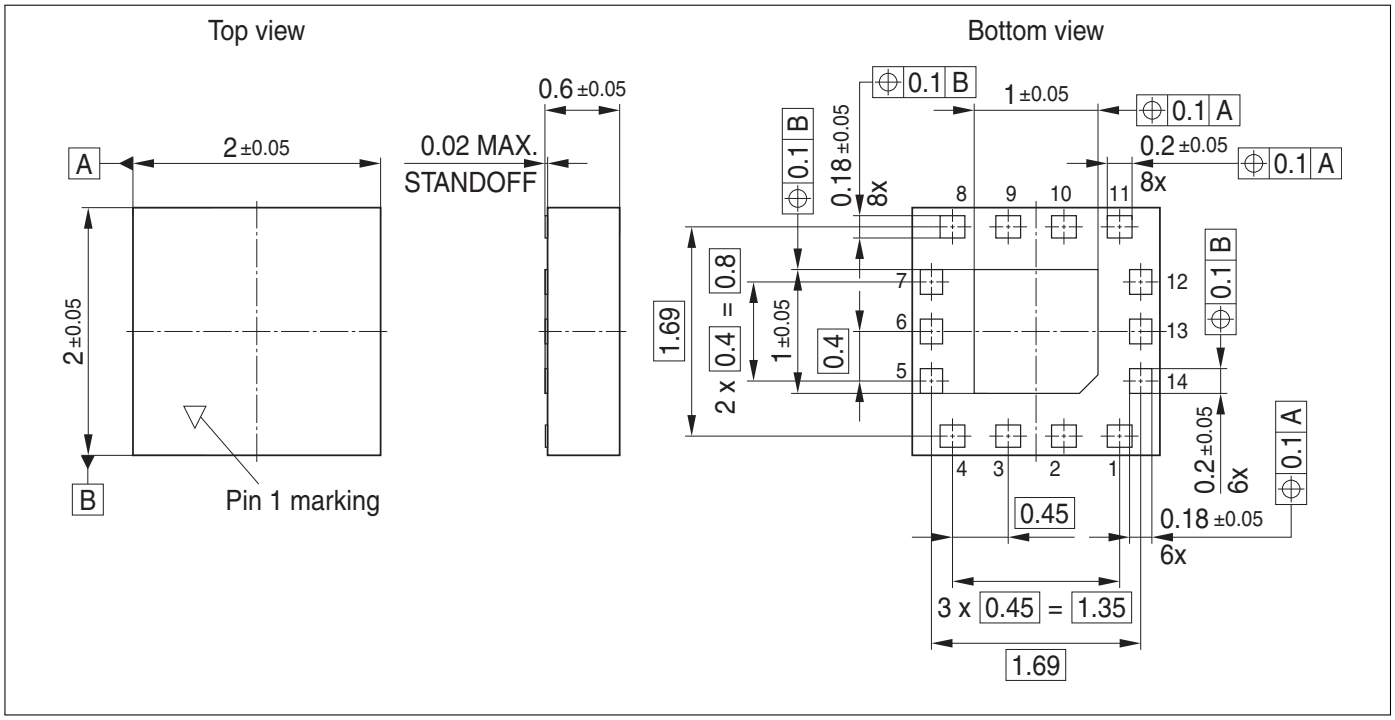


Figure 3: Package Outline Drawing

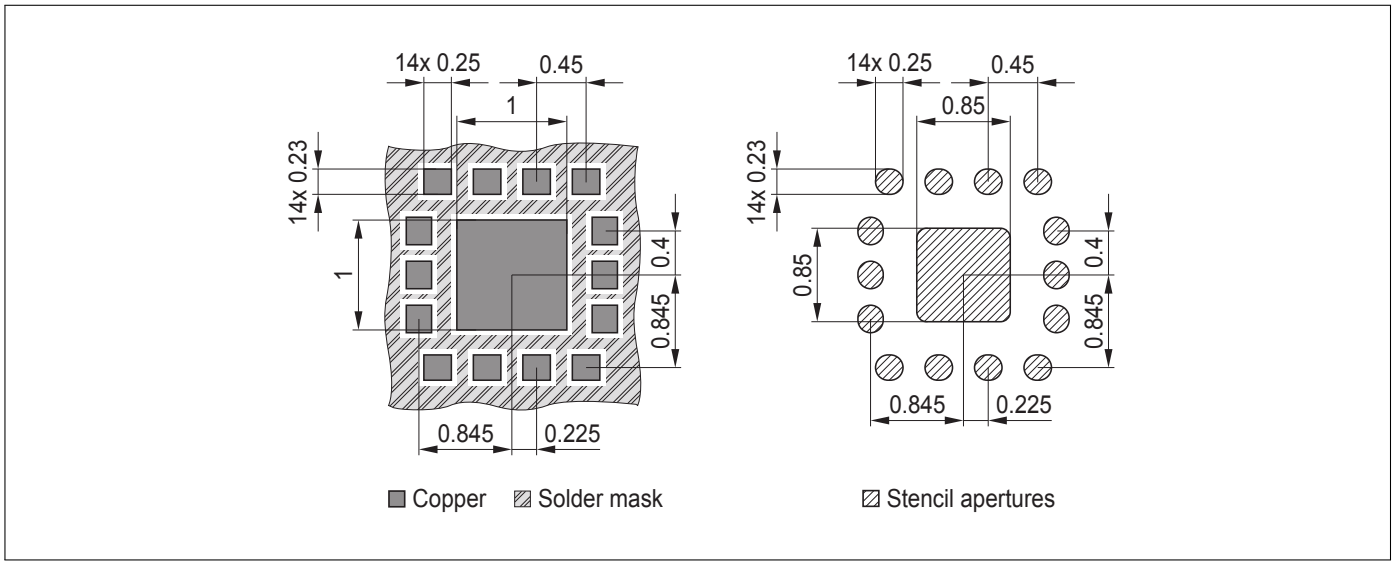


Figure 4: Land Pattern Drawing

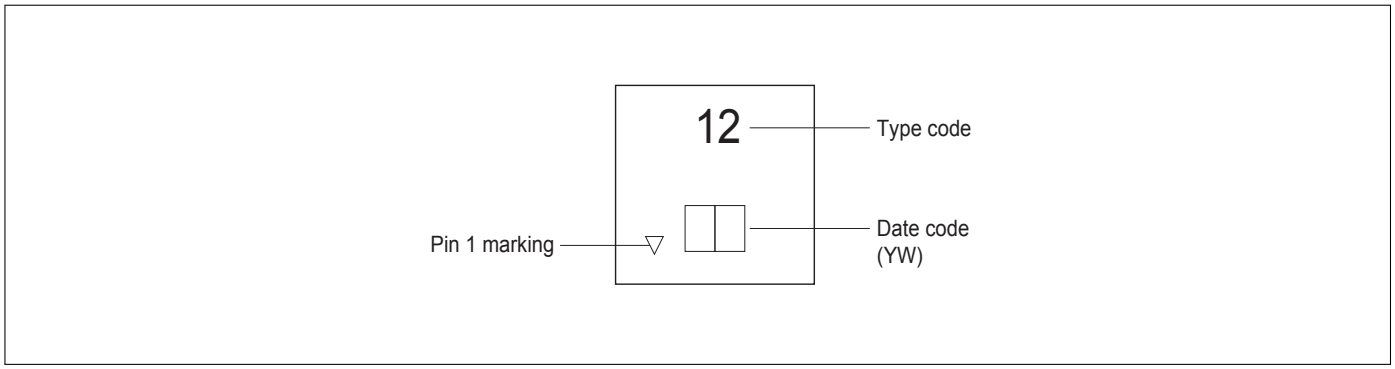


Figure 5: Laser marking

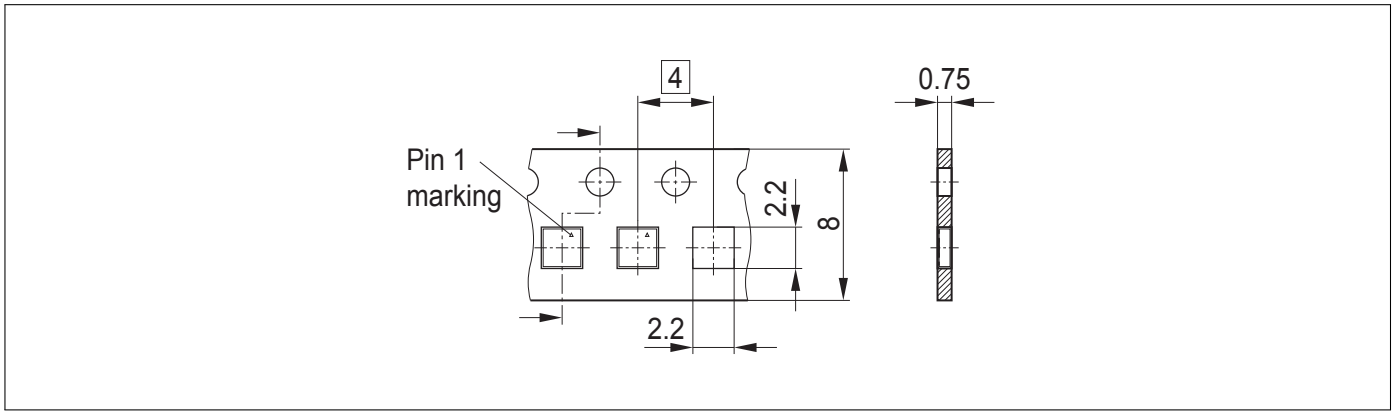


Figure 6: Carrier Tape

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