



MCP606/607/608/609

2.5V to 5.5V Micropower CMOS Op Amps

FEATURES

- Low Power $I_{DD} = 25 \mu A$, max
- Low Offset Voltage: 250 μV , max
- Rail-to-Rail Swing at Output
- 80 pA, Low Input Bias Current over Temperature
- Specifications rated for 2.5V to 5.5V Supplies
- Unity Gain Stable
- Chip Select (CS) Capability with MCP608
- Industrial Temperature range supported
- No Phase Reversal
- Available in Single, Dual, and Quad

APPLICATIONS

- Battery Power Instruments
- High Impedance Applications
 - Photodiode Pre-amps
 - pH probe Buffer Amplifier
 - Infrared Detectors
 - Precision Integrators
 - Charge Amplifier for Piezoelectric Transducers
- Strain Gauges
- Medical Instruments
- Test Equipment

AVAILABLE TOOLS

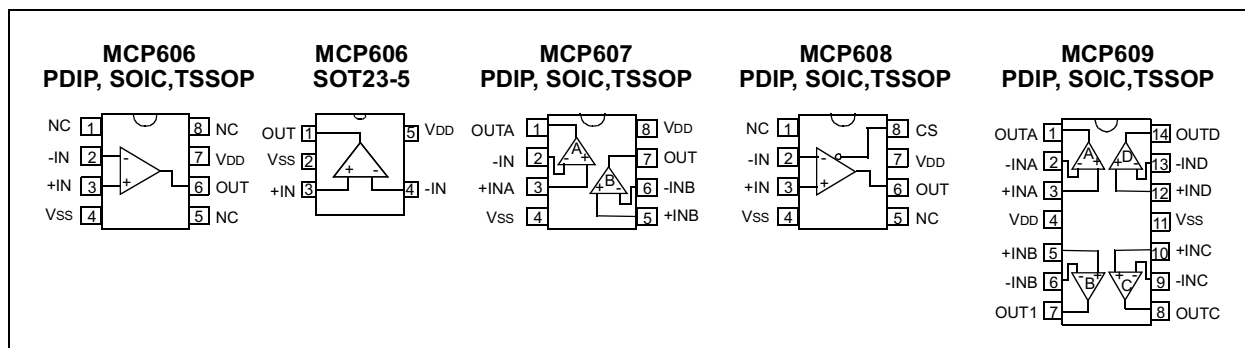
- Spice Macromodels (at www.microchip.com)
- FilterLab™ Software (at www.microchip.com)

DESCRIPTION

The MCP606, MCP607, MCP608 and MCP609 from Microchip Technology, Inc. are unity gain stable, low offset voltage operational amplifiers capable of precision low power single supply operation. Performance characteristics include ultra low offset voltage (250 μV max.), rail-to-rail output swing capability, and low input bias current (80 pA@85°C). These features make this family of amplifiers well suited for single supply precision, high impedance, battery powered applications.

The single MCP606 is available in standard 8-lead PDIP, SOIC, and TSSOP packages. Another version of the single op amp, MCP608 is offered with a Chip Select option in standard 8-lead PDIP, SOIC, and TSSOP packages. The dual MCP607 is offered in standard 8-lead PDIP, SOIC, as well as the TSSOP package. Finally, the quad MCP609 is offered in 14-lead PDIP, SOIC and TSSOP packages. All devices are fully specified from -40°C to +85°C with power supplies from 2.5V to 5.5V.

PACKAGES



MCP606/607/608/609

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

V_{DD} 7.0V
 All inputs and outputs w.r.t. $V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
 Difference Input voltage $|V_{DD} - V_{SS}|$
 Output Short Circuit Current continuous
 Current at Input Pin ± 2 mA
 Current at Output and Supply Pins ± 30 mA
 Storage temperature $-65^{\circ}C$ to $+150^{\circ}C$
 Ambient temp. with power applied $-55^{\circ}C$ to $+125^{\circ}C$
 Soldering temperature of leads (10 seconds) .. $+300^{\circ}C$
 ESD protection on all pins ≥ 2 kV

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
+IN/+INA/+INB/+INC/+IND	Non-inverting Input Terminals
-IN/-INA/-INB/-INC/-IND	Inverting Input Terminals
V_{DD}	Positive Power Supply
V_{SS}	Negative Power Supply
OUT/OUTA/OUTB/OUTC/OUTD	Output Terminals
CS	Chip Select
NC	No internal connection to IC

DC CHARACTERISTICS

Unless otherwise specified, all limits are specified for $V_{DD} = +2.5V$ to $+5.5V$, $V_{SS} = GND$, $T_A = 25^{\circ}C$, $V_{CM} = V_{DD}/2$, $R_L = 100\text{ k}\Omega$ to $V_{DD}/2$, and $V_{OUT} \sim V_{DD}/2$						
PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
INPUT OFFSET						
Input Offset Voltage	V_{OS}	-250	—	+250	μV	$T_A = -40^{\circ}C$ to $+85^{\circ}C$ for $V_{DD} = 2.5V$ to $5.5V$
Drift with Temperature	dV_{OS}/dT	—	± 1.8	—	$\mu V/^{\circ}C$	
Power Supply Rejection	PSRR	80	93	—	dB	
INPUT BIAS CURRENT AND IMPEDANCE						
Input Bias Current	I_B	—	1	—	pA	$T_A = -40^{\circ}C$ to $+85^{\circ}C$
Over Temperature	I_B	—	—	80	pA	
Input Offset Bias Current	I_{OS}	—	1	—	pA	
Common Mode Input Impedance	Z_{CM}	—	$10^{13} 6$	—	ΩpF	
Differential Input Impedance	Z_{DIFF}	—	$10^{13} 6$	—	ΩpF	
COMMON MODE						
Common-Mode Input Range	VCM	$V_{SS}-0.3$		$V_{DD}-1.1$	V	CMRR $\geq 75\text{ dB}$ $V_{DD} = 5V$, $V_{CM} = -0.3$ to $3.9V$
Common-Mode Rejection Ratio	CMRR	75	91	—	dB	
OPEN LOOP GAIN						
DC Open Loop Gain	A_{OL}	105	121	—	dB	$R_L = 25\text{ k}\Omega$ to $V_{DD}/2$, $50\text{ mV} < V_{OUT} <$ $(V_{DD} - 50\text{ mV})$ $R_L = 5\text{ k}\Omega$ to $V_{DD}/2$, $100\text{ mV} < V_{OUT} <$ $(V_{DD} - 100\text{ mV})$
DC Open Loop Gain	A_{OL}	100	118	—	dB	
OUTPUT						
Low Level/High Level Output Voltage Swing	V_{OL}, V_{OH}	$V_{SS} + 0.015$	—	$V_{DD} - 0.020$	V	$R_L = 25\text{ k}\Omega$ to $V_{DD}/2$ $R_L = 5\text{ k}\Omega$ to $V_{DD}/2$ $R_L = 25\text{ k}\Omega$ to $V_{DD}/2$, $A_{OL} \geq 105\text{ dB}$ $R_L = 5\text{ k}\Omega$ to $V_{DD}/2$, $A_{OL} \geq 100\text{ dB}$ $V_{OUT} = 2.5V$, $V_{DD} = 5V$
	V_{OL}, V_{OH}	$V_{SS} + 0.045$	—	$V_{DD} - 0.060$	V	
Linear Region Maximum Output Voltage Swing	V_{OUT}	$V_{SS} + 0.050$	—	$V_{DD} - 0.050$	V	
	V_{OUT}	$V_{SS} + 0.100$	—	$V_{DD} - 0.100$	V	
Output Short Circuit Current	I_{SC}		17		mA	
POWER SUPPLY						
Supply Voltage	V_S	2.5	—	5.5	V	$I_O = 0$
Quiescent Current Per Amplifier	I_O	—	18.7	25	μA	

MCP606/607/608/609

AC CHARACTERISTICS

Unless otherwise specified, all limits are specified for $V_{DD} = +2.5V$ to $+5.5V$, $V_{SS} = GND$, $T_A = 25^\circ C$, $V_{CM} = V_{DD}/2$, $R_L = 100\text{ k}\Omega$ to $V_{DD}/2$, and $V_{OUT} \sim V_{DD}/2$						
PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Gain Bandwidth Product	GBWP	—	155	—	kHz	$V_{DD} = 5V$, $C_L = 60\text{ pF}$
Phase Margin at Unity Crossing	θ	—	62	—	degrees	$V_{DD} = 5V$, $C_L = 60\text{ pF}$
Slew Rate	SR	—	0.08	—	V/ μs	$G = 1$, $V_{DD} = 5V$, $C_L = 60\text{ pF}$
Input Voltage Noise	e_n	—	2.8	—	μV_{p-p}	$f = 0.1\text{ Hz to }10\text{ Hz}$
Noise Density	e_n	—	38	—	nV/ $\sqrt{\text{Hz}}$	$f = 1\text{ kHz}$
Input Current Noise Density	i_n	—	3	—	fA/ $\sqrt{\text{Hz}}$	$f = 1\text{ kHz}$

SPECIFICATIONS FOR MCP608 CHIP SELECT FEATURE

Unless otherwise specified, all limits are specified for $V_{DD} = +2.5V$ to $+5.5V$, $V_{SS} = GND$, $T_A = 25^\circ C$, $V_{CM} = V_{DD}/2$, $R_L = 100\text{ k}\Omega$ to $V_{DD}/2$, and $V_{OUT} \sim V_{DD}/2$						
PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
CS LOW SPECIFICATIONS						
$\overline{CS}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	$0.2 V_{DD}$	V	For entire V_{DD} range
$\overline{CS}$ Input Current, Low	I_{CSL}	-0.1	0.01	—	μA	$\overline{CS} = 0.2V_{DD}$
CS HIGH SPECIFICATIONS						
$\overline{CS}$ Logic Threshold, High	V_{IH}	$0.8 V_{DD}$	—	V_{DD}	V	For entire V_{DD} range
$\overline{CS}$ Input Current, High	I_{CSH}	—	0.01	0.1	μA	$\overline{CS} = V_{DD}$
$\overline{CS}$ Input High, GND Current	I_Q	—	0.05	2	μA	$\overline{CS} = V_{DD}$
Amplifier Output Leakage, $\overline{CS}$ High	—	—	10	—	nA	$\overline{CS} = 0.8V_{DD}$
DYNAMIC SPECIFICATIONS						
$\overline{CS}$ Low to Amplifier Output High Turn-on Time	t_{ON}	—	9	100	μs	$\overline{CS}$ low = $0.2V_{DD}$, $V_{OUT} = 0.9 * V_{DD}/2$, $G = +1V/V$
$\overline{CS}$ High to Amplifier Output High Z	t_{OFF}	—	0.1	—	μs	$\overline{CS}$ high = $0.8V_{DD}$, $V_{OUT} = 0.1 * V_{DD}/2$, $G = +1V/V$
Hysteresis	—	—	0.6	—	V	$V_{DD} = 5V$

TEMPERATURE SPECIFICATIONS

Unless otherwise specified, all limits are specified for $V_{DD} = +2.5V$ to $+5.5V$, $V_{SS} = GND$						
PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TEMPERATURE RANGES						
Specified Temperature Range	T_A	-40	—	+85	$^\circ C$	
Operating Temperature Range	T_A	-40	—	+85	$^\circ C$	
Storage Temperature Range	T_A	-65	—	+150	$^\circ C$	
THERMAL PACKAGE RESISTANCE						
Thermal Resistance, 5L-SOT23	θ_{JA}	—	256	—	$^\circ C/W$	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	$^\circ C/W$	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	$^\circ C/W$	
Thermal Resistance, 8L-TSSOP	θ_{JA}	—	124	—	$^\circ C/W$	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	$^\circ C/W$	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	$^\circ C/W$	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	$^\circ C/W$	

2.0 TYPICAL PERFORMANCE CURVES

Note: Unless otherwise indicated, $T_A = 25^\circ\text{C}$, $V_{CM} = V_{DD}/2$ and $V_{OUT} \sim V_{DD}/2$, $V_{SS} = \text{GND}$.

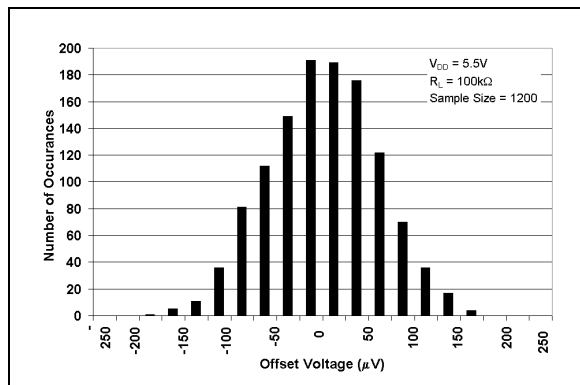


FIGURE 2-1: Offset Voltage vs. Number of Occurrences with $V_{DD} = 5.5\text{V}$.

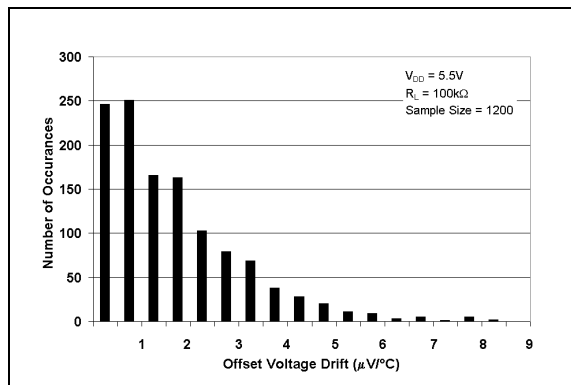


FIGURE 2-4: Offset Voltage Drift vs. Number of Occurrences with $V_{DD} = 5.5\text{V}$.

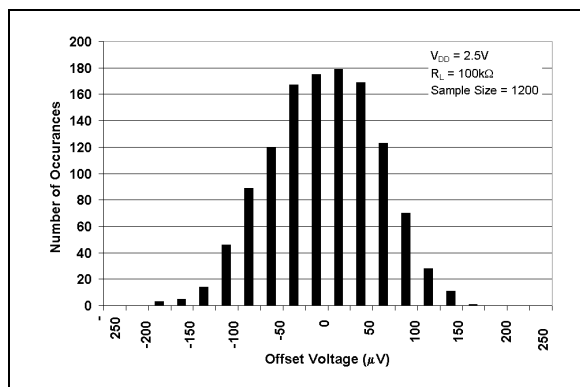


FIGURE 2-2: Offset Voltage vs. Number of Occurrences with $V_{DD} = 2.5\text{V}$.

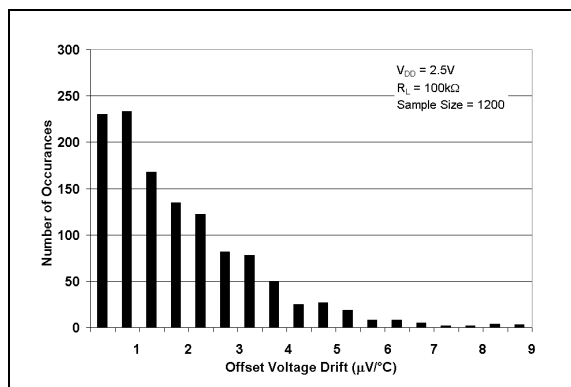


FIGURE 2-5: Offset Voltage Drift vs. Number of Occurrences with $V_{DD} = 2.5\text{V}$.

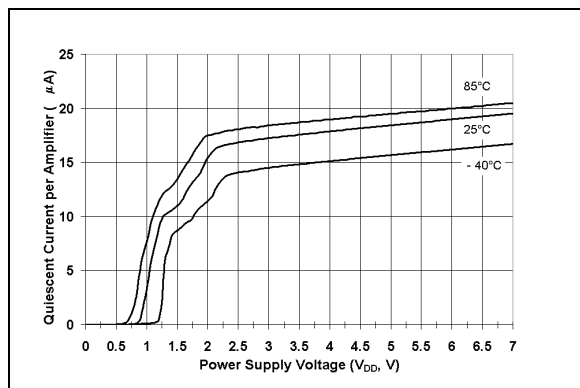


FIGURE 2-3: Quiescent Current vs. Power Supply Voltage vs. Temperature.

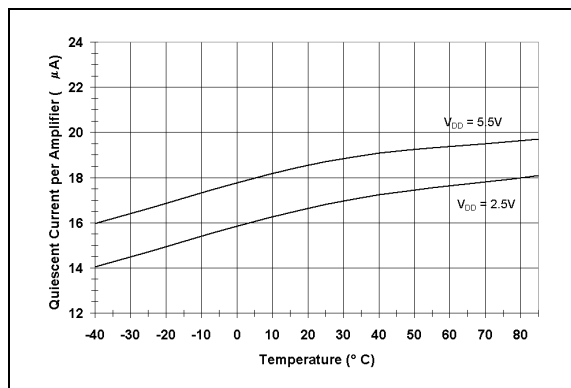


FIGURE 2-6: Quiescent Current vs. Temperature.

Note: Unless otherwise indicated, $T_A = 25^\circ\text{C}$, $V_{CM} = V_{DD}/2$ and $V_{OUT} \sim V_{DD}/2$, $V_{SS} = \text{GND}$.

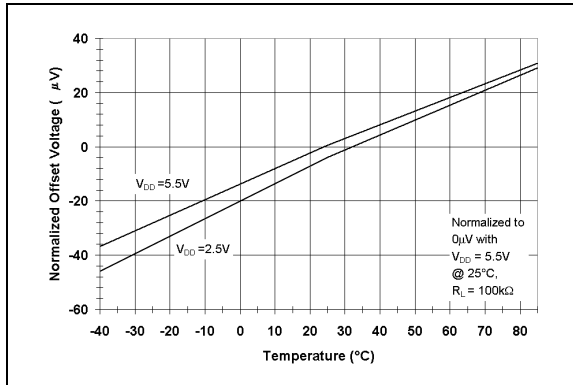


FIGURE 2-7: Normalized Offset Voltage vs. Temperature.

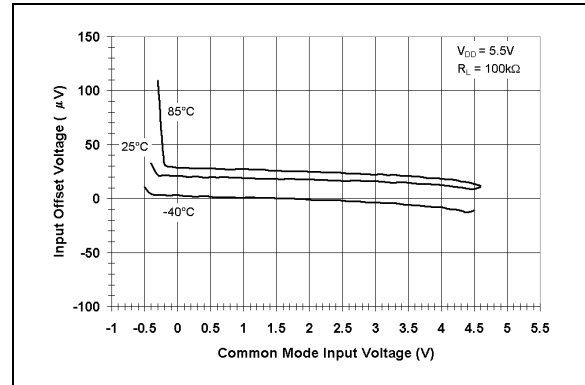


FIGURE 2-10: Input Offset Voltage vs. Common Mode Voltage.

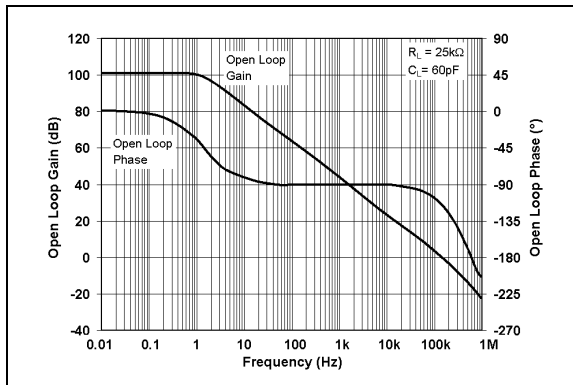


FIGURE 2-8: Open Loop Gain and Phase vs. Frequency.

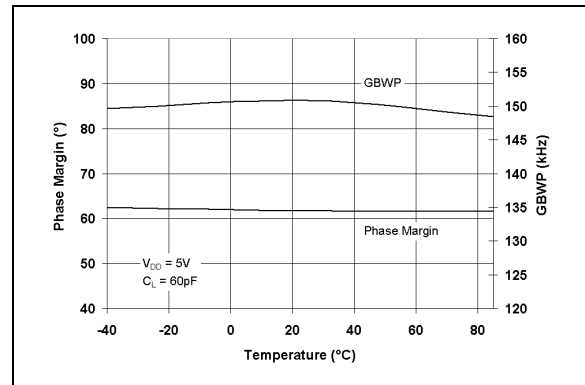


FIGURE 2-11: Phase Margin, Gain Bandwidth Product vs. Temperature.

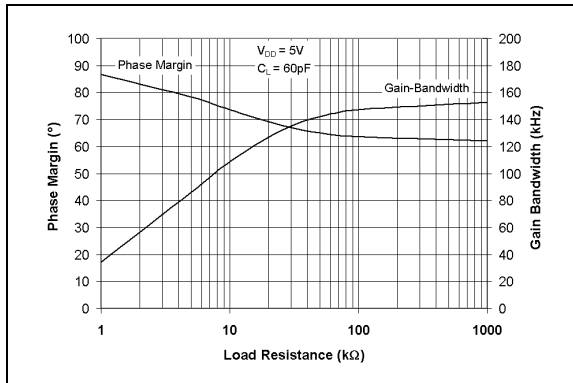


FIGURE 2-9: Phase Margin, Gain Bandwidth, vs. Load Resistance.

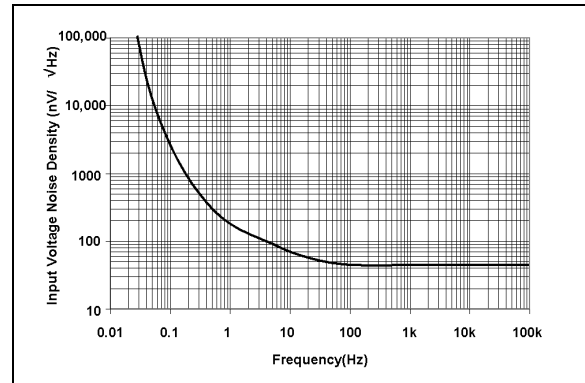


FIGURE 2-12: Input Voltage Noise Density vs. Frequency.

MCP606/607/608/609

Note: Unless otherwise indicated, $T_A = 25^\circ\text{C}$, $V_{CM} = V_{DD}/2$ and $V_{OUT} \sim V_{DD}/2$, $V_{SS} = \text{GND}$.

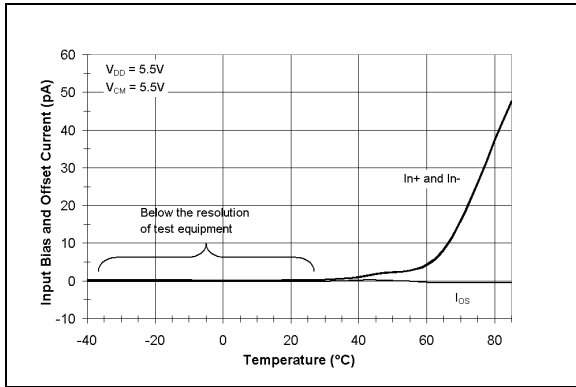


FIGURE 2-13: Input Bias Current, Input Offset Current vs. Temperature.

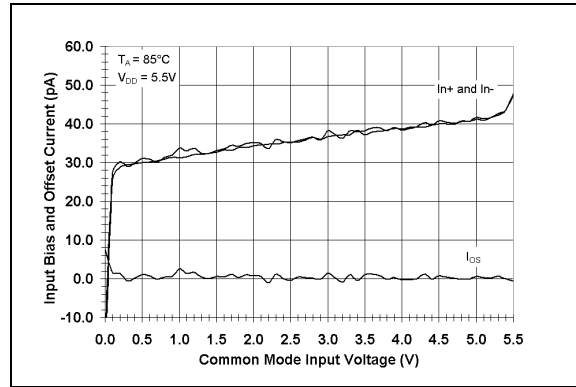


FIGURE 2-16: Input Bias Current, Input Offset Current vs. Common mode Input Voltage.

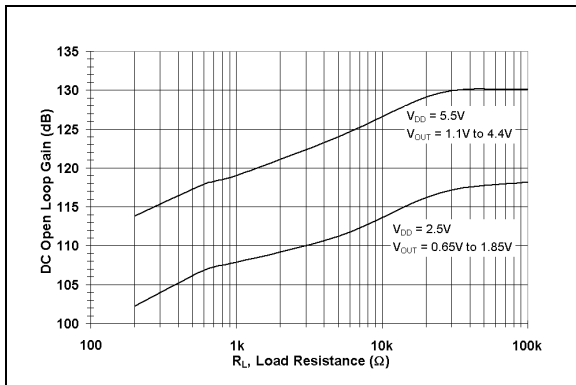


FIGURE 2-14: DC Open Loop Gain vs. Output Load Resistance.

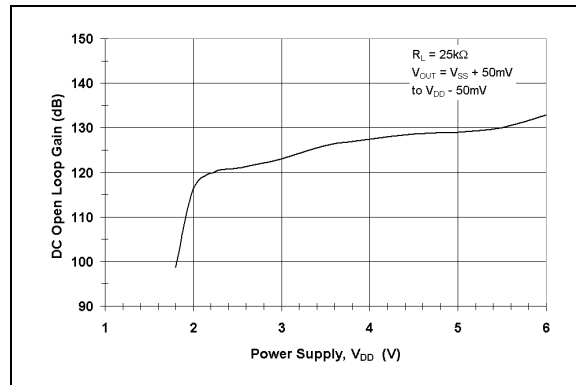


FIGURE 2-17: DC Open Loop Gain vs. Power Supply Voltage.

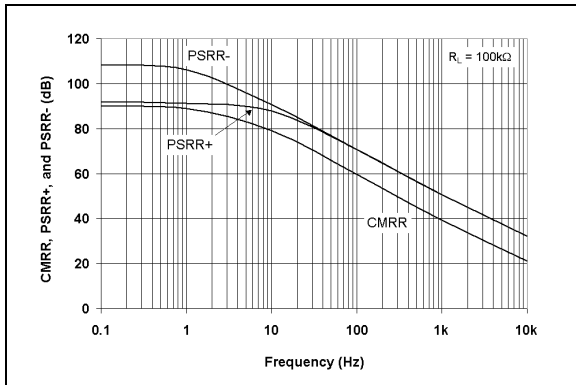


FIGURE 2-15: Common-Mode Rejection Ratio, Power Supply Rejection Ratio vs. Frequency.

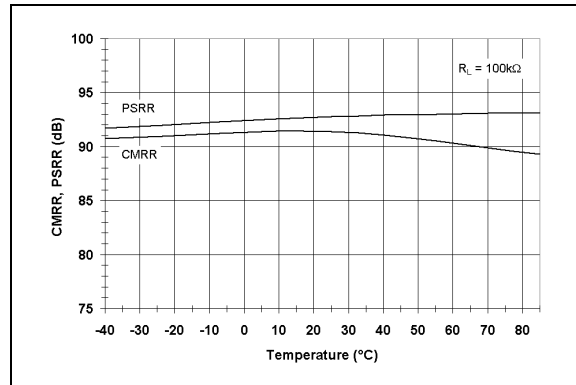


FIGURE 2-18: Common-Mode Rejection Ratio, Power Supply Rejection Ratio vs. Temperature.

Note: Unless otherwise indicated, $T_A = 25^\circ\text{C}$, $V_{CM} = V_{DD}/2$ and $V_{OUT} \sim V_{DD}/2$, $V_{SS} = \text{GND}$.

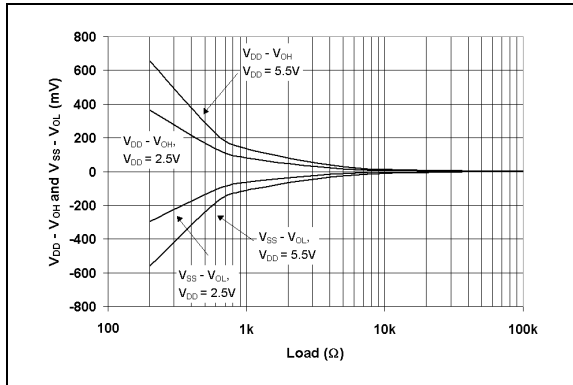


FIGURE 2-19: Low Level and High Level Output Swing vs. Load Resistance.

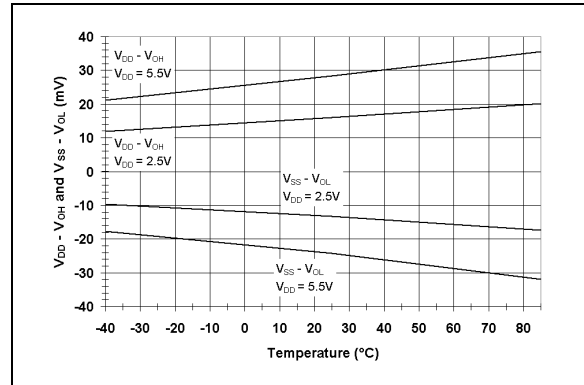


FIGURE 2-22: Low Level and High Level output Swing vs. Temperature, $R_L = 5\text{k}\Omega$.

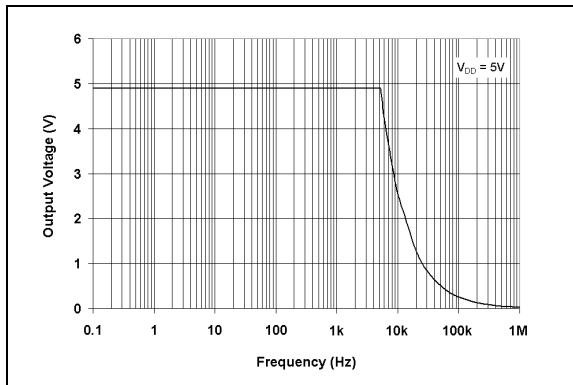


FIGURE 2-20: Maximum Output Voltage Swing vs. Frequency

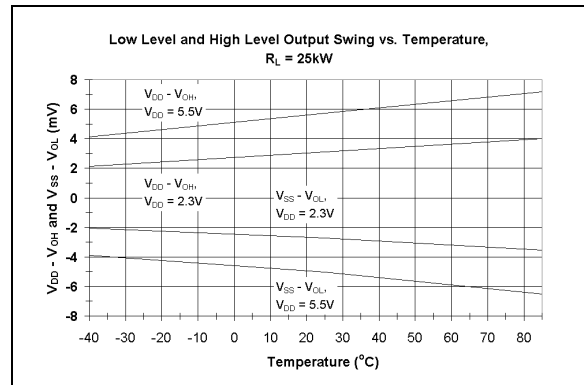


FIGURE 2-23: Low Level and High level Output Swing vs. Temperature, $R_L = 25\text{k}\Omega$

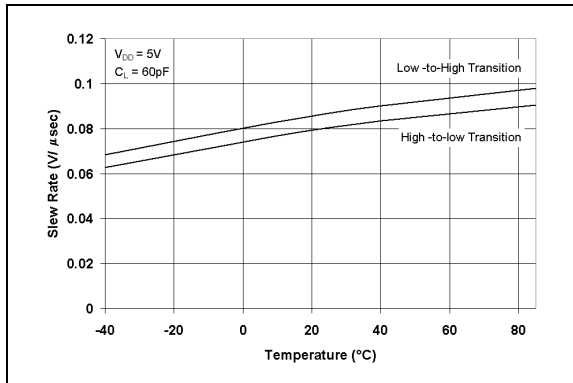


FIGURE 2-21: Slew Rate vs. Temperature.

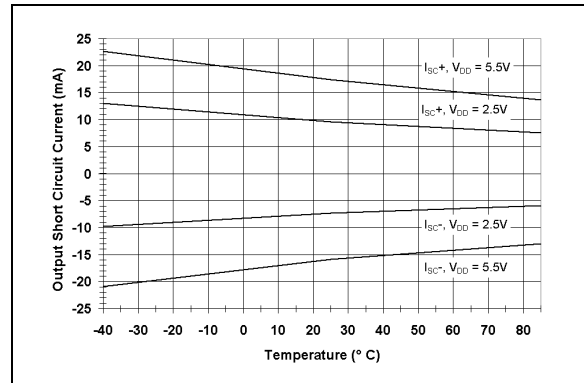


FIGURE 2-24: Output Short Circuit Current vs. Temperature.

MCP606/607/608/609

Note: Unless otherwise indicated, $T_A = 25^\circ\text{C}$, $V_{CM} = V_{DD}/2$ and $V_{OUT} \sim V_{DD}/2$, $V_{SS} = \text{GND}$.

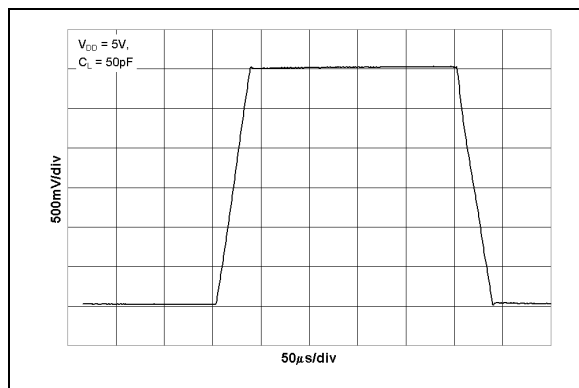


FIGURE 2-25: Large Signal Non-inverting Signal Pulse Response.

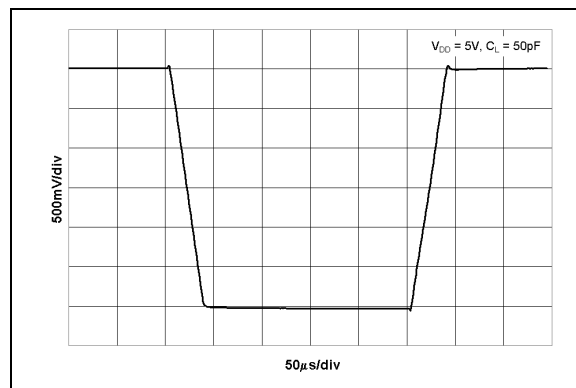


FIGURE 2-28: Large Signal Inverting Signal Pulse Response.

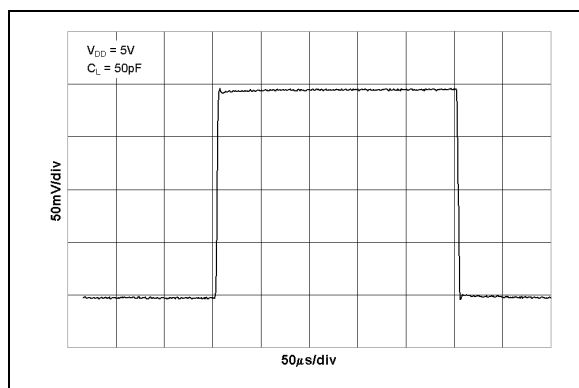


FIGURE 2-26: Small Signal Non-inverting Pulse Response.

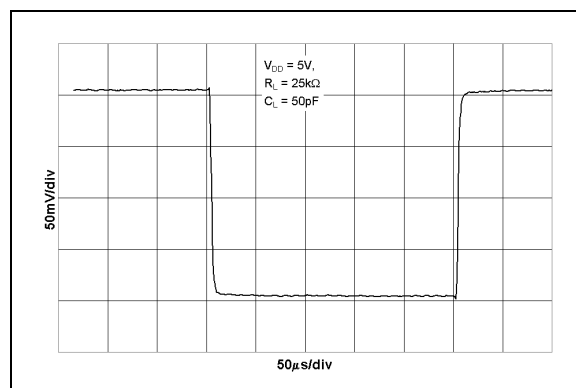


FIGURE 2-29: Small Signal Inverting Signal Pulse Response.

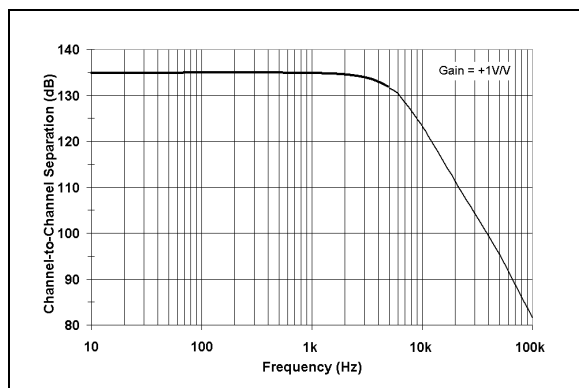


FIGURE 2-27: Channel to Channel Separation (MCP607 and MCP609 only).

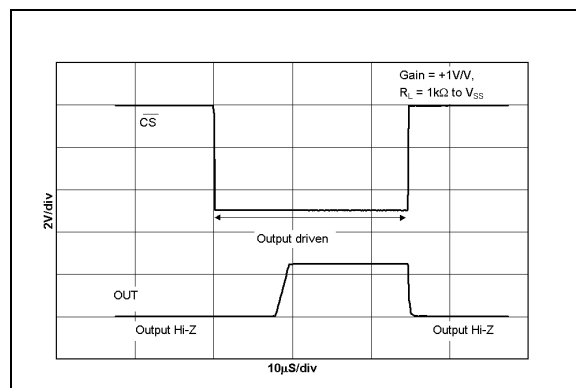


FIGURE 2-30: Chip Select to Amplifier Output Response Time (MCP608 only).

Note: Unless otherwise indicated, $T_A = 25^\circ\text{C}$, $V_{CM} = V_{DD} / 2$ and $V_{OUT} \sim V_{DD}/2$, $V_{SS} = \text{GND}$.

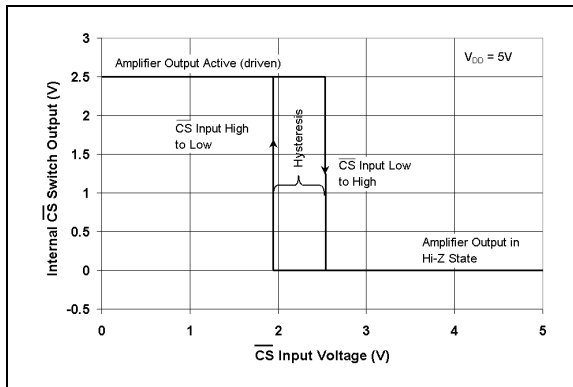


FIGURE 2-31: $\overline{CS}$ Hysteresis (MCP608 only).

3.0 APPLICATIONS INFORMATION

The MCP606/607/608/609 family of operational amplifiers are fabricated on Microchip's state-of-the-art CMOS process. They are unity gain stable and suitable for a wide range of general purpose applications. With this family of operational amplifiers, the power supply pin should be bypassed with a 0.1 μ F capacitor.

3.1 Rail-to-Rail Output Swing

There are two specifications that describe the output swing capability of the MCP606/607/608/609 family of operational amplifiers. The first specification, Low Level and High Level Output Voltage Swing, defines the absolute maximum swing that can be achieved under specified loaded conditions. For instance, the Low Level Output Voltage Swing of the MCP606/607/608/609 family is specified to be able to swing at least to 15 mV from the negative rail with a 25 k Ω load to $V_{DD}/2$.

This output swing performance is shown in Figure 3-1, where the output of an MCP606 is configured in a gain of +2V/V and overdriven with a 4 kHz triangle wave. In this figure, the degradation of the output swing linearity is clearly illustrated. This degradation occurs after the point at which the open loop gain of the amplifier is specified and before the amplifier reaches its maximum and minimum output swing.

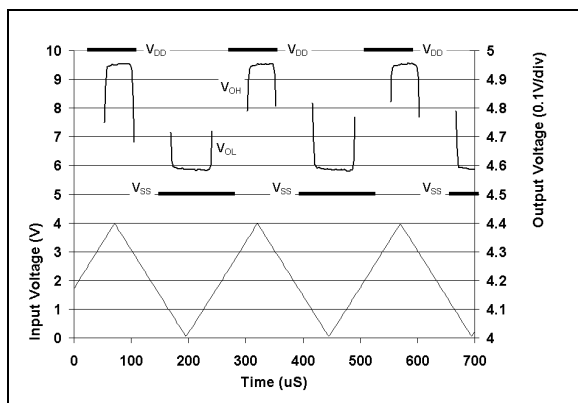


FIGURE 3-1: Low Level and High Level Output Swing.

The second specification that describes the output swing capability of these amplifiers is the Linear Region Maximum Output Voltage Swing. This specification defines the maximum output swing that can be achieved while the amplifier is still operating in its linear region.

The Linear Region Maximum Output Voltage Swing of the MCP606/607/608/609 family is specified within 50mV from the positive and negative rail with a 25 k Ω load and 100 mV from the rails with a 5 k Ω load. The overriding condition that defines the linear region of the amplifier is the open loop gain that is specified over that region. In the voltage output region between $V_{SS} + 50$ mV and $V_{DD} - 50$ mV, the open loop gain is specified to 105 dB (min) with a 25 k Ω load.

The classical definition of the DC open loop gain of an amplifier is:

$$A_{OL} = 20 \log_{10} \left(\frac{\Delta V_{OUT}}{\Delta V_{OS}} \right)$$

where:

A_{OL} is the DC open loop gain of the amplifier,

ΔV_{OUT} is equal to $(V_{DD} - 50 \text{ mV}) - (V_{SS} + 50 \text{ mV})$ for $R_L = 25 \text{ k}\Omega$, and

ΔV_{OS} is the change in offset voltage with the changing output voltage of the amplifier.

3.2 Input Voltage and Phase Reversal

Since the MCP606/607/608/609 amplifier family is designed with CMOS devices, it does not exhibit phase inversion when the input pins exceed the negative supply voltage. Figure 3-2 shows an input voltage exceeding both supplies with no resulting phase inversion.

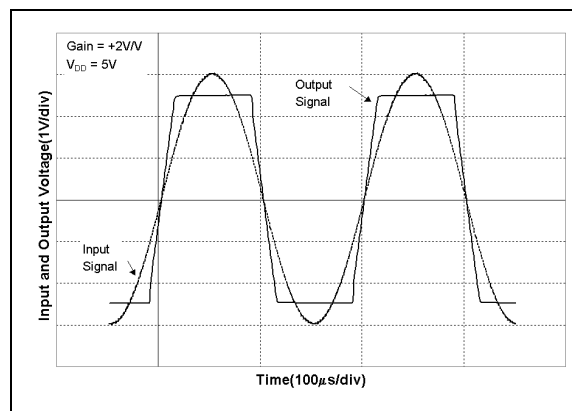


FIGURE 3-2: The MCP606/607/608/609 family of op amps do not have phase reversal issues. For this graph, the amplifier is in a gain of +2V/V.

The maximum operating common mode voltage that can be applied to the inputs is $V_{SS} - 0.3V$ to $V_{DD} - 1.1V$. In contrast, the absolute maximum input voltage is $V_{SS} - 0.3V$ and $V_{DD} + 0.3V$. Voltages on the input that exceed this absolute maximum rating can cause excessive current to flow in or out of the input pins. Current beyond ± 2 mA can cause possible reliability problems. Applications that exceed this rating must be externally limited with an input resistor as shown in Figure 3-3.

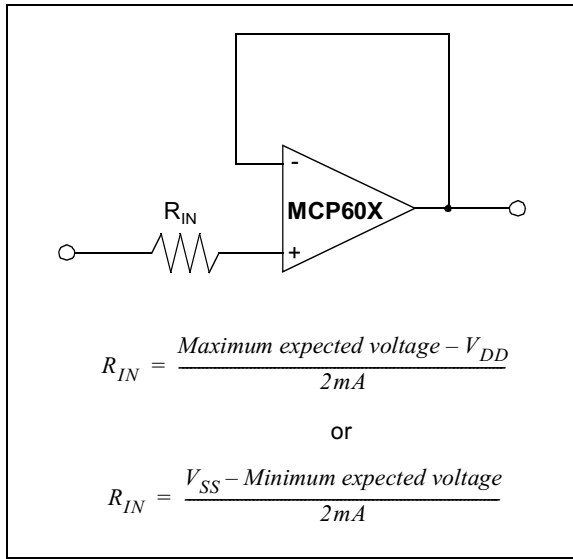


FIGURE 3-3: If the inputs of the amplifier exceed the Absolute Maximum Specifications, an input resistor, R_{IN} , should be used to limit the current flow into that pin.

3.3 Capacitive Load and Stability

Driving capacitive loads can cause stability problems with many of the higher speed amplifiers.

For any closed loop amplifier circuit, a good rule of thumb is to design for a phase margin that is no less than 45° . This is a conservative theoretical value, however, if the phase margin is lower, layout parasitics can degrade the phase margin further causing a truly unstable circuit. A system phase shift of 45° will have an overshoot in its step response of approximately 25%.

A buffer configuration with a capacitive load is the most difficult configuration for an amplifier to maintain stability. The Phase versus Capacitive Load of the MCP60X amplifier is shown in Figure 3-4. In this figure, it can be seen that the amplifier has a phase margin above 40° , while driving capacitance loads up to 220 pF.

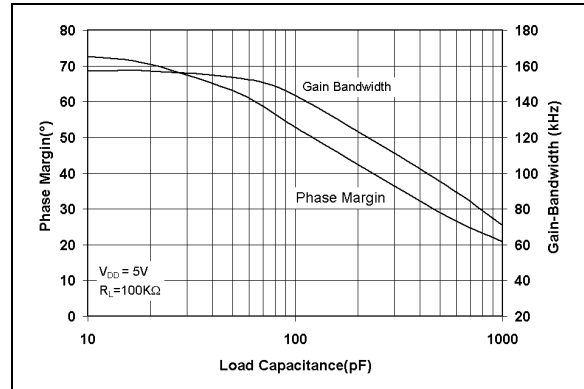


FIGURE 3-4: Gain Bandwidth, Phase Margin vs. Capacitive Load

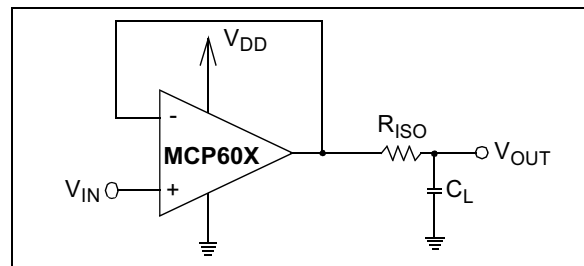


FIGURE 3-5: Amplifier circuits that can be used when driving heavy capacitive loads.

If the amplifier is required to drive larger capacitive loads, the circuit shown in Figure 3-5 can be used. A small series resistor (R_{ISO}) at the output of the amplifier improves the phase margin when driving large capacitive loads. This resistor decouples the capacitive load from the amplifier by introducing a zero in the transfer function.

This zero adjusts the phase margin by approximately:

$$\Delta\theta_m = \tan^{-1}(2\pi GBWP \times R_{ISO} \times C_L)$$

where:

$\Delta\theta_m$ is the improvement in phase margin,

$GBWP$ is the gain bandwidth product of the amplifier,

R_{ISO} is the capacitive decoupling resistor, and

C_L is the load capacitance

MCP606/607/608/609

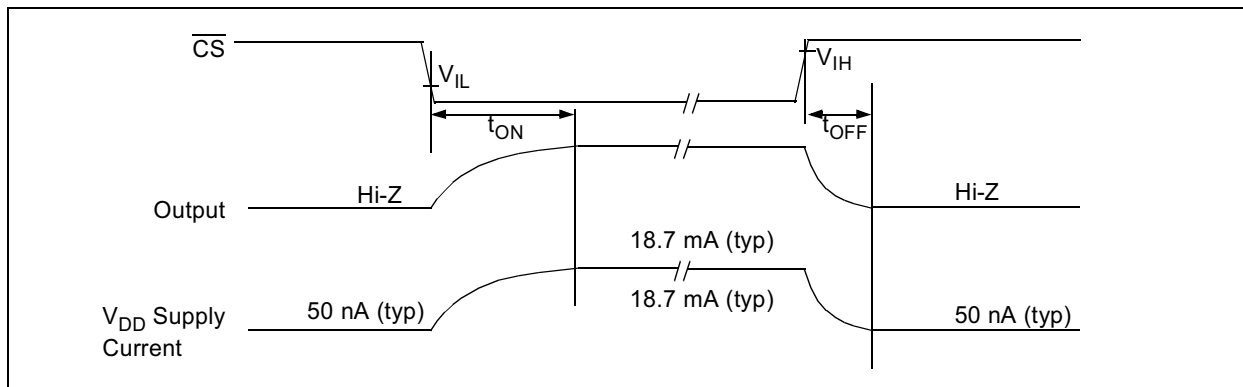


FIGURE 3-6: Timing Diagram for the $\overline{CS}$ function of the MCP608 amplifier.

3.4 The Chip Select Option of the MCP608

The MCP608 is a single amplifier with a Chip Select option. When $\overline{CS}$ is pulled high, the supply current drops to 50 nA (typ). In this state, the amplifier is put into a high impedance state. By pulling $\overline{CS}$ low, the amplifier is enabled. If the $\overline{CS}$ pin is left floating, the amplifier will not operate properly. Figure 3-6 shows the output voltage and supply current response to a $\overline{CS}$ pulse.

3.5 Layout Considerations

In applications where low input bias current is critical, PC board surface leakage effects and signal coupling from trace-to-trace need to be taken into consideration.

3.5.1 SURFACE LEAKAGE

Surface leakage across a PC board is a consequence of differing DC voltages between two traces combined with high humidity, dust or contamination on the board. For instance, the typical resistance from PC board trace-to-pad is approximately $10^{12} \Omega$ under low humidity conditions. If an adjacent trace is biased to 5V and the input pin of the amplifier is biased at or near zero volts, a 5 pA leakage current will appear on the amplifier's input node. This type of PCB leakage is five times the room temperature input bias current (1 pA, typ) of the MCP606/607/608/609 family of amplifiers.

The simplest technique that can be used to reduce the effects of PC board leakage is to design a ring around sensitive pins and traces. An example of this type of layout is shown in Figure 3-7.

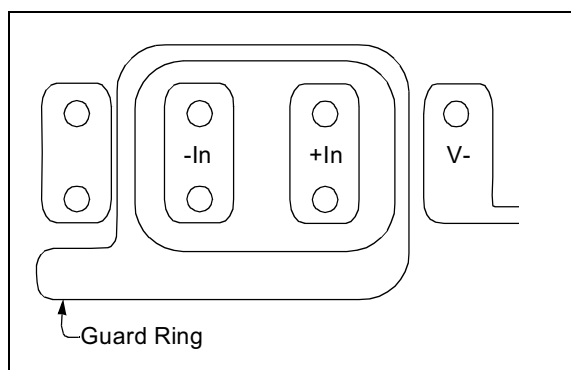


FIGURE 3-7: Example of Guard Ring for the MCP606, the A-amplifier of the MCP607 or the MCP608 in a PC Board Layout.

Circuit examples of ring implementations are shown in Figure 3-8. In Figure 3-8A, B and C, the guard ring is biased to the common mode voltage of the amplifier. This type of guard ring is most effective for applications where the common mode voltage of the input stage changes, such as buffers, non-inverting gain amplifiers or instrumentation amplifiers.

The strategy shown in Figure 3-8D, biases the common mode voltage and guard ring to ground. This type of guard ring is typically used in precision photo sensing circuits.

Figure 3-8A

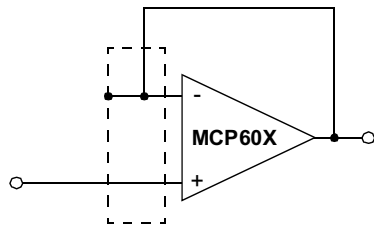


Figure 3-8B

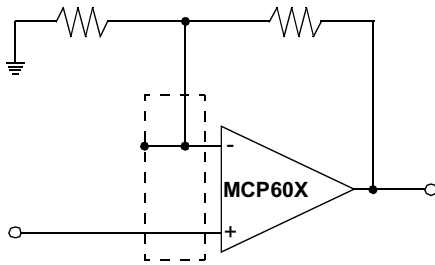


Figure 3-8C

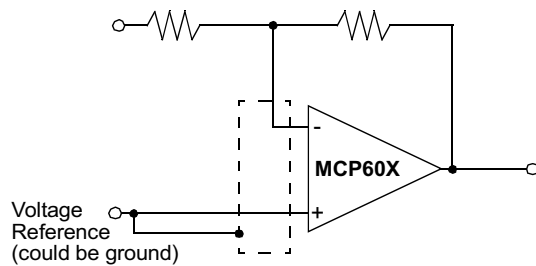


Figure 3-8D

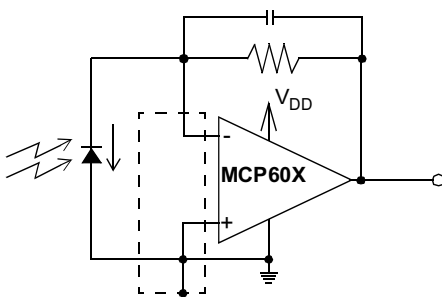


FIGURE 3-8: Examples of how to design PC Board traces to minimize leakage paths to the high impedance input pins of the MCP606/607/608/609 amplifiers.

3.5.2 SIGNAL COUPLING

The input pins of the MCP606/607/608/609 amplifiers have a high impedance providing an opportunity for noise injection if layout issues are not considered. These high impedance input terminals are sensitive to injected currents. This can occur if the trace from a high impedance input is next to a trace that has fast changing voltages, such as a digital or clock signal. When a high impedance trace is in close proximity to a trace with these types of voltage changes, charge is capacitively coupled into the high impedance trace.

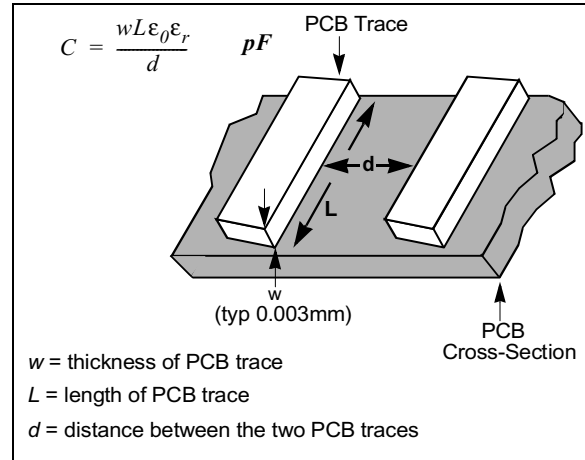


FIGURE 3-9: Capacitors can be built with PCB traces allowing for coupling of signals from one trace to another.

As shown in Figure 3-9, the value of the capacitance between two traces is primarily dependent on the distance (d) between the traces and the distance that the two traces are in parallel (L). From this model, the amount of current generated into the high impedance trace is equal to:

$$I = C \frac{\partial V}{\partial t}$$

where:

I equals the current that appears on the high impedance trace.

C equals the value of capacitance between the two PCB traces.

∂V equals the change in voltage of the trace that is switching.

∂t equals the amount of time that the voltage change took to get from one level to the next.

MCP606/607/608/609

3.6 Typical Applications

3.6.1 LOW SIDE BATTERY CURRENT SENSING

The MCP606/607/608/609 amplifiers can be used to sense the output current on the low side of a battery using the circuit in Figure 3-10. In this circuit, the current from the power supply (minus the current required to power the MCP606) flows through a ten ohm resistor from the rest of the circuit in the system. This current is converted to a voltage through the sense resistor and gained by the resistors around the amplifier. Since the input bias current and offset voltage of the MCP606 is low, there is very little error generated by the amplifier. Additionally, the amplifier is capable of swinging below ground and the quiescent current is very low. These four specifications make this amplifier appropriate for this type of circuit.

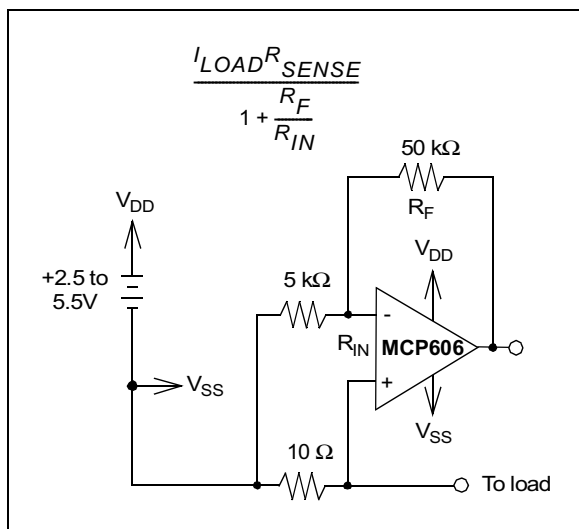


FIGURE 3-10: Low Side Battery Current Sensing

3.6.2 PREAMPLIFIER FOR PHOTO DETECTION CIRCUIT

Any amplifier from this family of operational amplifiers can be used to convert an output current signal from a sensor into a voltage. A sensor that fits this description is a photodiode as shown in Figure 3-11. This type of circuit is implemented with a single resistor and an optional capacitor in the feedback loop of the amplifier. As light impinges on the photo diode, charge is generated, causing a current to flow in the reverse bias direction of the photodiode.

Two circuits are shown in Figure 3-11. The top circuit is designed to provide precision sensing from the photodiode. In this circuit, the voltage across the detector is nearly zero and equal to the offset voltage of the amplifier. With this configuration, current that appears across the resistor, R₂, is primarily a result of the light excitation on the photodiode. The photosensing circuit on the bottom of Figure 3-11 is designed for higher

speed sensing. This is done by reverse biasing the photodiode, which reduces the parasitic capacitance of the diode.

The key specifications that influence the accuracy of these circuits are low offset voltage, low input bias current, high input impedance and an input common mode range below ground. The low input offset voltage and low input bias current provide an environment where there is minimal voltage placed across the photodiode, consequently the linearity of the photodiode is not compromised. Given that the MCP606/607/608/609 amplifiers are specified for a ±250 μV (max) offset voltage and input bias currents in the pico ampere region, they are ideal for these circuits. Additionally, these two circuits will only work if the common mode range of the amplifier includes zero, which is the case with the MCP606/607/608/609 amplifiers.

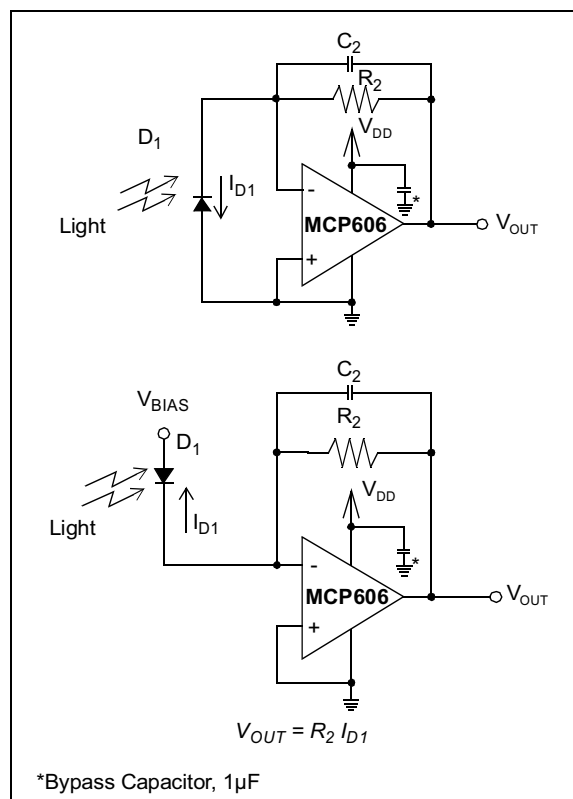


FIGURE 3-11: Pre-Amplifier for Photo Detection Circuit.

3.6.3 TWO OP AMP INSTRUMENTATION AMPLIFIER

The two op amp instrumentation amplifier shown in Figure 3-12 serves the function of taking the difference of two input voltages, level shifting then and providing a single output. This configuration is best suited for higher gains. "(gain > 3 V/V)" is shown in Figure 3-12. The key specifications that make the MCP606/607/608/609 family appropriate for this application circuit are low input bias current, low offset voltage and high common-mode rejection. The reference voltage of this circuit is supplied to the first op amp in the signal chain. Typically, this voltage is half of the supply voltage in a single supply environment.

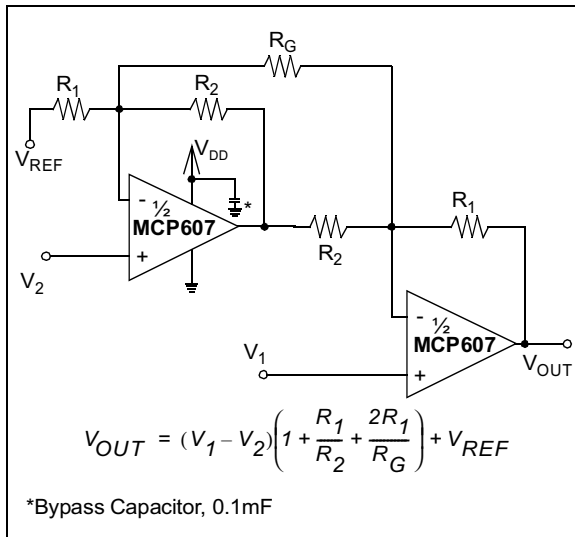


FIGURE 3-12: Two Op Amp Instrumentation Amplifier

3.6.4 THREE OP AMP INSTRUMENTATION AMPLIFIER

A classic, three op amp instrumentation amplifier is illustrated in Figure 3-15. The input operational amplifiers in this circuit provide signal gain. The output operational amplifier converts the signal from two inputs to a single ended output with a difference amplifier. The gain of this circuit is simply adjusted with one resistor, R_G . The reference voltage of the difference stage of this instrumentation amplifier is capable of spanning a wide range. Most typically, this node is referenced to half of the supply voltage in a signal supply application.

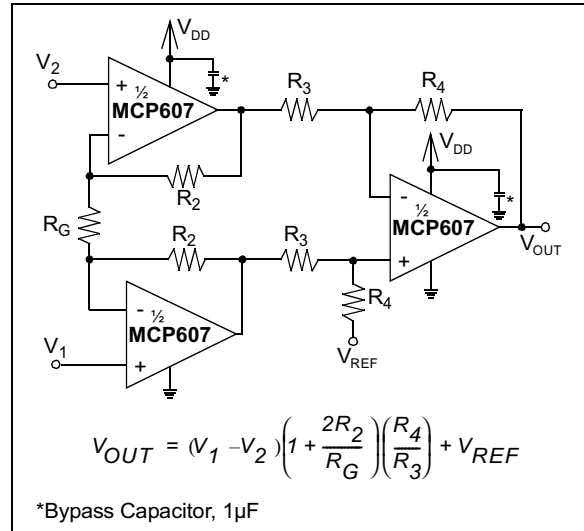


FIGURE 3-13: Three Op Amp Instrumentation Amplifier.

3.6.5 PRECISION GAIN WITH GOOD LOAD ISOLATION

In Figure 3-14, the low input offset voltage of the MCP606 is used to implement a circuit with a high gain. This precision measurement can easily be disrupted by changing the output current drive of the device that is doing the amplification work. Consequently, the precision amplifier configuration is followed by a MCP601 amplifier which is capable of driving higher currents. Since the two amplifiers are housed in separate packages, there is minimal change in offset voltage of the MCP606 due to loading effects.

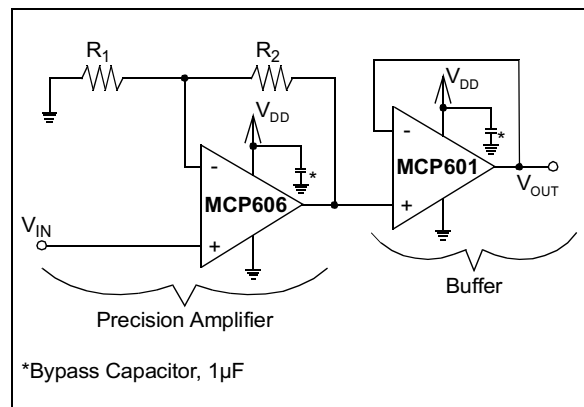


FIGURE 3-14: Precision Gain with Good Load Isolation.

MCP606/607/608/609

4.0 SPICE MACROMODEL

The Spice macromodel for the MCP606, MCP607, MCP608 and MCP609 simulates the typical amplifier performance of offset voltage, DC power supply rejection, input capacitance, DC common mode rejection ratio, open loop gain over frequency, phase margin with no capacitive load, output swing, DC power supply current, power supply current change with supply voltage, input common mode range and input voltage noise.

The characteristics of the MCP606, MCP607, MCP608, and MCP609 amplifiers are similar in terms of performance and behavior. This single op amp macromodel supports all four devices with the exception of the chip select function of the MCP608, which is not modeled.

The listing for this macromodel is shown on the next page. The most recent revision of the model can be downloaded from Microchip's web site at www.microchip.com.

Software License Agreement

The software supplied herewith by Microchip Technology Incorporated (the "Company") is intended and supplied to you, the Company's customer, for use solely and exclusively on Microchip products.

The software is owned by the Company and/or its supplier, and is protected under applicable copyright laws. All rights are reserved. Any use in violation of the foregoing restrictions may subject the user to criminal sanctions under applicable laws, as well as to civil liability for the breach of the terms and conditions of this license.

THIS SOFTWARE IS PROVIDED IN AN "AS IS" CONDITION. NO WARRANTIES, WHETHER EXPRESS, IMPLIED OR STATUTORY, INCLUDING, BUT NOT LIMITED TO, IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE APPLY TO THIS SOFTWARE. THE COMPANY SHALL NOT, IN ANY CIRCUMSTANCES, BE LIABLE FOR SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES, FOR ANY REASON WHATSOEVER.

```
.subckt mcp606 1 2 3 4 5
*
*      | | | |
*      | | | | Output
*      | | | Negative supply
*      | | Positive Supply
*      | Inverting input
*      Non-inverting input
*
* Macromodel for MCP606 (single), MCP607 (dual), MCP608 (single w/CS), and MCP609 (quad)
*
* The characteristics of the MCP606, MCP607, MCP608, and MCP609 have the same fundamental
* performance and behavior. Consequently, this single op amp macromodel supports all four
* devices. However, the chip select function of the MCP608 is not modeled.
*
* Revision History:
*   REV A : 6-30-99   created   BCB
*
* This macromodel models typical amplifier offset voltage, DC power supply rejection, input
* capacitance, open loop gain over frequency, phase margin with 60pF load, output swing,
* power supply current, input voltage noise, slew rate.
*
* NOTICE: THE INFORMATION PROVIDED HEREIN IS BELIEVED TO BE RELIABLE,
* HOWEVER, MICROCHIP ASSUMES NO RESPONSIBILITY FOR INACCURACIES OR
* OMISSIONS. MICROCHIP ASSUMES NO RESPONSIBILITY FOR THE USE OF THIS
* INFORMATION, AND ALL USE OF SUCH INFORMATION SHALL BE ENTIRELY AT
* THE USER'S OWN RISK. NO INTELLECTUAL PROPERTY RIGHTS OR LICENSES
* TO ANY OF THE TECHNOLOGY DESCRIBED HEREIN ARE IMPLIED OR GRANTED TO
* ANY THIRD PARTY. MICROCHIP RESERVES THE RIGHT TO CHANGE THIS MODEL
* AT ANY TIME WITHOUT NOTICE.
*
*
*Input Stage, pole at 300kHz
M1      9      64      7      3      Ptype
M2      8      2      7      3      Ptype
CDIFF   1      2      3E-12
CCM1    1      4      6E-12
CCM2    2      4      6E-12
IDD     3      7      13.33e-6
RA      8      6      1.839e3
RB      9      6      1.839e3
CA      8      9      125e-12
ICOMP   3      4      -194.63e-6

*Input Stage Common-Mode Clamping
VCMM    4      6      0.35
ECM     55     4      3 64 1

RCM     57     56     1E3
DCMP    56     55     DY
VCMP    57     4      1.2
```

MCP606/607/608/609

```
RST      58      59      1E3
DST      59      55      DX
VST      58      4       1.6

GCMP2   23 4 POLY(2) 57 56 58 59 0 0 0;0 -0.5E-3 0.5E-3

*Input errors (vos, en, psr)

ERR    64    1 poly(2) (67,4) (3, 4) -229.9e-6 1 23e-6

*Second Stage, pole at 0.183Hz
GS      23      4      8      9      543.78e-6
R1      23      4      8.2144e9
C2      23      4      110e-12

VSOM     3      24      4.784
VSOP     25      4      -3.98
DSOM     23      24      DY
DSOP     25      23      DY

*HCM     23      3      VCMP

FS 3 4 POLY(11) VO3 VO5 VO4 VO6 VO1 VO2 VO9 VO10 VMID1 VSOP VSOM
+ 200E-6 -1 -1 -1 1 -1 -1 1 1 -1 -1 -1

*mid-supply reference
RMID1    3      35      61.62E3
VMID1    35      34      0
RMID2    4      34      61.62E3
ELEVEL   34      4      23      4      -1

*output stage
DO3      34      43      DY
DO4      44      34      DY
DO5      3      45      DY
DO6      3      46      DY
DO7      4      45      DY
DO8      4      46      DY
VO3      43      5      0.1
VO4      5      44      0.03

GO5      3      47      3      34      10E-3
VO5      47      5      0
GO6      4      48      34      4      10E-3
VO6      48      5      0
GO1      49      4      5      34      10E-3
VO1      49      45      0

GO2      50      4      34      5      10E-3
VO2      50      46      0
RO9      3      51      100
VO9      51      5      0
RO10     52      4      100
VO10     52      5      0

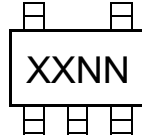
* input voltage noise
VN1      65      4      0.6
DN1      65      67      DX
RN1      67      4      10E3

.model Ptype PMOS L=2 W=105
.model DY D (IS=1e-15 BV =50)
.model DX D (IS=1e-18 AF=0.6 KF=10e-17)
.ENDS
```

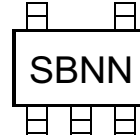
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

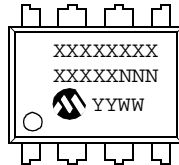
5-Lead SOT-23-5



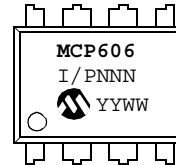
Example:



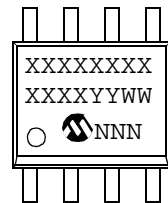
8-Lead PDIP (300 mil)



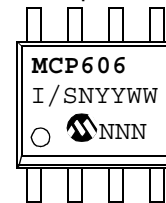
Example:



8-Lead SOIC (150 mil)



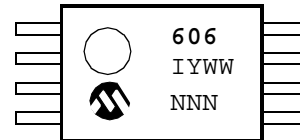
Example:



8-Lead TSSOP



Example:



Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

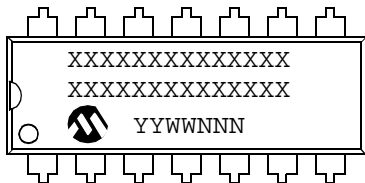
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code). For marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

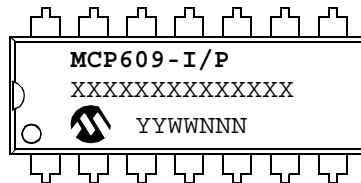
MCP606/607/608/609

Package Marking Information (Continued)

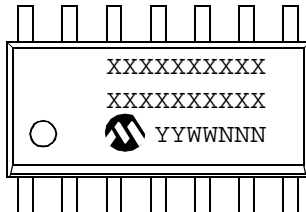
14-Lead PDIP (300 mil) (MCP609)



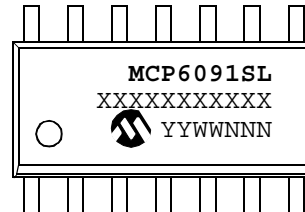
Example:



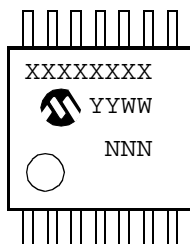
14-Lead SOIC (150 mil) (MCP609)



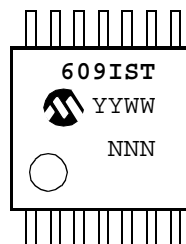
Example:



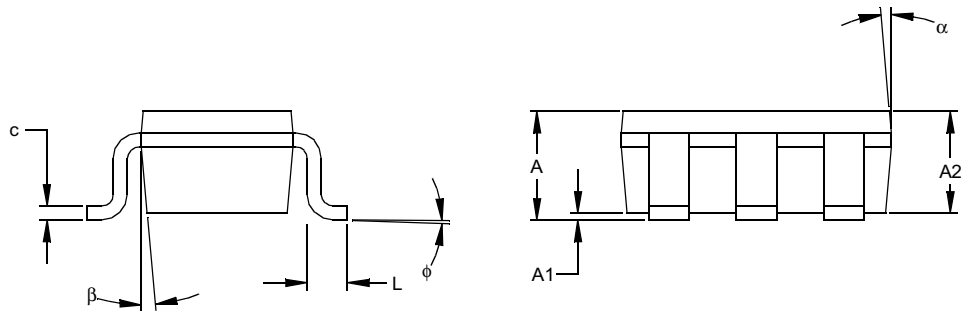
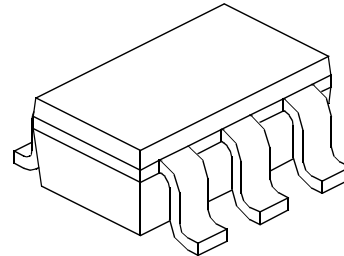
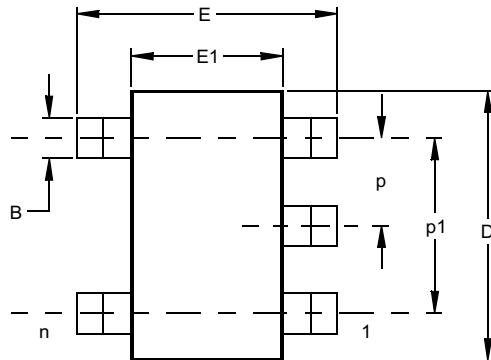
14-Lead TSSOP (MCP609)



Example:



5-Lead Plastic Small Outline Transistor (OT) (SOT23)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		5			5	
Pitch	p		.038			0.95	
Outside lead pitch (basic)	p1		.075			1.90	
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff §	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	φ	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

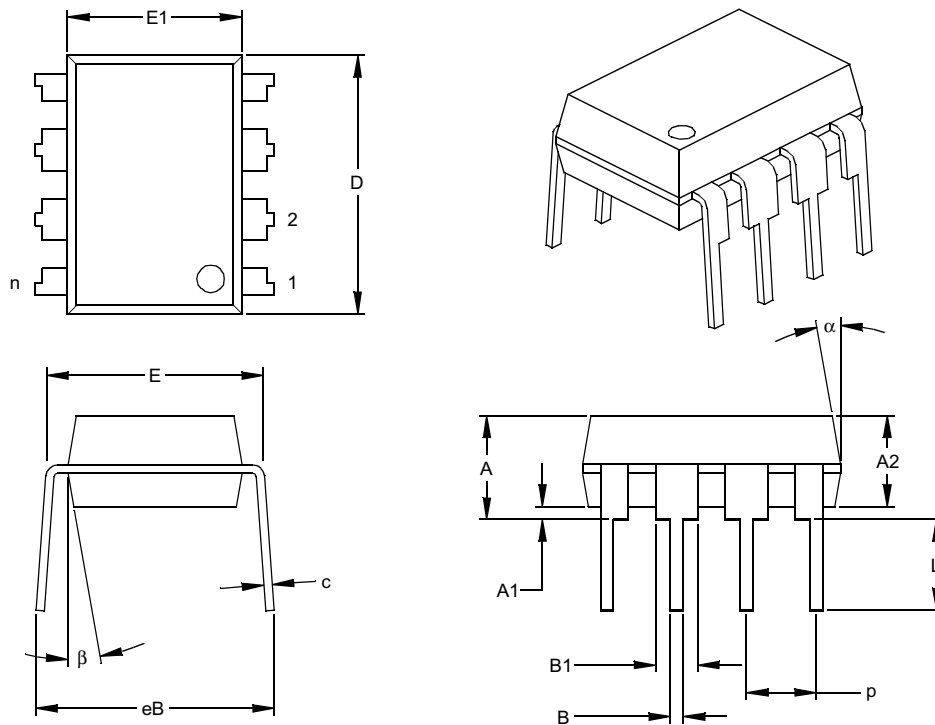
* Controlling Parameter
§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MO-178
Drawing No. C04-091

MCP606/607/608/609

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter

§ Significant Characteristic

Notes:

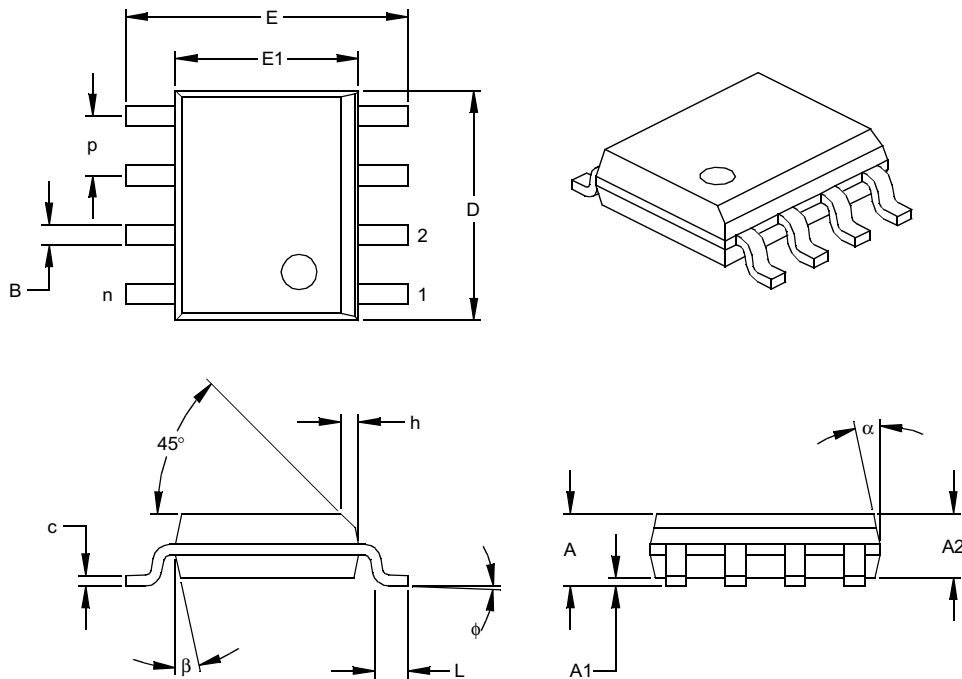
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-001

Drawing No. C04-018

MCP606/607/608/609

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:

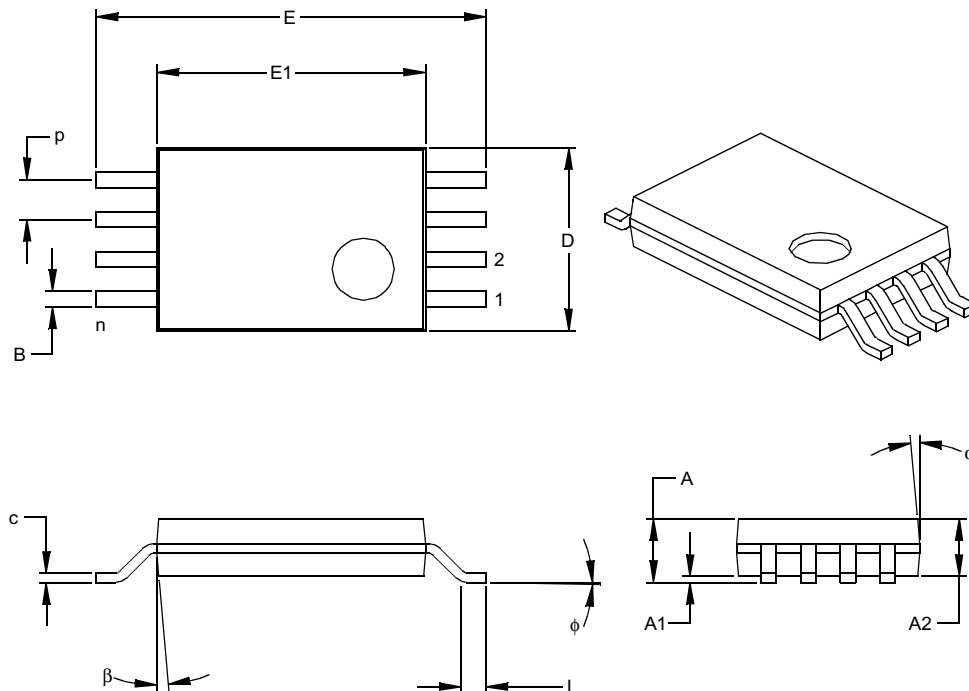
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-012

Drawing No. C04-057

MCP606/607/608/609

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter

§ Significant Characteristic

Notes:

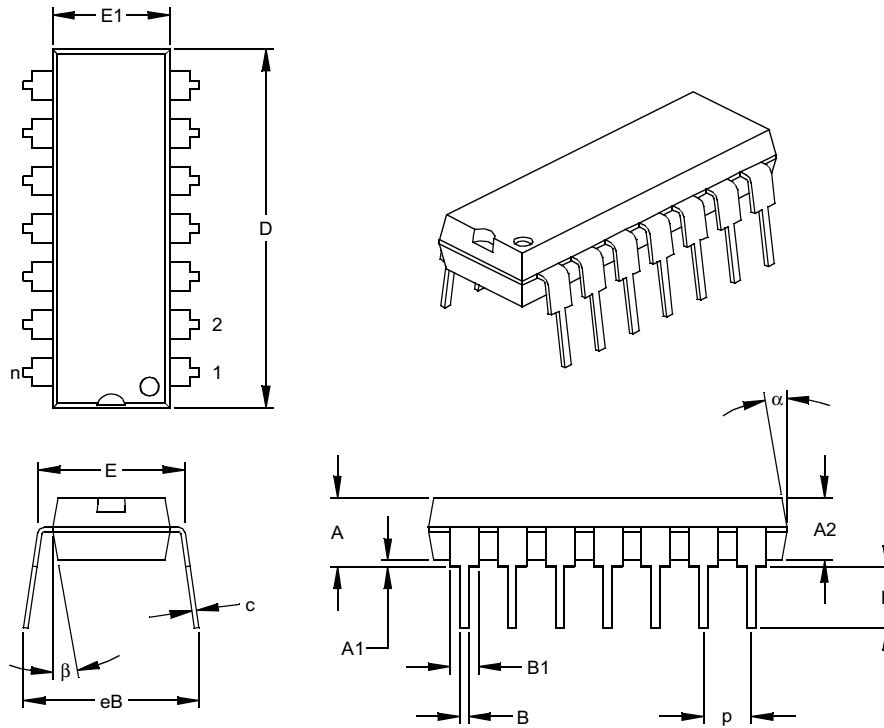
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

JEDEC Equivalent: MO-153

Drawing No. C04-086

MCP606/607/608/609

14-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.740	.750	.760	18.80	19.05	19.30
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter

§ Significant Characteristic

Notes:

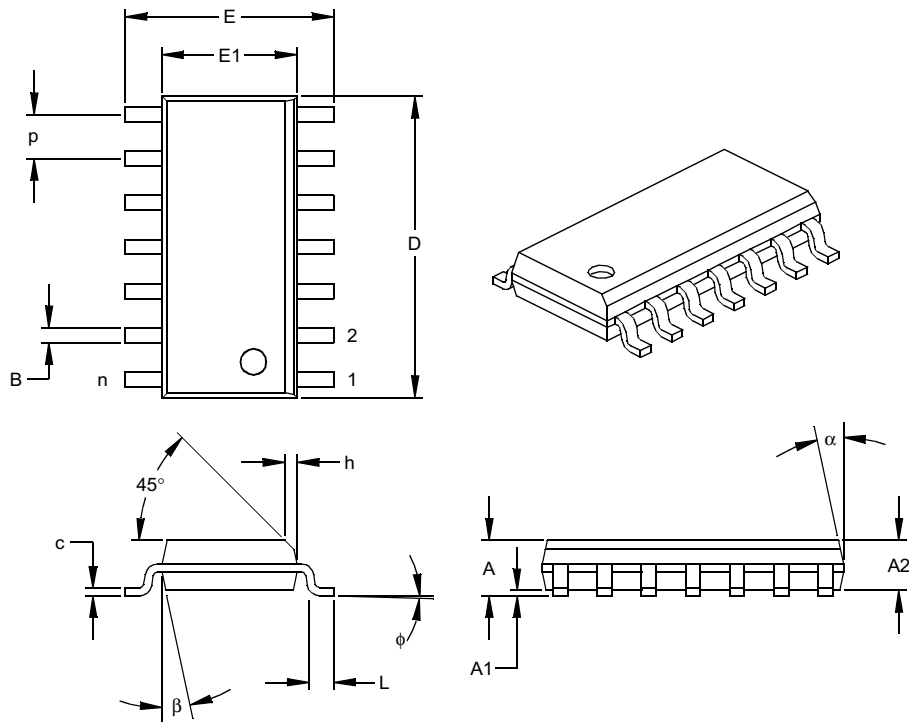
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-001

Drawing No. C04-005

MCP606/607/608/609

14-Lead Plastic Small Outline (SL) – Narrow, 150 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.81
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter

§ Significant Characteristic

Notes:

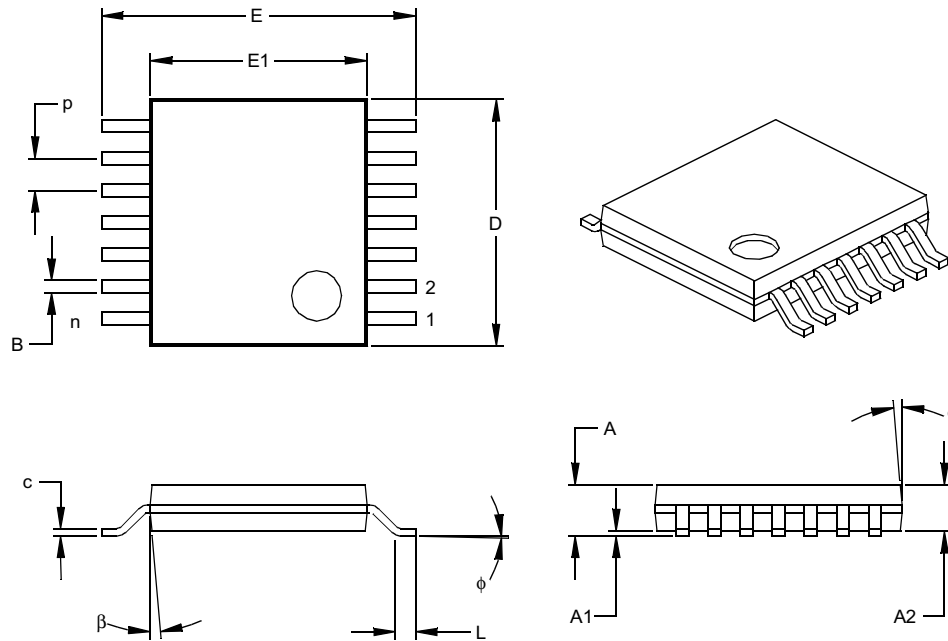
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-012

Drawing No. C04-065

MCP606/607/608/609

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B1	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

JEDEC Equivalent: MO-153

Drawing No. C04-087

MCP606/607/608/609

NOTES:

ON-LINE SUPPORT

Microchip provides on-line support on the Microchip World Wide Web (WWW) site.

The web site is used by Microchip as a means to make files and information easily available to customers. To view the site, the user must have access to the Internet and a web browser, such as Netscape or Microsoft Explorer. Files are also available for FTP download from our FTP site.

Connecting to the Microchip Internet Web Site

The Microchip web site is available by using your favorite Internet browser to attach to:

www.microchip.com

The file transfer site is available by using an FTP service to connect to:

<ftp://ftp.microchip.com>

The web site and file transfer site provide a variety of services. Users may download files for the latest Development Tools, Data Sheets, Application Notes, User's Guides, Articles and Sample Programs. A variety of Microchip specific business information is also available, including listings of Microchip sales offices, distributors and factory representatives. Other data available for consideration is:

- Latest Microchip Press Releases
- Technical Support Section with Frequently Asked Questions
- Design Tips
- Device Errata
- Job Postings
- Microchip Consultant Program Member Listing
- Links to other useful web sites related to Microchip Products
- Conferences for products, Development Systems, technical information and more
- Listing of seminars and events

Systems Information and Upgrade Hot Line

The Systems Information and Upgrade Line provides system users a listing of the latest versions of all of Microchip's development systems software products. Plus, this line provides information on how customers can receive any currently available upgrade kits. The Hot Line Numbers are:

1-800-755-2345 for U.S. and most of Canada, and

1-480-792-7302 for the rest of the world.

013001

MCP606/607/608/609

READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this Data Sheet.

To: Technical Publications Manager
RE: Reader Response
From: Name _____
Company _____
Address _____
City / State / ZIP / Country _____
Telephone: (_____) _____ - _____ FAX: (_____) _____ - _____

Application (optional):

Would you like a reply? ____Y ____N

Device: **MCP606/607/608/609** Literature Number: **DS11177C**

Questions:

1. What are the best features of this document?

2. How does this document meet your hardware and software development needs?

3. Do you find the organization of this data sheet easy to follow? If not, why?

4. What additions to the data sheet do you think would enhance the structure and subject?

5. What deletions from the data sheet could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?

8. How would you improve our software, systems, and silicon products?

NOTES:

MCP606/607/608/609

NOTES:

NOTES:

MCP606/607/608/609

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>/XX</u>									
Device	Temperature Range	Package									
<table><tr><td>Device</td><td>MCP606 = Single Operational Amplifier MCP606T = Single Operational Amplifier (Tape and Reel-SOIC/TSSOP) MCP607 = Dual Operational Amplifier MCP607T = Dual Operational Amplifier (Tape and Reel-SOIC/TSSOP) MCP608 = Single Operational Amplifier w/<u>CS</u> Function MCP608T = Single Operational Amplifier w/<u>CS</u> Function (Tape and Reel-SOIC/TSSOP) MCP609 = Quad Operational Amplifier MCP609T = Quad Operational Amplifier (Tape and Reel-SOIC/TSSOP)</td><td></td></tr><tr><td>Temperature Range</td><td>I = -40°C to +85°C</td><td></td></tr><tr><td>Package</td><td>P = Plastic DIP (300 mil Body), 8-lead & 14-lead SN = Plastic SOIC (150 mil Body), 8-lead SL = Plastic SOIC (150 mil Body), 14-lead ST = Plastic TSSOP, 8-lead & 14-lead OT = Plastic SOT-23, 5-lead</td><td></td></tr></table>			Device	MCP606 = Single Operational Amplifier MCP606T = Single Operational Amplifier (Tape and Reel-SOIC/TSSOP) MCP607 = Dual Operational Amplifier MCP607T = Dual Operational Amplifier (Tape and Reel-SOIC/TSSOP) MCP608 = Single Operational Amplifier w/ <u>CS</u> Function MCP608T = Single Operational Amplifier w/ <u>CS</u> Function (Tape and Reel-SOIC/TSSOP) MCP609 = Quad Operational Amplifier MCP609T = Quad Operational Amplifier (Tape and Reel-SOIC/TSSOP)		Temperature Range	I = -40°C to +85°C		Package	P = Plastic DIP (300 mil Body), 8-lead & 14-lead SN = Plastic SOIC (150 mil Body), 8-lead SL = Plastic SOIC (150 mil Body), 14-lead ST = Plastic TSSOP, 8-lead & 14-lead OT = Plastic SOT-23, 5-lead	
Device	MCP606 = Single Operational Amplifier MCP606T = Single Operational Amplifier (Tape and Reel-SOIC/TSSOP) MCP607 = Dual Operational Amplifier MCP607T = Dual Operational Amplifier (Tape and Reel-SOIC/TSSOP) MCP608 = Single Operational Amplifier w/ <u>CS</u> Function MCP608T = Single Operational Amplifier w/ <u>CS</u> Function (Tape and Reel-SOIC/TSSOP) MCP609 = Quad Operational Amplifier MCP609T = Quad Operational Amplifier (Tape and Reel-SOIC/TSSOP)										
Temperature Range	I = -40°C to +85°C										
Package	P = Plastic DIP (300 mil Body), 8-lead & 14-lead SN = Plastic SOIC (150 mil Body), 8-lead SL = Plastic SOIC (150 mil Body), 14-lead ST = Plastic TSSOP, 8-lead & 14-lead OT = Plastic SOT-23, 5-lead										

Examples:

- a) MCP606-I/P Industrial Temp., PDIP package
- b) MCP606T-I/P Tape and Reel, Industrial Temp., PDIP package
- c) MCP606-I/SN Industrial Temp., SOIC package
- d) MCP606T-I/SN Tape and Reel, Industrial Temp., SOIC package
- e) MCP606-I/ST Industrial Temp., TSSOP package
- f) MCP606T-I/ST Tape and Reel, Industrial Temp., TSSOP package
- g) MCP606-I/OT Industrial Temp., SOT-23 package
- h) MCP606T-I/OT Tape and Reel, Industrial Temp., SOT-23 package
- i) MCP607-I/P Industrial Temp., PDIP package
- j) MCP607T-I/P Industrial Temp., PDIP package
- k) MCP608-I/SN Industrial Temp., SOIC package
- l) MCP608T-I/SN Tape and Reel, Industrial Temp., SOIC package
- m) MCP609-I/P Industrial Temp., PDIP package
- n) MCP609T-I/P Industrial Temp., PDIP package

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

New Customer Notification System

Register on our web site (www.microchip.com/cn) to receive the most current information on our products.

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, PIC, PICmicro, PICMASTER, PICSTART, PRO MATE, KEELoQ, SEEVAL, MPLAB and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

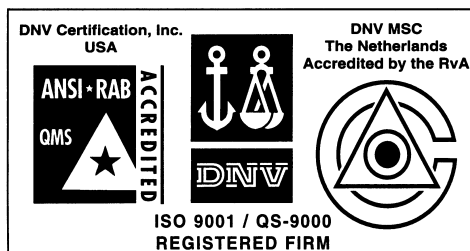
Total Endurance, ICSP, In-Circuit Serial Programming, Filter-Lab, MXDEV, microID, *FlexROM*, *fuzzyLAB*, MPASM, MPLINK, MPLIB, PICC, PICDEM, PICDEM.net, ICEPIC, Migratable Memory, FanSense, ECONOMONITOR, Select Mode and microPort are trademarks of Microchip Technology Incorporated in the U.S.A.

Serialized Quick Term Programming (SQTP) is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2001, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.



Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELoQ® code hopping devices, Serial EEPROMs and microperipheral products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.



WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200 Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: <http://www.microchip.com>

Rocky Mountain

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966 Fax: 480-792-7456

Atlanta

500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770-640-0034 Fax: 770-640-0307

Austin - Analog

8303 MoPac Expressway North
Suite A-201
Austin, TX 78759
Tel: 512-345-2030 Fax: 512-345-6085

Boston

2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848 Fax: 978-692-3821

Boston - Analog

Unit A-8-1 Millbrook Tarry Condominium
97 Lowell Road
Concord, MA 01742
Tel: 978-371-6400 Fax: 978-371-0050

Chicago

333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas

4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423 Fax: 972-818-2924

Dayton

Two Prestige Place, Suite 130
Miamisburg, OH 45342
Tel: 937-291-1654 Fax: 937-291-9175

Detroit

Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

Los Angeles

18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

New York

150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose

Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto

6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Australia

Microchip Technology Australia Pty Ltd
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing

Microchip Technology Consulting (Shanghai)
Co., Ltd., Beijing Liaison Office
Unit 915
New China Hong Kong Manhattan Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Chengdu

Microchip Technology Consulting (Shanghai)
Co., Ltd., Chengdu Liaison Office
Rm. 2401, Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-6766200 Fax: 86-28-6766599

China - Fuzhou

Microchip Technology Consulting (Shanghai)
Co., Ltd., Fuzhou Liaison Office
Rm. 531, North Building
Fujian Foreign Trade Center Hotel
73 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7557563 Fax: 86-591-7557572

China - Shanghai

Microchip Technology Consulting (Shanghai)
Co., Ltd.
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

China - Shenzhen

Microchip Technology Consulting (Shanghai)
Co., Ltd., Shenzhen Liaison Office
Rm. 1315, 13/F, Shenzhen Kerry Centre,
Renminnan Lu
Shenzhen 518001, China
Tel: 86-755-2350361 Fax: 86-755-2366086

Hong Kong

Microchip Technology Hongkong Ltd.
Unit 901, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

India

Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaughnessy Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan

Microchip Technology Japan K.K.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471-6166 Fax: 81-45-471-6122

Korea

Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Singapore

Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-334-8870 Fax: 65-334-8850

Taiwan

Microchip Technology Taiwan
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Denmark

Microchip Technology Denmark ApS
Regus Business Centre
Lautrup høj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France

Arizona Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - 1er Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany

Arizona Microchip Technology GmbH
Gustav-Heinemann Ring 125
D-81739 Munich, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Germany - Analog

Lochamer Strasse 13
D-82152 Martinsried, Germany
Tel: 49-89-895650-0 Fax: 49-89-895650-22

Italy

Arizona Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom

Arizona Microchip Technology Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

06/01/01