



STB12NK80Z, STF12NK80Z, STP12NK80Z, STW12NK80Z

N-channel 800 V, 0.65Ω typ., 10.5 A Zener-protected SuperMESH™
Power MOSFET in D²PAK, TO-220FP, TO-220 and TO-247

Datasheet — production data

Features

Type	V _{DSS} (@ T _{jmax})	R _{DS(on)}	I _D	P _W
STB12NK80Z	800V	<0.75Ω	10.5 A	190W
STF12NK80Z	800V	<0.75Ω	10.5 A	40W
STP12NK80Z	800V	<0.75Ω	10.5 A	190W
STW12NK80Z	800V	<0.75Ω	10.5 A	190W

- Extremely high dv/dt capability
- Improved esd capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing reliability

Applications

- Switching applications

Description

These devices are N-channel Zener-protected Power MOSFETs developed using STMicroelectronics' SuperMESH™ technology, achieved through optimization of ST's well established strip-based PowerMESH™ layout. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

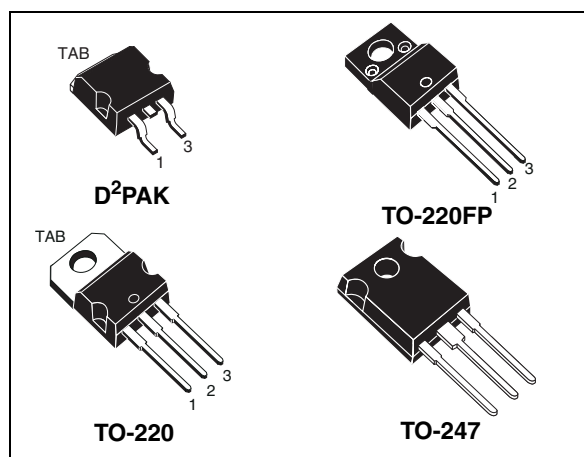


Figure 1. Internal schematic diagram

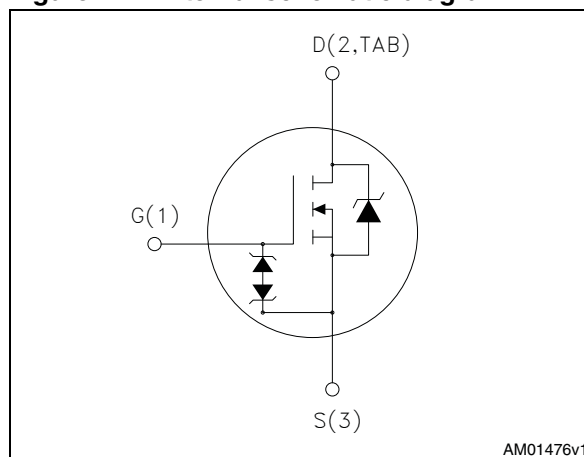


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB12NK80Z	12NK80Z	D ² PAK	Tape and reel
STF12NK80Z	12NK80Z	TO-220FP	Tube
STP12NK80Z	12NK80Z	TO-220	Tube
STW12NK80Z	12NK80Z	TO-247	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D ² PAK TO-220 TO-247	TO-220FP	
V _{DS}	Drain-source voltage (V _{GS} = 0)	800		V
V _{DGR}	Drain-gate voltage (R _{GS} = 20kΩ)	800		V
V _{GS}	Gate-source voltage	± 30		V
I _D	Drain current (continuous) at T _C = 25°C	10.5	10.5 ⁽¹⁾	A
I _D	Drain current (continuous) at T _C = 100°C	6.6	6.6 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	42	42 ⁽¹⁾	A
P _{TOT}	Total dissipation at T _C = 25°C	190	40	W
	Derating factor	1.52	0.32	W/°C
Vesd(G-S)	G-S ESD (HBM C= 100pF, R= 1.5kΩ)	4		kV
V _{ISO}	Insulation withstand voltage (DC)	--	2500	V
dv/dt ⁽³⁾	Peak diode recovery voltage slope	4.5		V
T _J T _{stg}	Operating junction temperature Storage temperature	-55 to 150		°C

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3. I_{SD} ≤ 10.5 A, di/dt ≤ 200A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		TO-220/ D ² PAK	TO-220FP	TO-247	
R _{thj-case}	Thermal resistance junction-case max	0.66	3.1	0.66	°C/W
R _{thj-a}	Thermal resistance junction-ambient max	62.5		50	°C/W

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	10.5	A
E_{AS}	Single pulse avalanche energy (starting Tj=25°C, Id=Iar, Vdd=50V)	400	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified).

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{mA}$, $V_{GS} = 0$	800			V
I_{DSS}	Peak diode recovery voltage slope	$V_{DS} = 800\text{V}$, $V_{DS} = 800\text{V}$, $T_C = 125^{\circ}\text{C}$			1 50	μA μA
I_{GSS}	Gate body leakage current ($V_{GS} = 0$)	$V_{GS} = \pm 20\text{V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{V}$, $I_D = 5.25\text{A}$		0.65	0.75	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{V}$, $I_D = 5.25\text{A}$	-	12	-	S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{V}$, $f = 1\text{MHz}$, $V_{GS} = 0$	-	2620 250 53	-	pF pF pF
$C_{osseq}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0$, $V_{DS} = 0\text{V}$ to 640V	-	100	-	pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 640\text{V}$, $I_D = 10.5\text{A}$ $V_{GS} = 10\text{V}$ (see Figure 21)	-	87 14 44	-	nC nC nC
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Off-voltage rise time Fall time	$V_{DD} = 400\text{V}$, $I_D = 5.25\text{A}$, $R_G = 4.7\Omega$, $V_{GS} = 10\text{V}$ (see Figure 22)	-	30 18 70 20	-	ns ns ns ns
$t_{r(Voff)}$ t_f t_c	Off voltage rise time Fall time Cross-over time	$V_{DD} = 640\text{V}$, $I_D = 10.5\text{A}$, $R_G = 4.7\Omega$, $V_{GS} = 10\text{V}$ (see Figure 22)	-	16 15 28	-	ns ns ns

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		10.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		42	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=10.5A$, $V_{GS}=0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD}=10.5A$,		635		ns
Q_{rr}	Reverse recovery charge	$di/dt = 100A/\mu s$,	-	5.9		μC
I_{RRM}	Reverse recovery current	$V_{DD}=100V$, $T_J=150^{\circ}C$		18.5		A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Table 8. Gate-source zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
BV_{GSO}	Gate-Source breakdown voltage	$I_{gs}=\pm 1mA$ (Open drain)	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220 and D²PAK

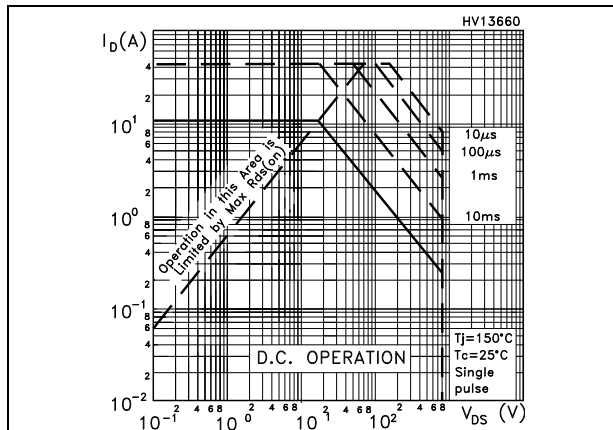


Figure 3. Thermal impedance for TO-220 and D²PAK

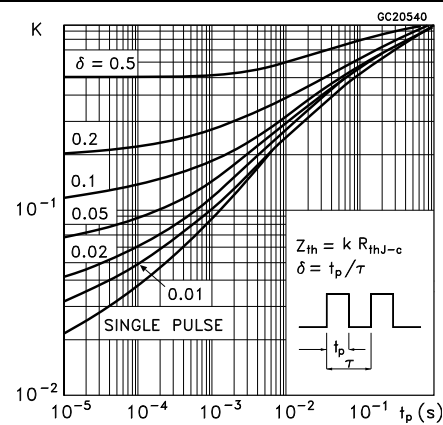


Figure 4. Safe operating area for TO-220FP

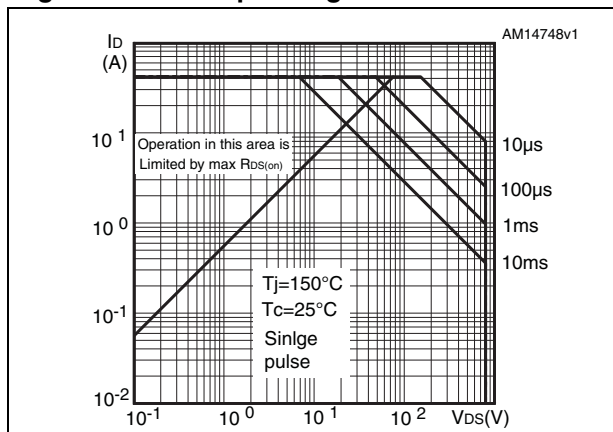


Figure 5. Thermal impedance for TO-220FP

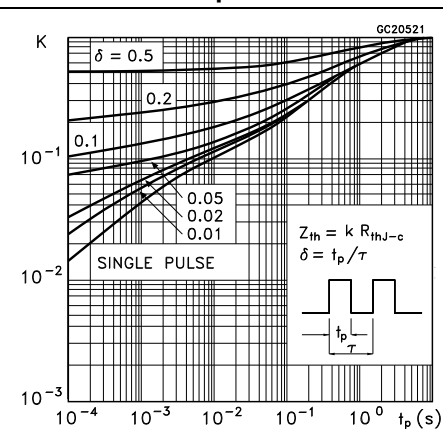


Figure 6. Safe operating area for TO-247

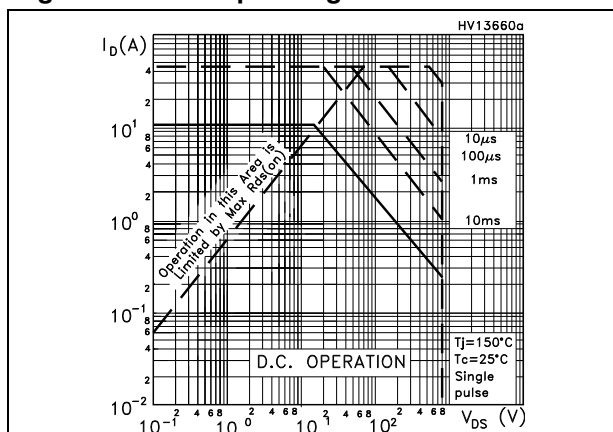


Figure 7. Thermal impedance for TO-247

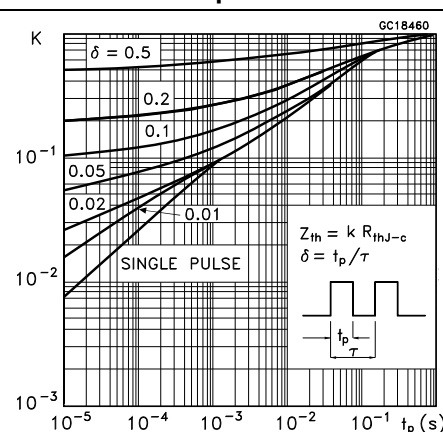


Figure 8. Output characteristics

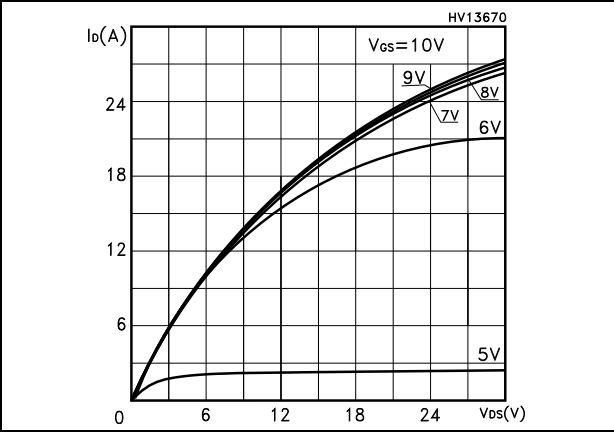


Figure 9. Transfer characteristics

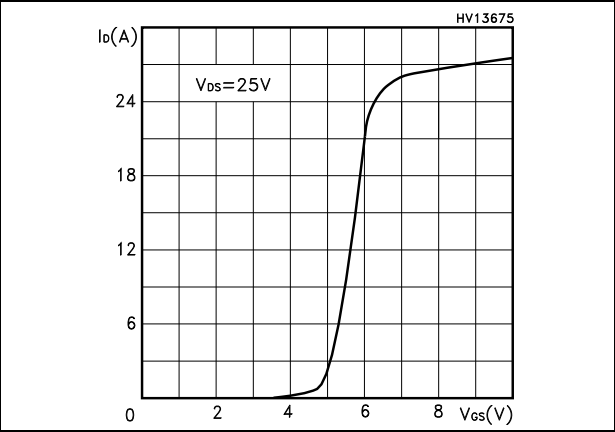


Figure 10. Transconductance

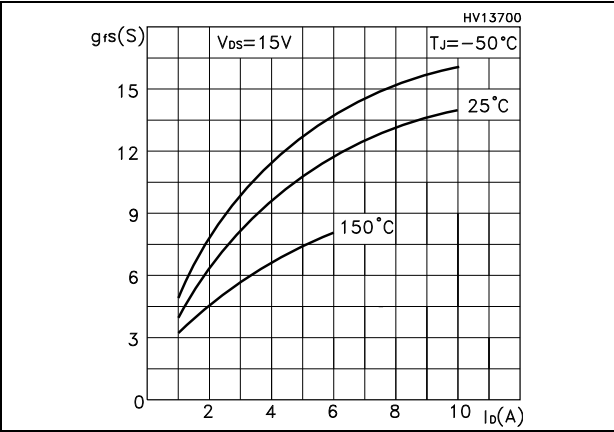


Figure 11. Static drain-source on-resistance

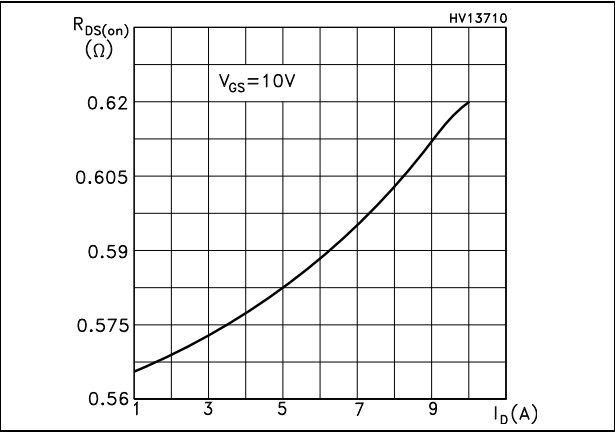


Figure 12. Gate charge vs gate-source voltage

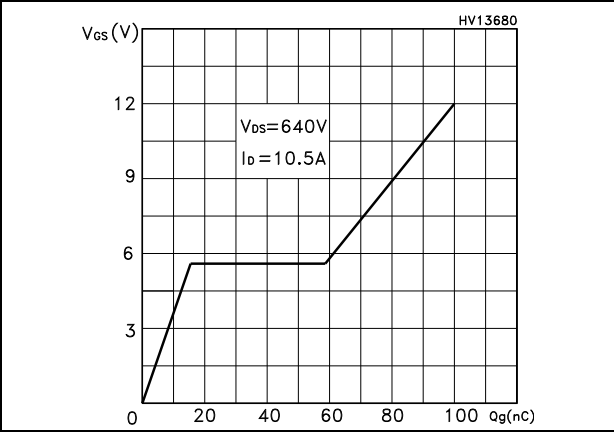


Figure 13. Capacitance variations

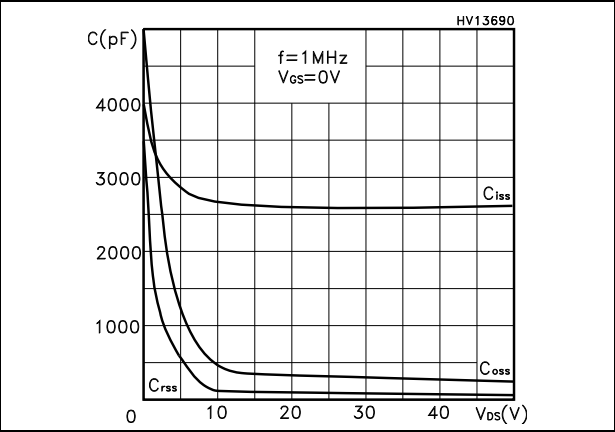


Figure 14. Normalized gate threshold voltage vs temperature

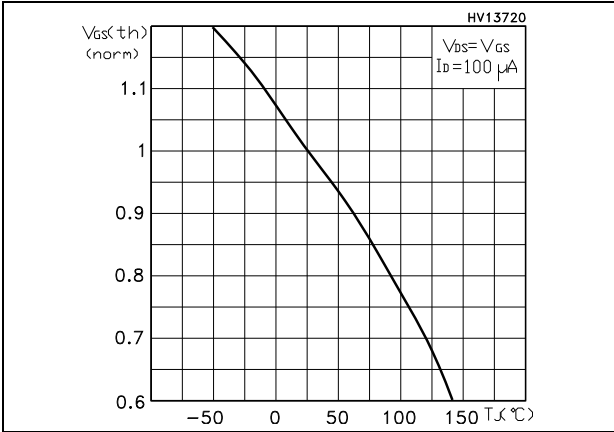


Figure 15. Normalized on-resistance vs temperature

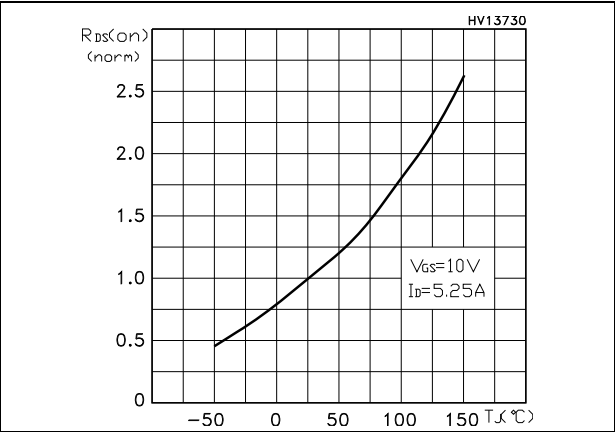


Figure 16. Source-drain diode forward characteristics

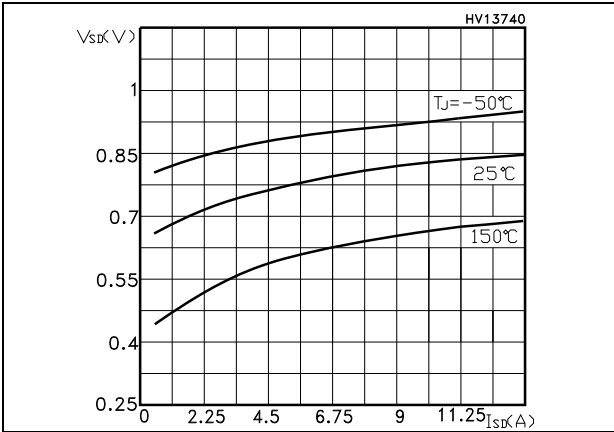


Figure 17. Normalized $B_{V_{DSS}}$ vs temperature

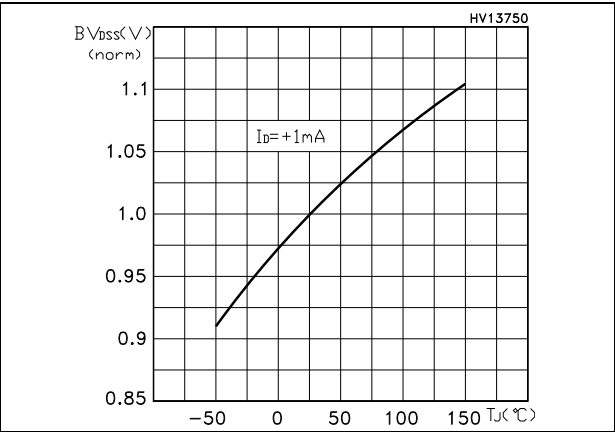
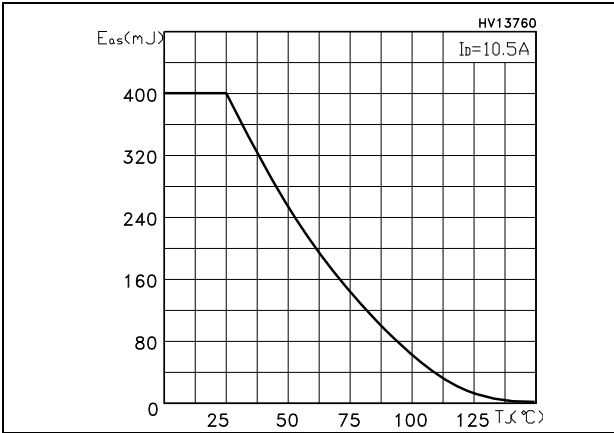


Figure 18. Maximum avalanche energy vs temperature



3 Test circuits

Figure 19. Switching times test circuit for resistive load

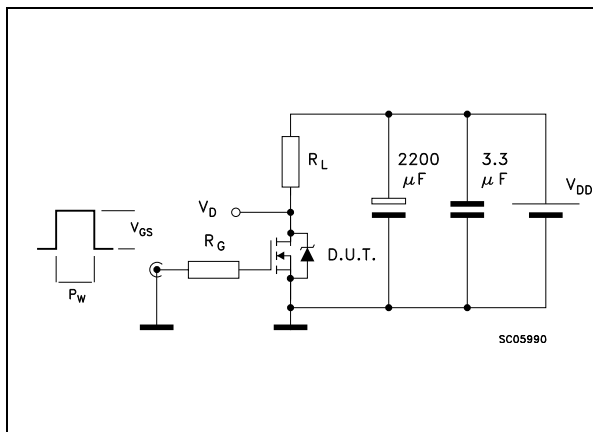


Figure 20. Gate charge test circuit

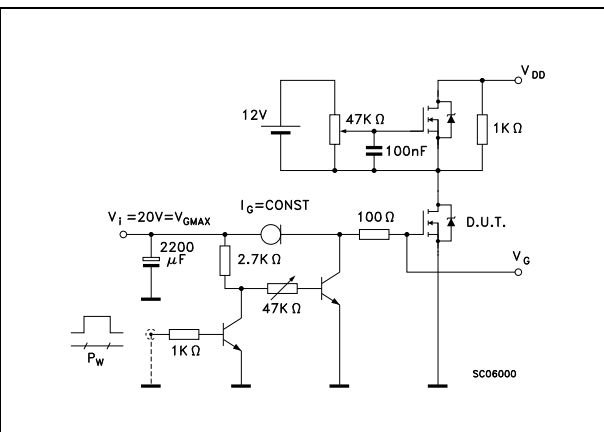


Figure 21. Test circuit for inductive load switching and diode recovery times

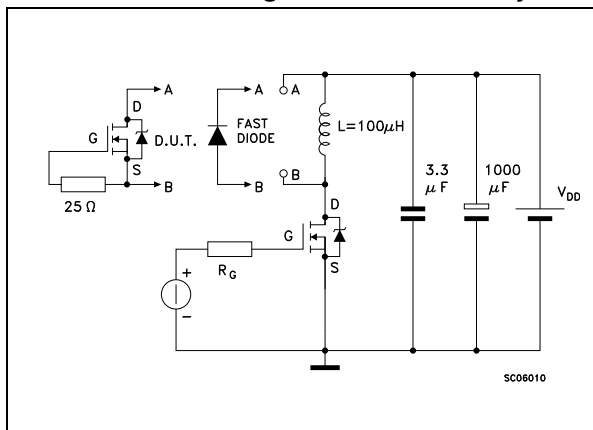


Figure 22. Unclamped Inductive load test circuit

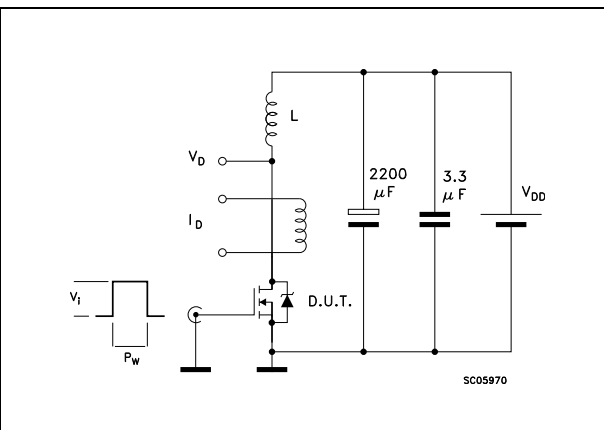
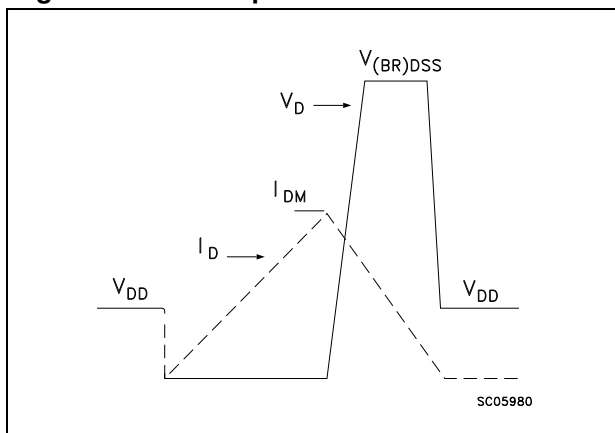


Figure 23. Unclamped inductive waveform

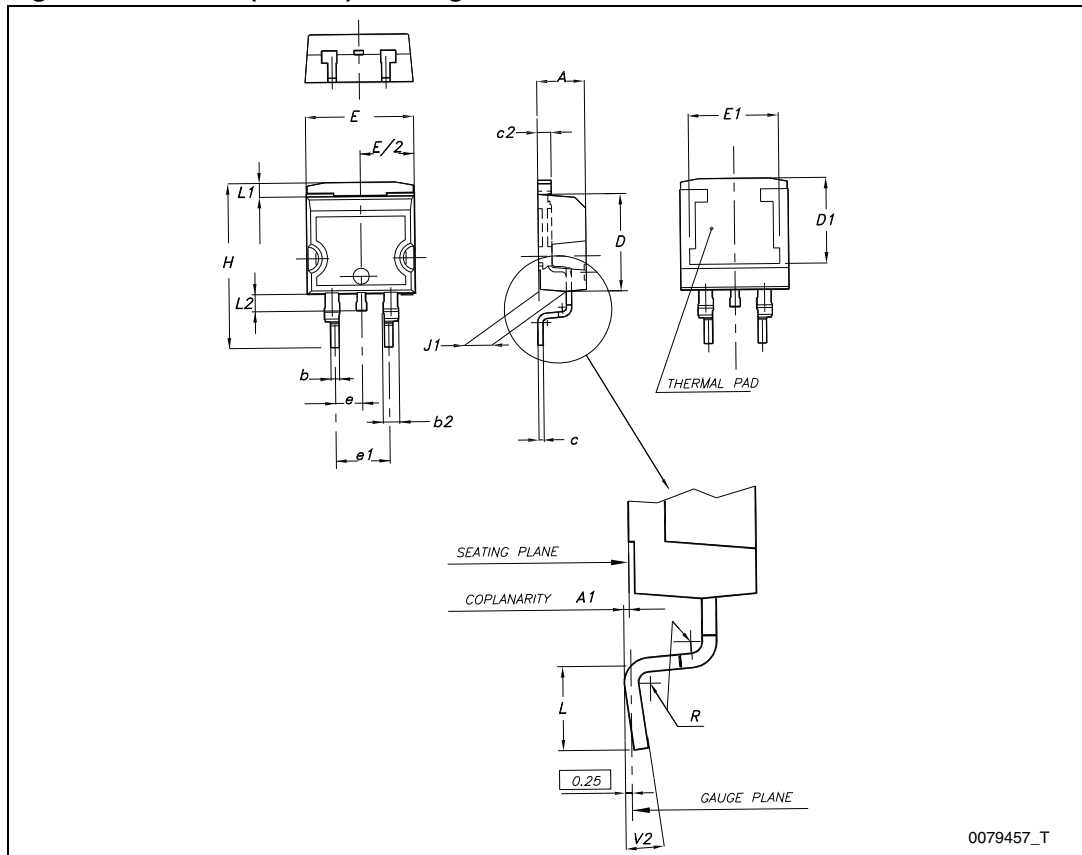
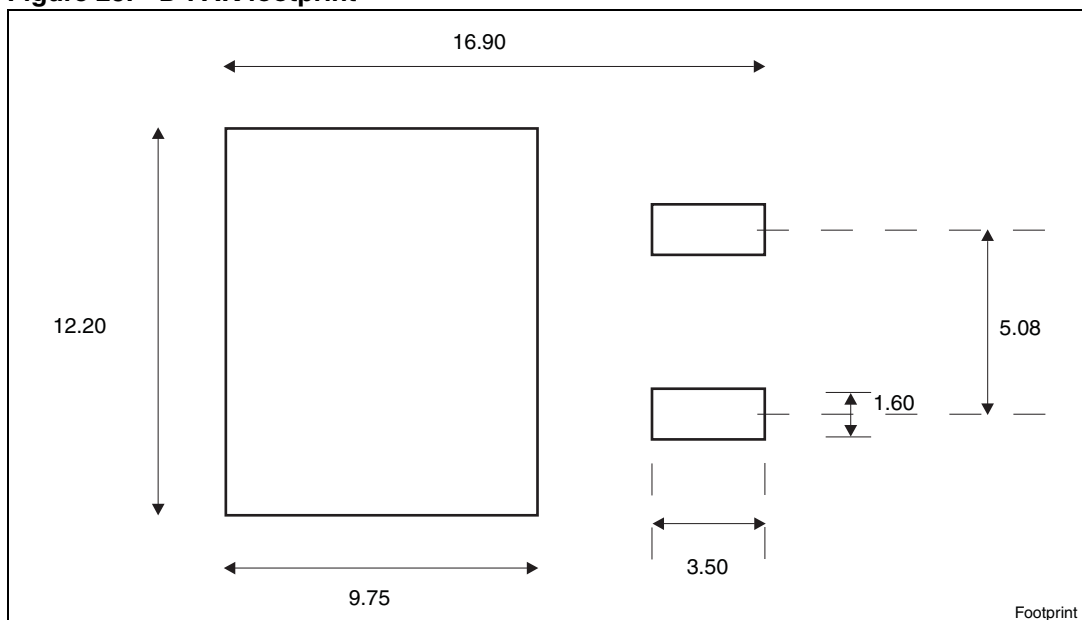


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. D²PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

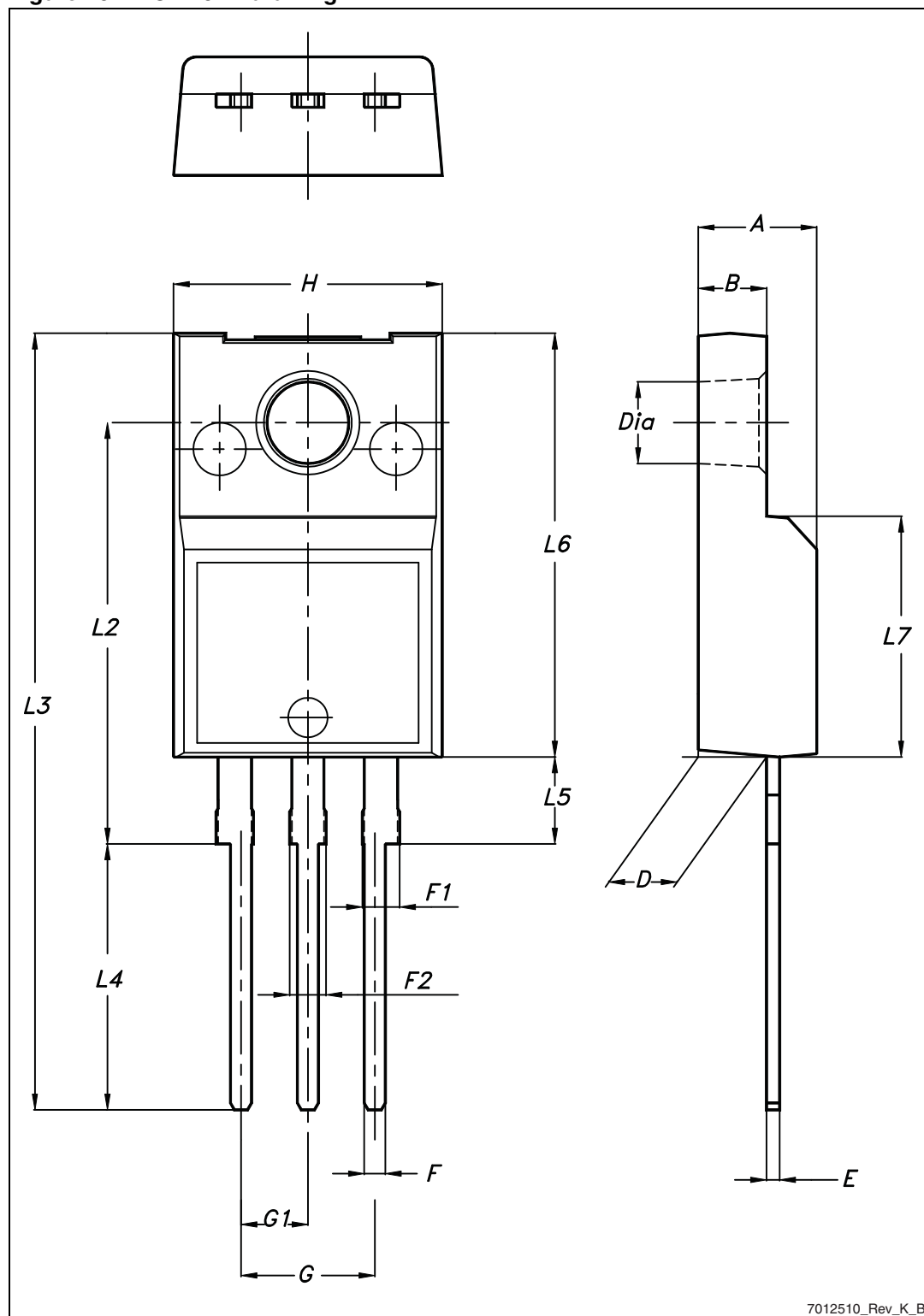
Figure 24. D²PAK (TO-263) drawingFigure 25. D²PAK footprint^(a)

a. All dimension are in millimeters

Table 10. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 26. TO-220FP drawing



7012510_Rev_K_B

Table 11. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 27. TO-220 type A drawing

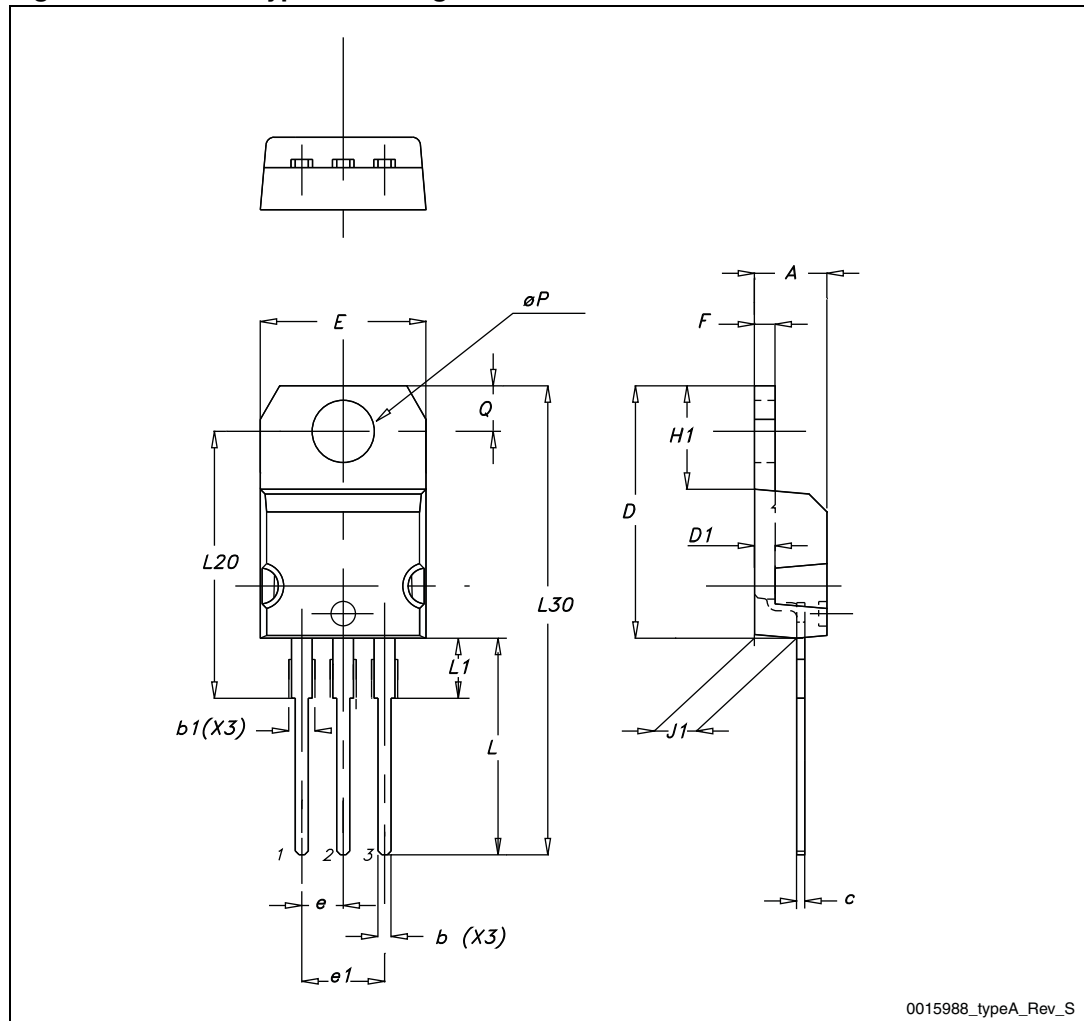
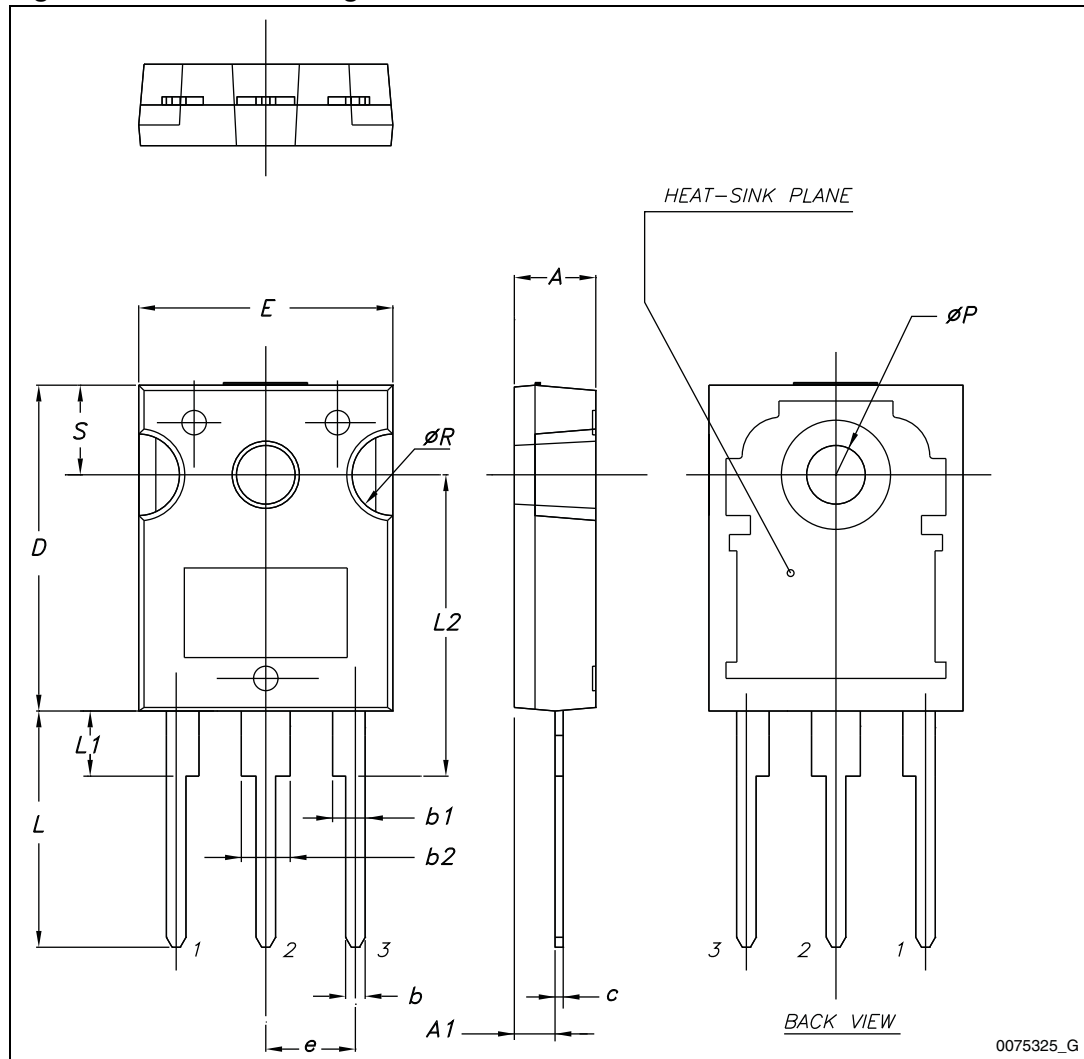


Table 12. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

Figure 28. TO-247 drawing



0075325_G

5 Packaging mechanical data

Table 13. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

REEL DIMENSIONS

40mm min.

Access hole

At slot location

A

B

C

D

E

F

G measured at hub

H

I

J

K

L

M

N

O

P

Q

R

S

T

Full radius

Tape slot in core for tape start 25 mm min. width

AM08851v2

6 Revision history

Table 14. Document revision history

Date	Revision	Changes
22-Jun-2004	2	Preliminary version.
28-Jan-2005	3	Complete version.
08-Sep-2005	4	Figure 2 and Figure 6 changed.
31-Jul-2006	5	The document has been reformatted.
27-Apr-2007	6	Modified $R_{DS(on)}$ value on Table 5 .
28-Aug-2012	7	Inserted new device in TO-220FP. Updated Table 1: Device summary , Table 2: Absolute maximum ratings and Table 3: Thermal data . Updated Section 4: Package mechanical data and Section 5: Packaging mechanical data . Minor text changes in the cover page.

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