HIGH-PRECISION VOLTAGE DETECTOR WITH A BUILT-IN DELAY CIRCUIT

S-801 Series

The S-801 Series is a high-precision voltage detector with a built-in delay time generater of fixed time developed using CMOS process. The detection voltage is fixed internally, with an accuracy of ±2.0%. Internal oscillator and counter timer can delay the release signal for a fixed time with no external attachment part. Three delay times, 50 ms typ., 100ms typ., or 200 ms typ. are available. Two output types, Nch open-drain and CMOS output, are available.

■ Features

- Ultra-low current consumption
  1.3 μA typ. (at V_{DD}=3.5 V)
- Hysteresis characteristics
  60 mV typ.
- Three delay times
  A series : 50 ms typ.
  B series : 100 ms typ.
  C series : 200 ms typ.
- High-precision detection voltage
  ±2.0%
- ON/OFF switch of delay time (DS pin)
- Operating voltage
  0.95 to 10.0 V
- Detection voltage
  2.2 to 6.0 V (0.1V step)
- Output
  Nch open-drain active low or CMOS active low output

■ Applications

- Power monitor for portable equipment such as note type personal computers, digital cameras, PDA devices, and portable phone.
- Constant voltage power monitor for cameras, video equipment and communication devices.
- Power monitor for microcomputers and reset for CPUs.

■ Package

5 pin, SOT-23-5 (See PKG code, MP005-A)

■ Block Diagram

(1) Nch open-drain active low output

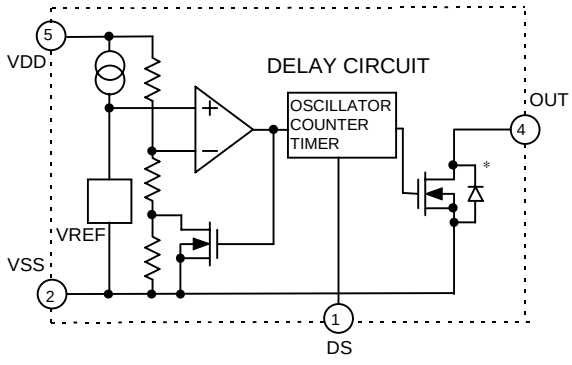


Figure 1 Block Diagram (Nch open-drain)

(2) CMOS active low output

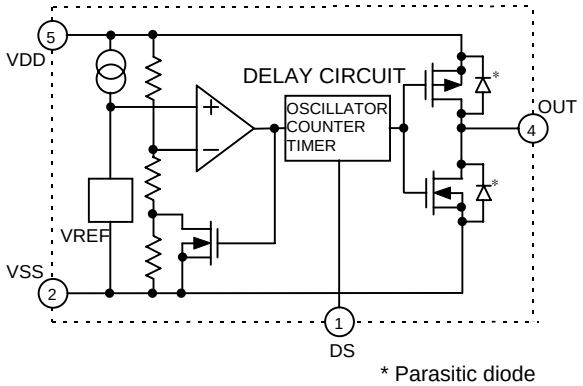


Figure 2 Block Diagram (CMOS)

■ Selection Guide

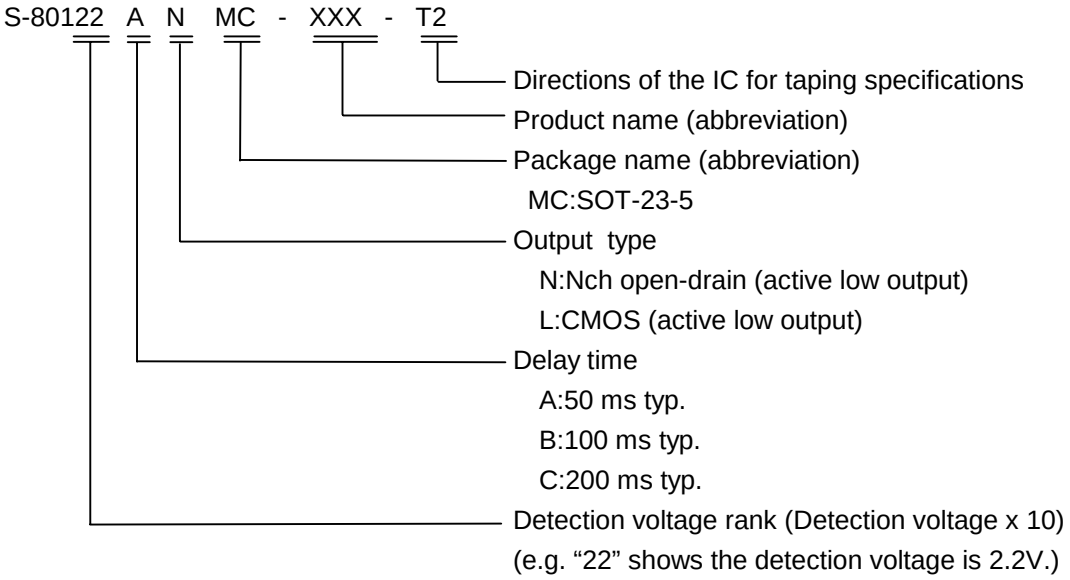


Table 1 Selection Guide

SII will develop products marked with mesh in order, contact sales personnel for a sample. (1/3)

Detection voltage range	Delay time	Nch Open-Drain (Low)	CMOS Output (Low)
2.2 V ± 2.0%	50 ms typ.	S-80122ANMC-JCH-T2	S-80122ALMC-JAH-T2
	100 ms typ.	S-80122BNMC-JGH-T2	S-80122BLMC-JEH-T2
	200 ms typ.	S-80122CNMC-JKH-T2	S-80122CLMC-JIH-T2
2.3 V ± 2.0%	50 ms typ.	S-80123ANMC-JCI-T2	S-80123ALMC-JAI-T2
	100 ms typ.	S-80123BNMC-JGI-T2	S-80123BLMC-JEI-T2
	200 ms typ.	S-80123CNMC-JKI-T2	S-80123CLMC-JII-T2
2.4 V ± 2.0%	50 ms typ.	S-80124ANMC-JCJ-T2	S-80124ALMC-JAJ-T2
	100 ms typ.	S-80124BNMC-JGJ-T2	S-80124BLMC-JEJ-T2
	200 ms typ.	S-80124CNMC-JKJ-T2	S-80124CLMC-JIJ-T2
2.5 V ± 2.0%	50 ms typ.	S-80125ANMC-JCK-T2	S-80125ALMC-JAK-T2
	100 ms typ.	S-80125BNMC-JGK-T2	S-80125BLMC-JEK-T2
	200 ms typ.	S-80125CNMC-JKK-T2	S-80125CLMC-JIK-T2
2.6 V ± 2.0%	50 ms typ.	S-80126ANMC-JCL-T2	S-80126ALMC-JAL-T2
	100 ms typ.	S-80126BNMC-JGL-T2	S-80126BLMC-JEL-T2
	200 ms typ.	S-80126CNMC-JKL-T2	S-80126CLMC-JIL-T2
2.7 V ± 2.0%	50 ms typ.	S-80127ANMC-JCM-T2	S-80127ALMC-JAM-T2
	100 ms typ.	S-80127BNMC-JGM-T2	S-80127BLMC-JEM-T2
	200 ms typ.	S-80127CNMC-JKM-T2	S-80127CLMC-JIM-T2
2.8 V ± 2.0%	50 ms typ.	S-80128ANMC-JCN-T2	S-80128ALMC-JAN-T2
	100 ms typ.	S-80128BNMC-JGN-T2	S-80128BLMC-JEN-T2
	200 ms typ.	S-80128CNMC-JKN-T2	S-80128CLMC-JIN-T2
2.9 V ± 2.0%	50 ms typ.	S-80129ANMC-JCO-T2	S-80129ALMC-JAO-T2
	100 ms typ.	S-80129BNMC-JGO-T2	S-80129BLMC-JEO-T2
	200 ms typ.	S-80129CNMC-JKO-T2	S-80129CLMC-JIO-T2
3.0 V ± 2.0%	50 ms typ.	S-80130ANMC-JCP-T2	S-80130ALMC-JAP-T2
	100 ms typ.	S-80130BNMC-JGP-T2	S-80130BLMC-JEP-T2
	200 ms typ.	S-80130CNMC-JKP-T2	S-80130CLMC-JIP-T2
3.1 V ± 2.0%	50 ms typ.	S-80131ANMC-JCQ-T2	S-80131ALMC-JAQ-T2
	100 ms typ.	S-80131BNMC-JGQ-T2	S-80131BLMC-JEQ-T2
	200 ms typ.	S-80131CNMC-JKQ-T2	S-80131CLMC-JIQ-T2

Table 1 Selection Guide

SII will develop products marked with mesh in order, contact sales personnel for a sample. (2/3)

Detection voltage range	Delay time	Nch Open-Drain (Low)	CMOS Output (Low)
3.2 V ± 2.0%	50 ms typ.	S-80132ANMC-JCR-T2	S-80132ALMC-JAR-T2
	100 ms typ.	S-80132BNMC-JGR-T2	S-80132BLMC-JER-T2
	200 ms typ.	S-80132CNMC-JKR-T2	S-80132CLMC-JIR-T2
3.3 V ± 2.0%	50 ms typ.	S-80133ANMC-JCS-T2	S-80133ALMC-JAS-T2
	100 ms typ.	S-80133BNMC-JGS-T2	S-80133BLMC-JES-T2
	200 ms typ.	S-80133CNMC-JKS-T2	S-80133CLMC-JIS-T2
3.4 V ± 2.0%	50 ms typ.	S-80134ANMC-JCT-T2	S-80134ALMC-JAT-T2
	100 ms typ.	S-80134BNMC-JGT-T2	S-80134BLMC-JET-T2
	200 ms typ.	S-80134CNMC-JKT-T2	S-80134CLMC-JIT-T2
3.5 V ± 2.0%	50 ms typ.	S-80135ANMC-JCU-T2	S-80135ALMC-JAU-T2
	100 ms typ.	S-80135BNMC-JGU-T2	S-80135BLMC-JEU-T2
	200 ms typ.	S-80135CNMC-JKU-T2	S-80135CLMC-JIU-T2
3.6 V ± 2.0%	50 ms typ.	S-80136ANMC-JCV-T2	S-80136ALMC-JAV-T2
	100 ms typ.	S-80136BNMC-JGV-T2	S-80136BLMC-JEV-T2
	200 ms typ.	S-80136CNMC-JKV-T2	S-80136CLMC-JIV-T2
3.7 V ± 2.0%	50 ms typ.	S-80137ANMC-JCW-T2	S-80137ALMC-JAW-T2
	100 ms typ.	S-80137BNMC-JGW-T2	S-80137BLMC-JEW-T2
	200 ms typ.	S-80137CNMC-JKW-T2	S-80137CLMC-JIW-T2
3.8 V ± 2.0%	50 ms typ.	S-80138ANMC-JCX-T2	S-80138ALMC-JAX-T2
	100 ms typ.	S-80138BNMC-JGX-T2	S-80138BLMC-JEX-T2
	200 ms typ.	S-80138CNMC-JKX-T2	S-80138CLMC-JIX-T2
3.9 V ± 2.0%	50 ms typ.	S-80139ANMC-JCY-T2	S-80139ALMC-JAY-T2
	100 ms typ.	S-80139BNMC-JGY-T2	S-80139BLMC-JEY-T2
	200 ms typ.	S-80139CNMC-JKY-T2	S-80139CLMC-JIY-T2
4.0 V ± 2.0%	50 ms typ.	S-80140ANMC-JCZ-T2	S-80140ALMC-JAZ-T2
	100 ms typ.	S-80140BNMC-JGZ-T2	S-80140BLMC-JEZ-T2
	200 ms typ.	S-80140CNMC-JKZ-T2	S-80140CLMC-JIZ-T2
4.1 V ± 2.0%	50 ms typ.	S-80141ANMC-JC2-T2	S-80141ALMC-JA2-T2
	100 ms typ.	S-80141BNMC-JG2-T2	S-80141BLMC-JE2-T2
	200 ms typ.	S-80141CNMC-JK2-T2	S-80141CLMC-JI2-T2
4.2 V ± 2.0%	50 ms typ.	S-80142ANMC-JC3-T2	S-80142ALMC-JA3-T2
	100 ms typ.	S-80142BNMC-JG3-T2	S-80142BLMC-JE3-T2
	200 ms typ.	S-80142CNMC-JK3-T2	S-80142CLMC-JI3-T2
4.3 V ± 2.0%	50 ms typ.	S-80143ANMC-JC4-T2	S-80143ALMC-JA4-T2
	100 ms typ.	S-80143BNMC-JG4-T2	S-80143BLMC-JE4-T2
	200 ms typ.	S-80143CNMC-JK4-T2	S-80143CLMC-JI4-T2
4.4 V ± 2.0%	50 ms typ.	S-80144ANMC-JC5-T2	S-80144ALMC-JA5-T2
	100 ms typ.	S-80144BNMC-JG5-T2	S-80144BLMC-JE5-T2
	200 ms typ.	S-80144CNMC-JK5-T2	S-80144CLMC-JI5-T2
4.5 V ± 2.0%	50 ms typ.	S-80145ANMC-JC6-T2	S-80145ALMC-JA6-T2
	100 ms typ.	S-80145BNMC-JG6-T2	S-80145BLMC-JE6-T2
	200 ms typ.	S-80145CNMC-JK6-T2	S-80145CLMC-JI6-T2
4.6 V ± 2.0%	50 ms typ.	S-80146ANMC-JC7-T2	S-80146ALMC-JA7-T2
	100 ms typ.	S-80146BNMC-JG7-T2	S-80146BLMC-JE7-T2
	200 ms typ.	S-80146CNMC-JK7-T2	S-80146CLMC-JI7-T2
4.7 V ± 2.0%	50 ms typ.	S-80147ANMC-JC8-T2	S-80147ALMC-JA8-T2
	100 ms typ.	S-80147BNMC-JG8-T2	S-80147BLMC-JE8-T2
	200 ms typ.	S-80147CNMC-JK8-T2	S-80147CLMC-JI8-T2
4.8 V ± 2.0%	50 ms typ.	S-80148ANMC-JC9-T2	S-80148ALMC-JA9-T2
	100 ms typ.	S-80148BNMC-JG9-T2	S-80148BLMC-JE9-T2
	200 ms typ.	S-80148CNMC-JK9-T2	S-80148CLMC-JI9-T2

Table 1 Selection Guide

SII will develop products marked with mesh in order, contact sales personnel for a sample. (3/3)

Detection voltage range	Delay time	Nch Open-Drain (Low)	CMOS Output (Low)
4.9 V ± 2.0%	50 ms typ.	S-80149ANMC-JDA-T2	S-80149ALMC-JBA-T2
	100 ms typ.	S-80149BNMC-JHA-T2	S-80149BLMC-JFA-T2
	200 ms typ.	S-80149CNMC-JLA-T2	S-80149CLMC-JJA-T2
5.0 V ± 2.0%	50 ms typ.	S-80150ANMC-JDB-T2	S-80150ALMC-JBB-T2
	100 ms typ.	S-80150BNMC-JHB-T2	S-80150BLMC-JFB-T2
	200 ms typ.	S-80150CNMC-JLB-T2	S-80150CLMC-JJB-T2
5.1 V ± 2.0%	50 ms typ.	S-80151ANMC-JDC-T2	S-80151ALMC-JBC-T2
	100 ms typ.	S-80151BNMC-JHC-T2	S-80151BLMC-JFC-T2
	200 ms typ.	S-80151CNMC-JLC-T2	S-80151CLMC-JJC-T2
5.2 V ± 2.0%	50 ms typ.	S-80152ANMC-JDD-T2	S-80152ALMC-JBD-T2
	100 ms typ.	S-80152BNMC-JHD-T2	S-80152BLMC-JFD-T2
	200 ms typ.	S-80152CNMC-JLD-T2	S-80152CLMC-JJD-T2
5.3 V ± 2.0%	50 ms typ.	S-80153ANMC-JDE-T2	S-80153ALMC-JBE-T2
	100 ms typ.	S-80153BNMC-JHE-T2	S-80153BLMC-JFE-T2
	200 ms typ.	S-80153CNMC-JLE-T2	S-80153CLMC-JJE-T2
5.4 V ± 2.0%	50 ms typ.	S-80154ANMC-JDF-T2	S-80154ALMC-JBF-T2
	100 ms typ.	S-80154BNMC-JHF-T2	S-80154BLMC-JFF-T2
	200 ms typ.	S-80154CNMC-JLF-T2	S-80154CLMC-JJF-T2
5.5 V ± 2.0%	50 ms typ.	S-80155ANMC-JDG-T2	S-80155ALMC-JBG-T2
	100 ms typ.	S-80155BNMC-JHG-T2	S-80155BLMC-JFG-T2
	200 ms typ.	S-80155CNMC-JLG-T2	S-80155CLMC-JJG-T2
5.6 V ± 2.0%	50 ms typ.	S-80156ANMC-JDH-T2	S-80156ALMC-JBH-T2
	100 ms typ.	S-80156BNMC-JHH-T2	S-80156BLMC-JFH-T2
	200 ms typ.	S-80156CNMC-JLH-T2	S-80156CLMC-JJH-T2
5.7 V ± 2.0%	50 ms typ.	S-80157ANMC-JDI-T2	S-80157ALMC-JBI-T2
	100 ms typ.	S-80157BNMC-JHI-T2	S-80157BLMC-JFI-T2
	200 ms typ.	S-80157CNMC-JLI-T2	S-80157CLMC-JJI-T2
5.8 V ± 2.0%	50 ms typ.	S-80158ANMC-JDJ-T2	S-80158ALMC-JBJ-T2
	100 ms typ.	S-80158BNMC-JHJ-T2	S-80158BLMC-JFJ-T2
	200 ms typ.	S-80158CNMC-JLJ-T2	S-80158CLMC-JJJ-T2
5.9 V ± 2.0%	50 ms typ.	S-80159ANMC-JDK-T2	S-80159ALMC-JBK-T2
	100 ms typ.	S-80159BNMC-JHK-T2	S-80159BLMC-JFK-T2
	200 ms typ.	S-80159CNMC-JLK-T2	S-80159CLMC-JJK-T2
6.0 V ± 2.0%	50 ms typ.	S-80160ANMC-JDL-T2	S-80160ALMC-JBL-T2
	100 ms typ.	S-80160BNMC-JHL-T2	S-80160BLMC-JFL-T2
	200 ms typ.	S-80160CNMC-JLL-T2	S-80160CLMC-JJL-T2

■ Pin Configuration

See the end of the book for details of the package.

SOT-23-5
Top view

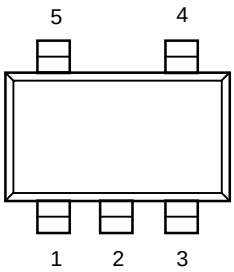


Figure 3 Pin Configuration

Table 2 Pin Description

No.	Symbol	Description
1	DS (*1)	ON/OFF switch of delay time pin
2	VSS	Ground pin
3	NC (*2)	non-connection
4	OUT	Voltage detection output pin
5	VDD	Voltage input pin

(*1) See “2 Delay Circuit (Page 10)” for operation.
(*2) NC means open electrically.
Connecting pin No.3 to VDD or VSS has no problem.

■ Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings

(Unless otherwise specified: Ta=25°C)

Parameter		Symbol	Ratings	Units
Power supply voltage		$V_{DD}-V_{SS}$	12	V
Output voltage	Nch open-drain	V_{OUT}	V_{SS}-0.3 to 12	V
	CMOS		V_{SS}-0.3 to V_{DD}+0.3	V
Output current		I_{OUT}	50	mA
Power dissipation		P_d	150	mW
Operating temperature		T_{opr}	−40 to +85	°C
Storage temperature		T_{stg}	−40 to +125	°C

Note: This IC has a built-in protection circuit for static electricity, however, prevent contact with a large static electricity or electrostatic voltage which exceeds the performance of the protection circuit.

■ Electrical Characteristics

Table 4 Erectrical Characteristics

(Unless otherwise specified: Ta=25 °C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units	Test circuit
Detection voltage	$-V_{DET}$	—		$-V_{DET}\times 0.98$	$-V_{DET}$	$-V_{DET}\times 1.02$	V	1
Hysteresis width	V_{HYS}	—		30	60	100	mV	1
Operating voltage	V_{DD}	—		0.95	—	10.0	V	1
Output current of output transistor	I_{OUT}	Nch V_{OUT}=0.5V	V_{DD}=1.2V S-80122 to 60	0.75	1.5	—	mA	2
			V_{DD}=2.4V S-80127 to 60	3.0	6.0	—		
		Pch(only for CMOS output products) V_{DD}-V_{OUT}=0.5V	V_{DD}=4.8V S-80122 to 39	1.0	2.0	—		
			V_{DD}=6.0V S-80140 to 54	1.25	2.5	—		
			V_{DD}=8.4V S-80155 to 60	1.5	3.0	—		
Leakage current of output transistor	I_{LEAK}	Nch (only for Nch open-drein output procudts) V_{DD}=10.0V V_{OUT}=10.0V		—	—	0.1	μA	2
Temperature coefficient of detection voltage *1)	$\frac{\Delta -V_{DET}}{\Delta Ta \bullet -V_{DET}}$	Ta=−40°C to +85°C		—	±120	±360	ppm/°C	1
Delay time 1	td 1	V_{DD}=$-V_{DET}$+1V DS pin : “L”	S-801XXAX	32.5	50	72.5	ms	1
			S-801XXBX	65	100	145		
			S-801XXCX	130	200	290		
Delay time 2	td 2	V_{DD}=$-V_{DET}$+1V, DS pin “H”		110	220	330	μs	3
Current consumption	I_{SS}	V_{DD}=3.5V	S-80122 to 26	—	1.3	3.3	μA	1
		V_{DD}=4.5V	S-80127 to 39	—	1.5	3.5		
		V_{DD}=6.5V	S-80140 to 60	—	1.8	4.0		
Input voltage of DS pin	V_{SH}	V_{DD}=6.0V		1.0	—	—	V	4
	V_{SL}	V_{DD}=6.0V		—	—	0.3	V	4

*1) The detection voltage change for temperature change (mV/°C) is calculated with the following formula:

$$\underbrace{\frac{\Delta -V_{DET}}{\Delta Ta}\left[\text{mV/°C}\right]}_{\text{Detection voltage change for temperature change}} = \underbrace{-V_{DET}(\text{Typ.})\left[\text{V}\right]}_{\text{Detection voltage}} \times \underbrace{\frac{\Delta -V_{DET}}{\Delta Ta \bullet -V_{DET}}\left[\text{ppm/°C}\right]}_{\text{Temperature coefficient of detection voltage}} \div 1000$$

■ Test Circuits

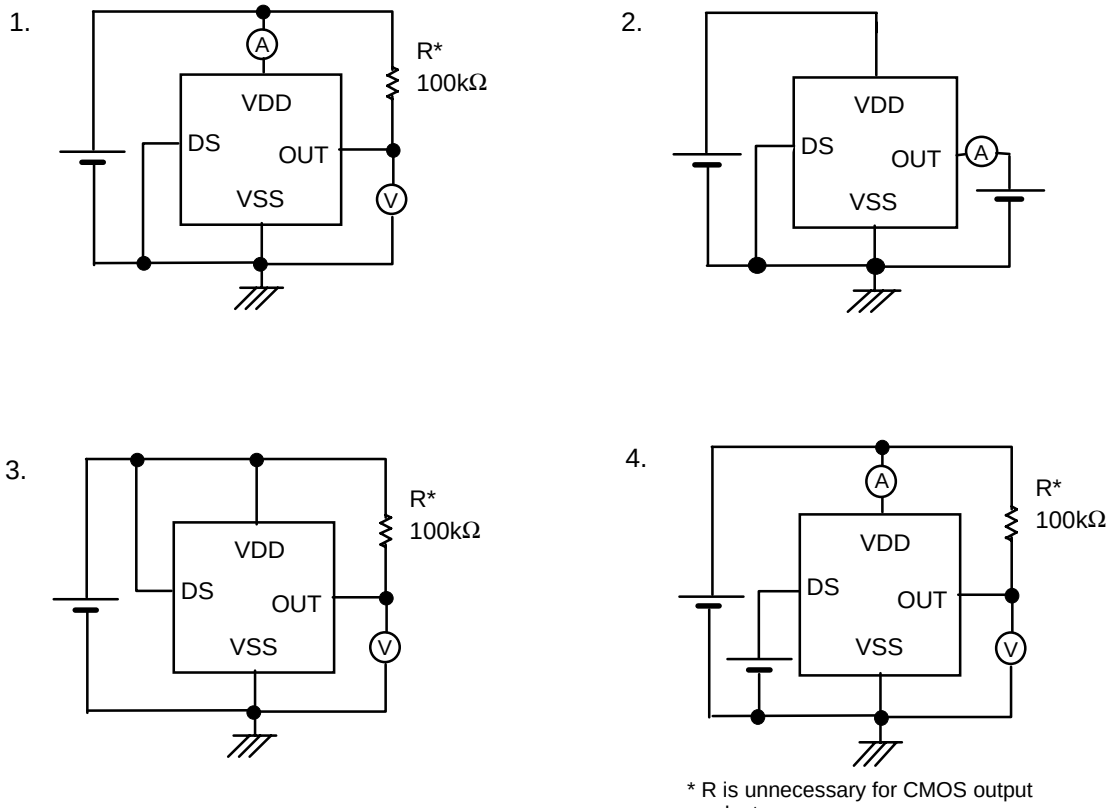


Figure 4 Test Circuits

■ Technical Terms

1. Detection voltage ($-V_{DET}$)

   The detection voltage ($-V_{DET}$) is the voltage at which the output switches to low. This detection voltage varies slightly among products of the same type. The variation of voltages between the specified minimum [($-V_{DET}$)min.] and maximum [($-V_{DET}$)max.] values is called the detection voltage range (See Figure 5).

   Example : For the S-80122AN, detection voltage lies in the range of $2.156 \leq (-V_{DET}) \leq 2.244$.
   This means that $-V_{DET}$ is 2.156 in a product while $-V_{DET}$ is 2.244 in another of the same S-80122AN.

2. Release voltage ($+V_{DET}$)

   The release voltage ($+V_{DET}$) is the voltage at which the output returns (is "released") to high. This release voltage varies slightly among products of the same type. The variation of voltages between the specified minimum [($+V_{DET}$)min.] and maximum [($+V_{DET}$)max.] values is called the release voltage range (See Figure 6).

   Example : For the S-80122AN, the release voltage lies in the range of $2.186 \leq (+V_{DET}) \leq 2.344$.
   This means that $+V_{DET}$ is 2.186 in a product while $+V_{DET}$ is 2.344 in another of the same S-80122AN.

   Remark: Although the detection voltage and release voltage overlap in the range of 2.186 V to 2.244 V, $+V_{DET}$ will always be larger than $-V_{DET}$.

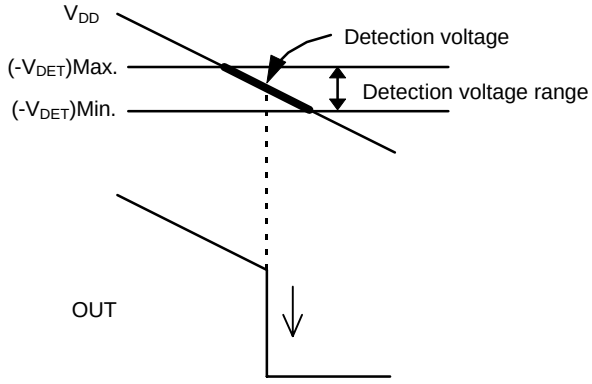


Figure 5 Detection Voltage

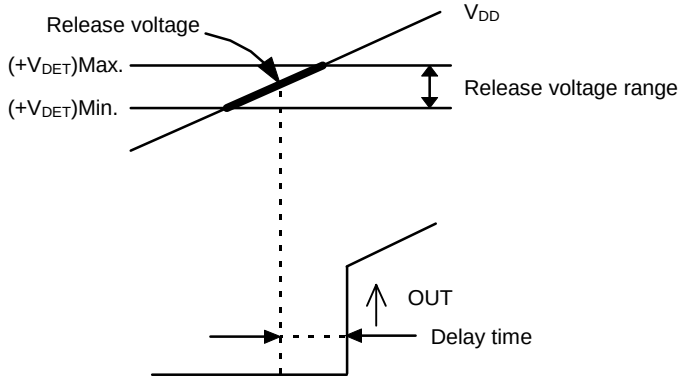


Figure 6 Release Voltage

3. Hysteresis width (V_{HYS})

   The hysteresis width is the voltage difference between the detection voltage and the release voltage (B-A=V_{HYS} in Figure 11). By giving a device hysteresis, trouble such as noise at the input is avoided.

4. Delay time (td)

   The delay time is a time that the input voltage to VDD pin exceeds the release voltage ($+V_{DET}$) and then the output of the OUT pin inverts. The delay time is fixed according to a series.

   - S-801XXAX series: typ.50 ms
   - S-801XXBX series: typ.100 ms
   - S-801XXCX series: typ.200 ms

   The output of the OUT pin can be inverted in a short deley time by inputting "H" to DS pin.

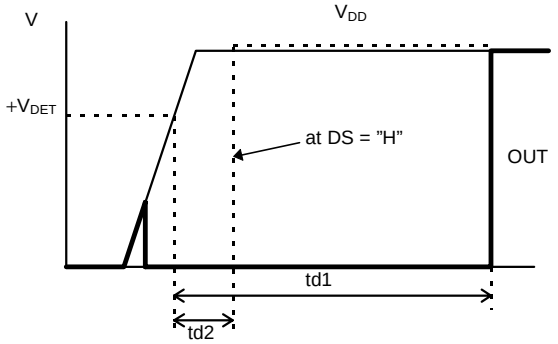


Figure 7 Delay Time

5. Through-type current

   Through-type current refers to the current which flows instantaneously at the time of detection and release of a voltage detector. Through-type current flows in a frequency of 20 kHz for release delay time because internal logic circuit operates.

6. Oscillation

   In applications where a resistor is connected to the voltage detector input (Figure 10), in the CMOS active low products for example, the through-type current generated when the output goes from low to high (release) causes a voltage drop equal to [through-type current] × [input resistance] across the resistor. When the resultant input voltage drops below the detection voltage $-V_{DET}$, the output voltage returns to its low level. In this state, the through-type current and its resultant voltage drop have disappeared, and the output goes back from low to high. A through-type current is again generated, a voltage drop appears, and the process repeats. This unstable condition is referred to as oscillation.

   Misimplementation with input voltage divider

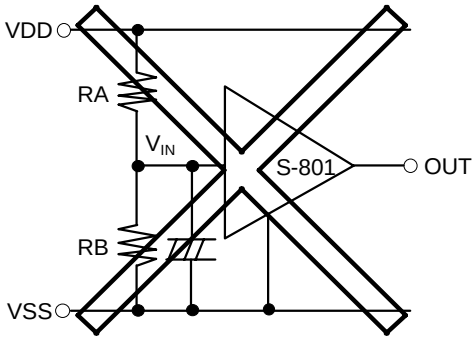
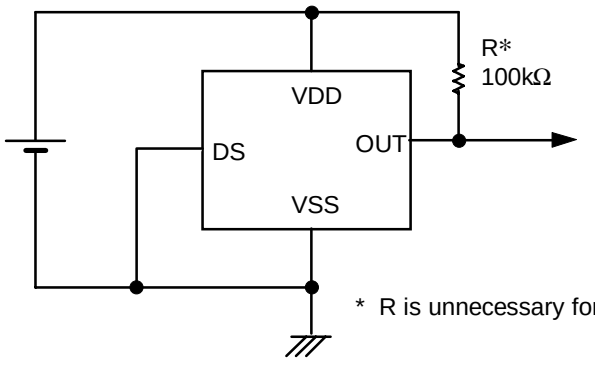


Figure 8 Misimplementation with Input Voltage Divider

■ Standard Circuit



* R is unnecessary for CMOS output products.

Figure 9 Standard Circuit

■ Operation

1. Basic operation : CMOS active low output

(1) When power supply voltage V_{DD} is greater than the release voltage $+V_{DET}$, the Nch transistor is OFF and the Pch transistor ON, causing V_{DD} (high) to appear at the output. With the Nch transistor N1 of Figure 10 OFF, the comparator input voltage is $(RB+RC)/(RA+RB+RC)\times V_{DD}$.
(2) When power supply voltage V_{DD} goes below $+V_{DET}$, the output maintains the power supply voltage level, as long as V_{DD} remains above the detection voltage $-V_{DET}$. When V_{DD} does fall below $-V_{DET}$ (A in Figure 11), the Nch transistor goes ON, the Pch transistor goes OFF, and V_{SS} appears at the output. With the Nch transistor N 1 of Figure 10 ON, the comparator input voltage is $RB/(RA+RB)\times V_{DD}$.
(3) When V_{DD} falls below the minimum operating voltage, the output becomes undefined. However, output will revert to V_{DD} if a pull-up has been employed.
(4) V_{SS} will again be output when V_{DD} rises above the minimum operating voltage. V_{SS} will continue to be output even when V_{DD} surpasses $-V_{DET}$, as long as it does not exceed the release voltage $+V_{DET}$.
(5) When V_{DD} rises above $+V_{DET}$ (B in Figure 11), the Nch transistor goes OFF, the Pch transistor goes ON, and V_{DD} appears at the output. Then V_{DD} at the OUT pin appears with delay time(td) due to delay circuit.

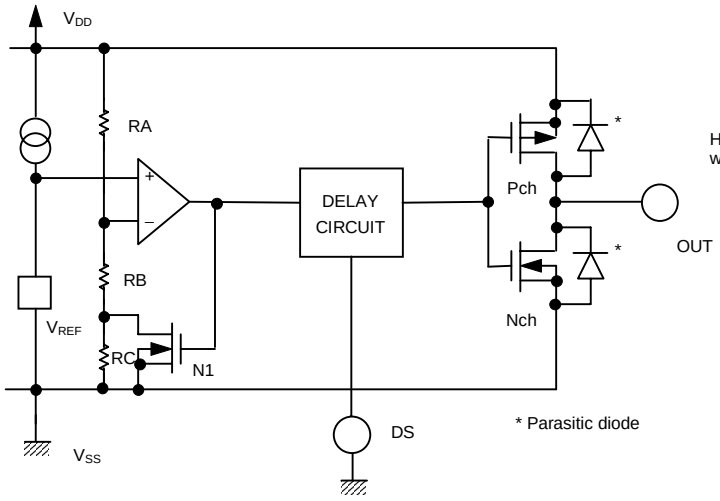


Figure 10 Operation 1

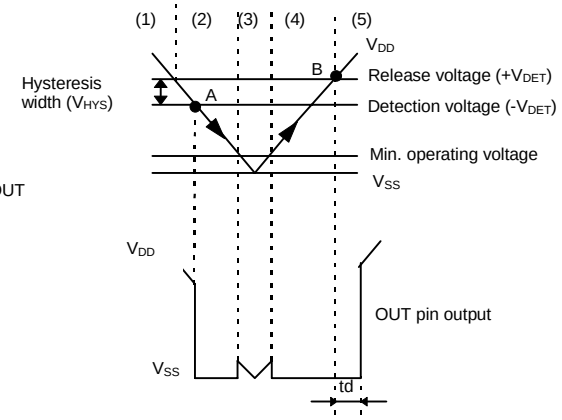


Figure 11 Operation 2

2. Delay circuit

(1) Dalay time

The delay circuit outputs the signal delayed from the release voltage ($+V_{DET}$) point of the power voltage V_{DD} rising. The output signal is not delayed when the V_{DD} goes down the detection voltage ($-V_{DET}$) or less. (See Figure 11).
The delay time (td) is a fixed value that is determined by a built-in oscillator circuit and counter.

(2) DS pin: ON/OFF switch of delay time

Always connect DS pin to “L” or “H”. When DS pin is in “H”, a delay time of output becomes short because the output signal is output in the middle of count. (See “Delay time 2” in Table 4.)

3. Other characteristics

(1) Temperature characteristic of detection voltage

The temperature characteristics of the detection voltage are expressed by the oblique line parts in Figure 12.

S-80122XXMC:

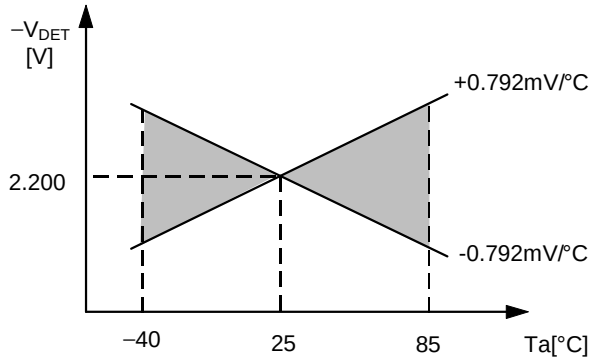


Figure 12 Temperature Characteristics of Detection Voltage

(2) Temperature characteristics of release voltage

The temperature factor $\left(\frac{\Delta + V_{DET}}{\Delta Ta}\right)$ of the release voltage is calculated by the temperature factor $\left(\frac{\Delta - V_{DET}}{\Delta Ta}\right)$ of the detection voltage as follows:

$$\frac{\Delta + V_{DET}}{\Delta Ta} = \frac{+V_{DET}}{-V_{DET}} \times \frac{\Delta - V_{DET}}{\Delta Ta}$$

The temperature factor of the release voltage has a same sign characteristics as the temperature factor of the detection voltage.

(3) Temperature characteristics of hysteresis voltage

The temperature characteristics of hysteresis voltage $\left(\frac{\Delta + V_{DET}}{\Delta Ta} - \frac{\Delta - V_{DET}}{\Delta Ta}\right)$ is calculated as follows:

$$\frac{\Delta + V_{DET}}{\Delta Ta} - \frac{\Delta - V_{DET}}{\Delta Ta} = \frac{V_{HYS}}{-V_{DET}} \times \frac{\Delta - V_{DET}}{\Delta Ta}$$

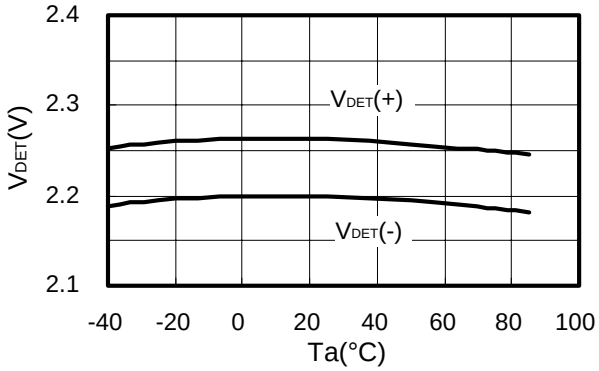
■ Notes

- In CMOS output products of the S-801 Series, through type current flows when the device is detecting or releasing. If a high impedance is connected to the input, oscillation may be caused due to the fall of the voltage by the through type current during releasing.
- In S-801 series products, through-type current flows in a frequency of approx. 20 kHz for a delay time because internal oscillator circuit and counter timer operate at voltage release. High impeadance of input by connecting a resistor may cause an oscillation by through-type current. When impeadance of input is high, insert a capacitor between VDD and VSS pins to prevent an oscillation.
- When designing for mass production using an application circuit described herein, take the product deviation and temperature characteristic into consideration.
- Seiko Instruments Inc. shall not bear any responsibility for the patents on the circuits described herein.

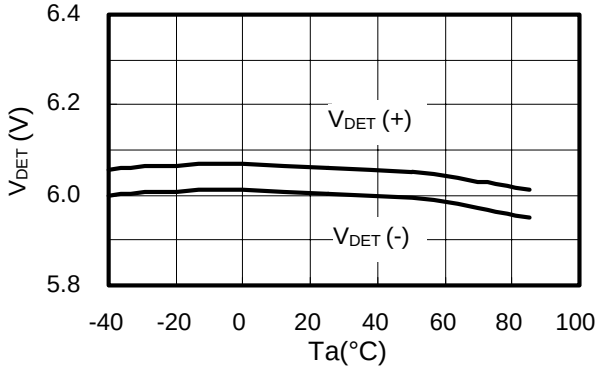
■ Characteristics (typical characteristics)

(1) Detection voltage (V_{DET}) - Temperature (Ta)

S-80122AL

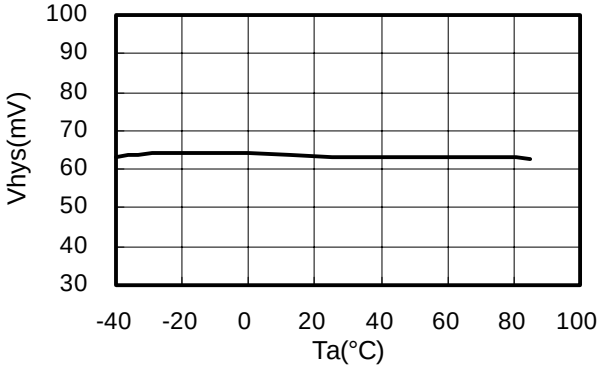


S-80160AL

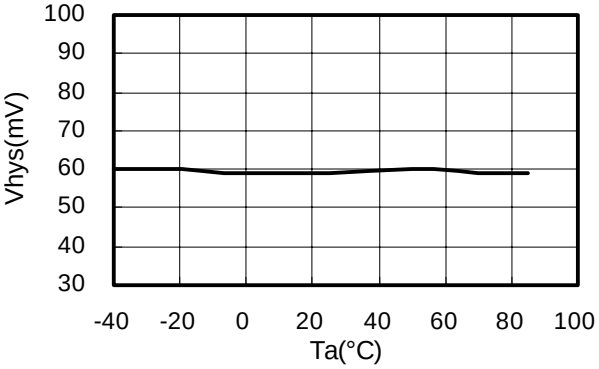


(2) Hysteresis voltage width (Vhys) - Temperature (Ta)

S-80122AL

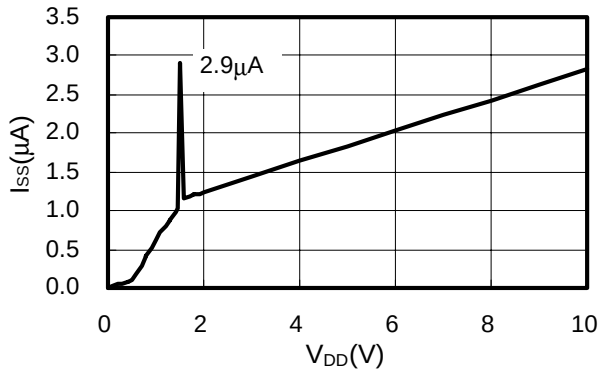


S-80160AL

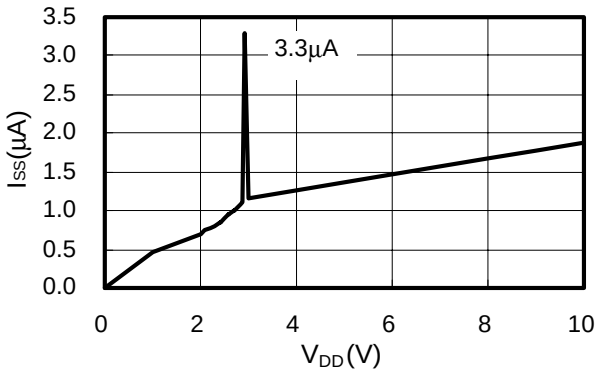


(3) Current consumption (I_{SS}) - Input voltage (V_{DD})

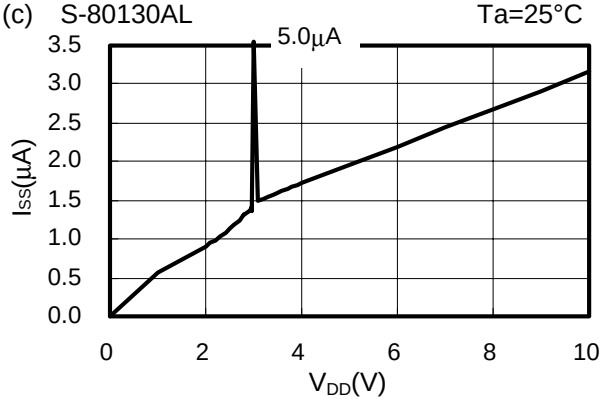
(a) S-80122AL Ta=25°C



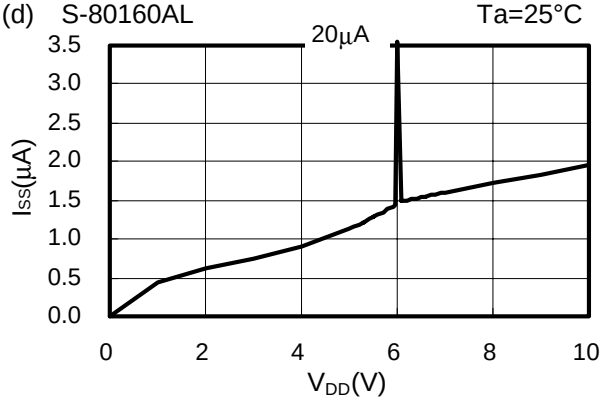
(b) S-80129AL Ta=25°C



(c) S-80130AL Ta=25°C

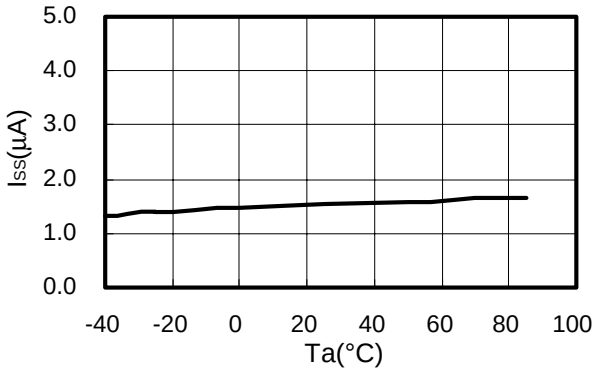


(d) S-80160AL Ta=25°C

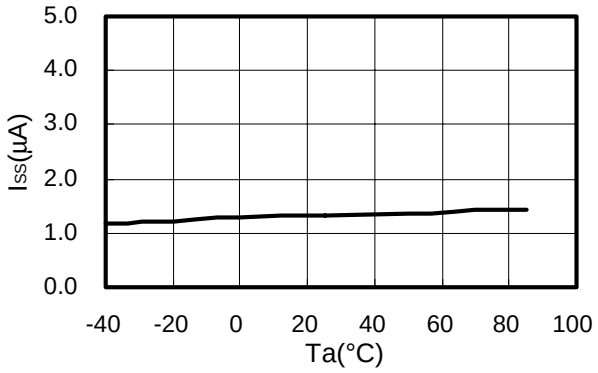


(4) Current consumption (I_{SS}) - Temperature (Ta)

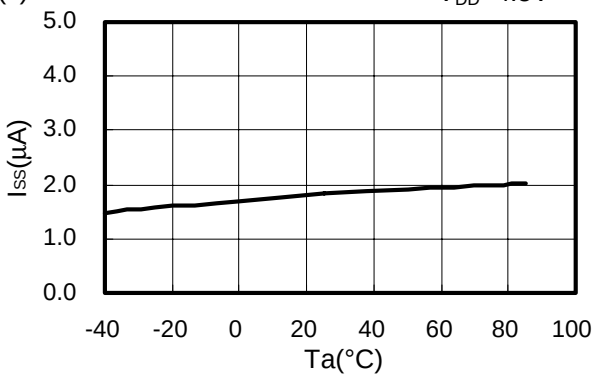
(a) S-80122AL V_{DD}=3.5V



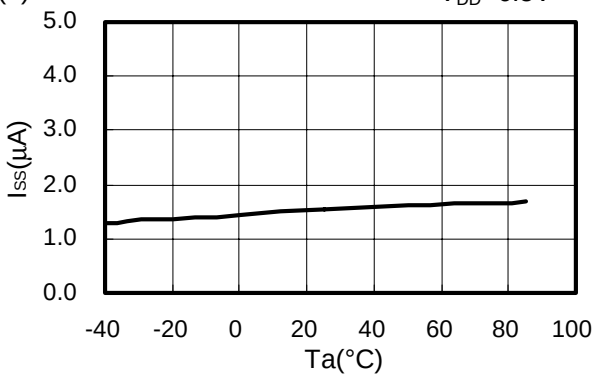
(b) S-80129AL V_{DD}=4.5V



(c) S-80130AL V_{DD}=4.5V

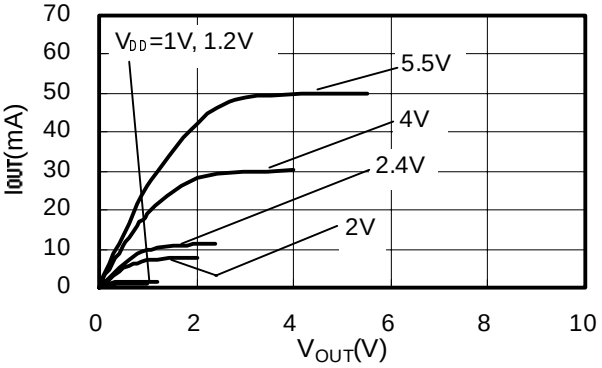


(d) S-80160AL V_{DD}=6.5V



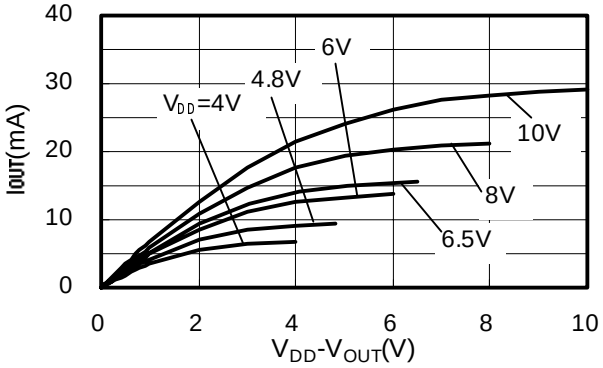
(5) Nch transistor output current (I_{OUT}) - V_{OUT}

S-80160AL Ta=25°C



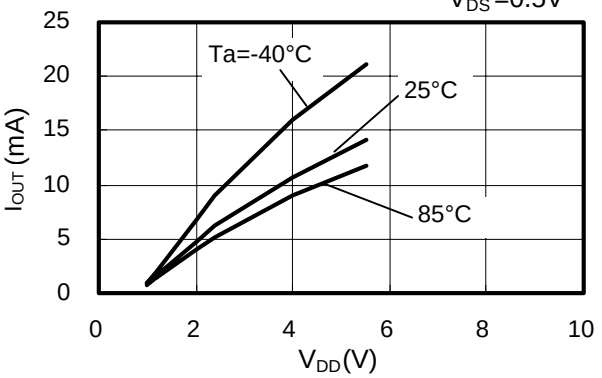
(6) Pch transistor output current (I_{OUT}) - (V_{DD}-V_{OUT})

S-80122AL Ta=25°C



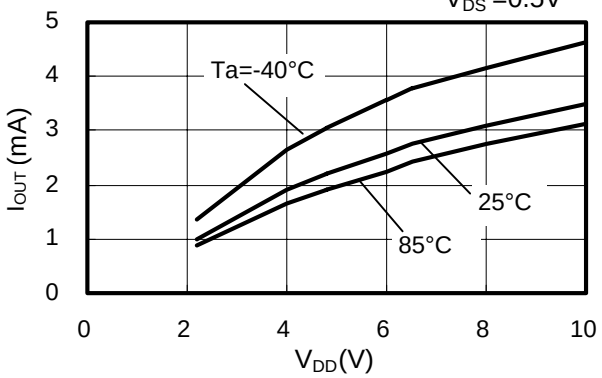
(7) Nch transistor output current (I_{OUT}) - Input voltage(V_{DD})

S-80160AL V_{DS}=0.5V

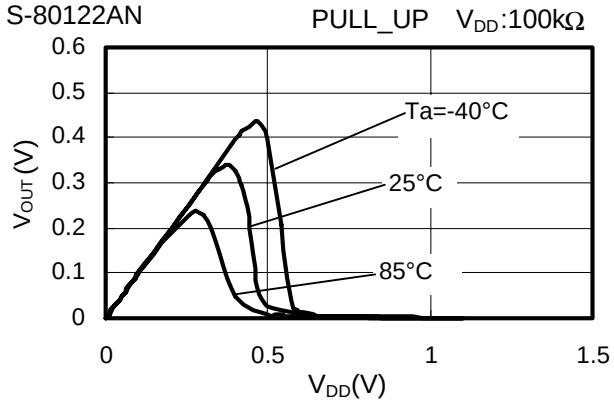


(8) Pch transistor output current(I_{OUT}) - Input voltage(V_{DD})

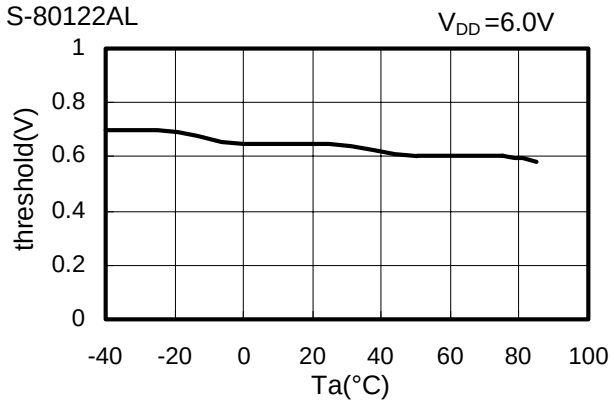
S-80122AL V_{DS}=0.5V



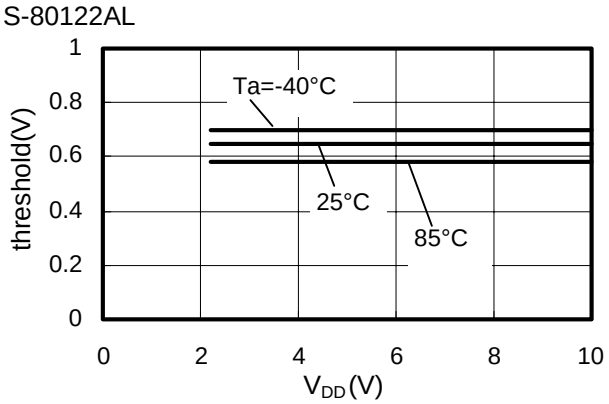
(9) Minimum operating voltage - Input voltage(V_{DD})



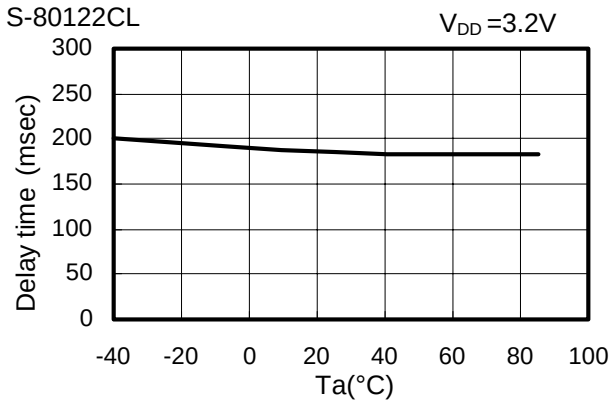
(10) Threshold voltage of DS pin - Temperature (Ta)

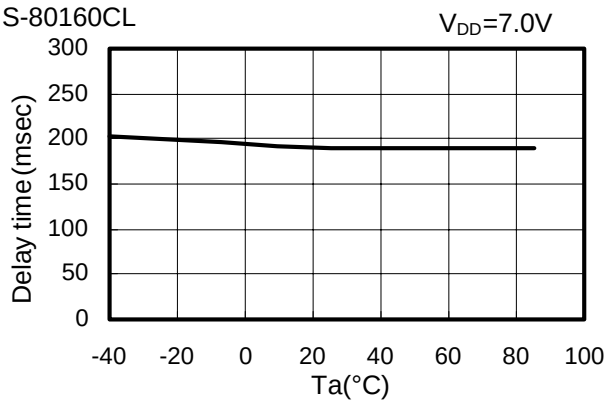


(11) Threshold voltage of DS pin - Input voltage (V_{DD})

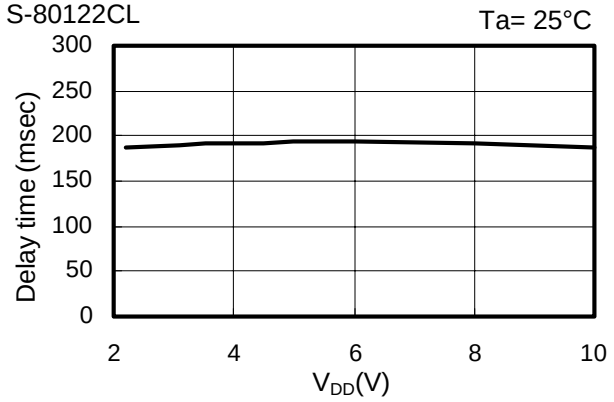


(12) Delay time 1 - Temperature (Ta)

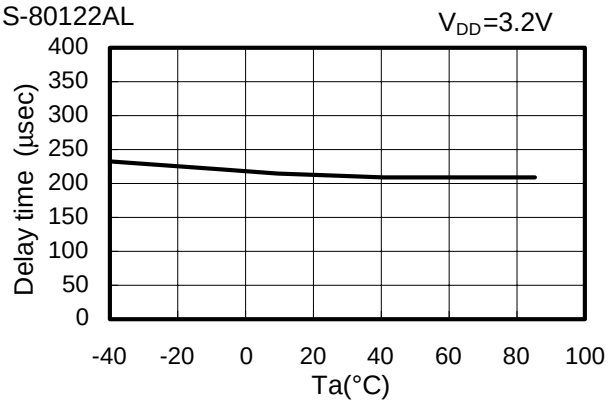


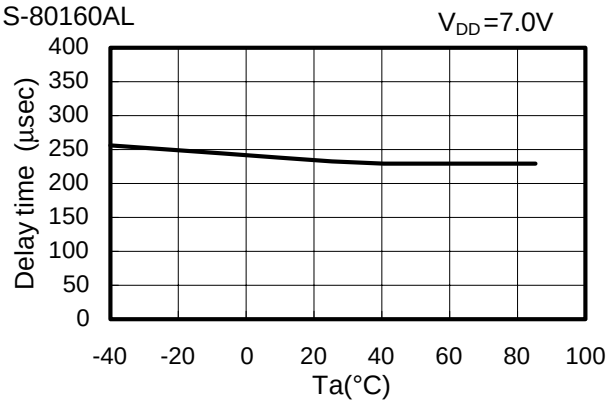


(13) Delay time 1 - Input voltage (V_{DD})

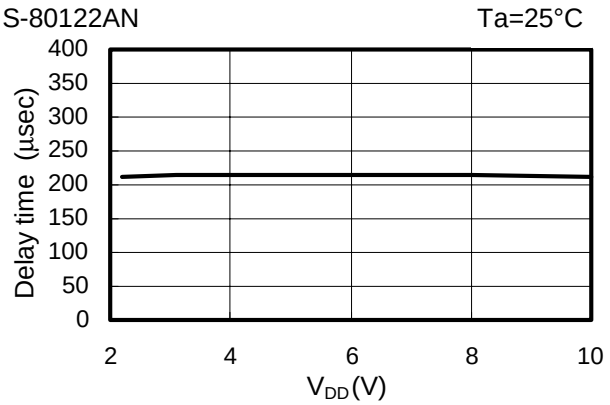


(14) Delay time 2 - Temperature (Ta)





(15) Delay time 2 - Input voltage (V_{DD})



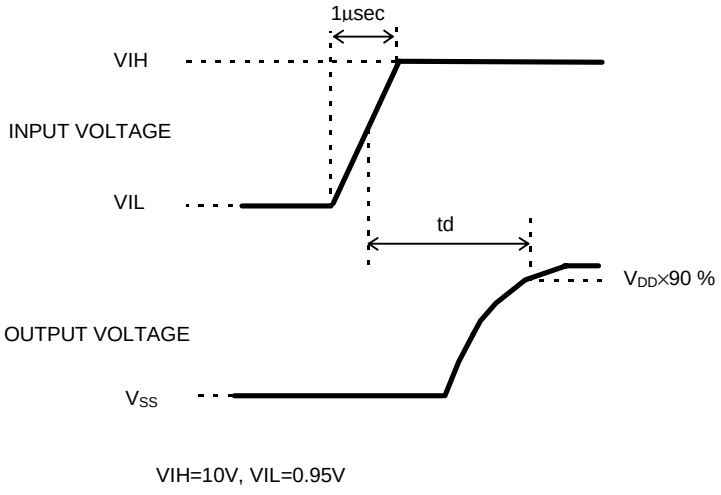
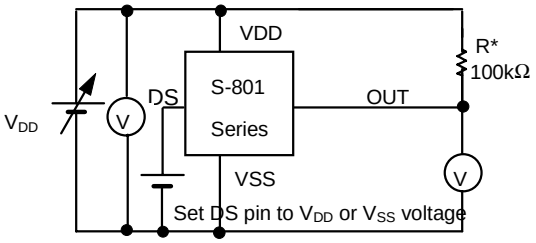


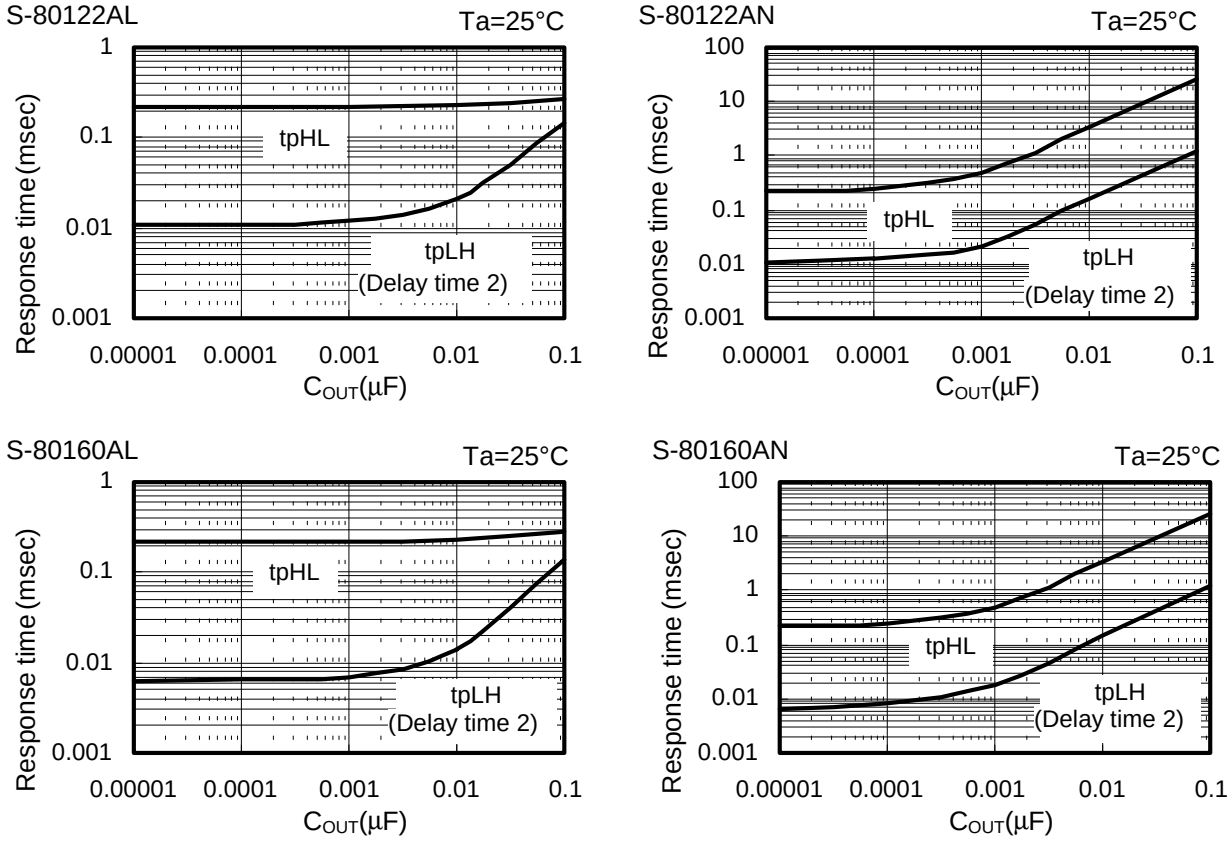
Figure 13 Measuring Conditions of Delay Time



* R is not necessary for CMOS output products.

Figure 14 Measuring Circuit of Delay Time

(16) Response time - Load capacitor (C_{OUT})



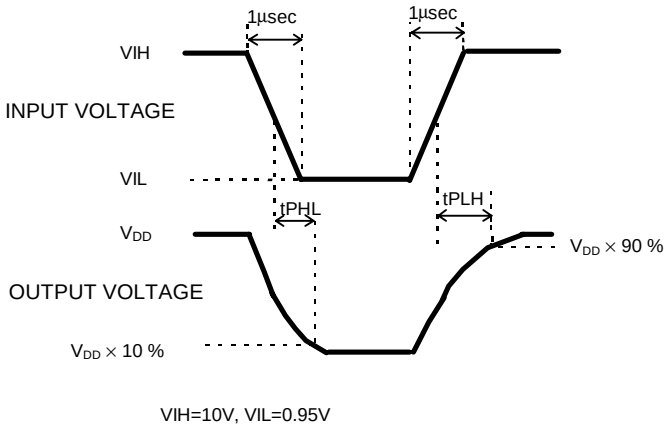
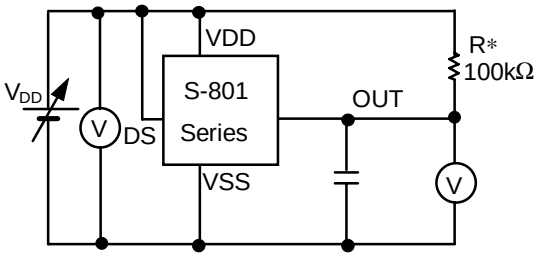


Figure 15 Measuring Conditions of Response Time



* R is not necessary for CMOS output products.

Figure 16 Measuring Circuit of Delay Time

■ Application Circuit Examples

1. Microcomputer reset circuits

   With the S-801 Series which has a low operating voltage, a high-precision detection voltage, hysteresis characteristic, and a built-in delay circuit, the reset circuits shown in Figures 17 to 18 can be easily constructed.

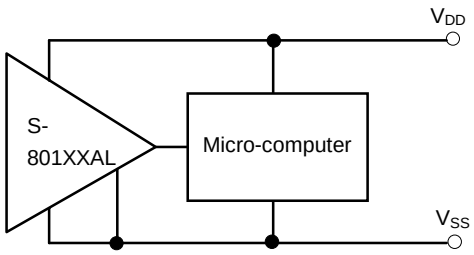
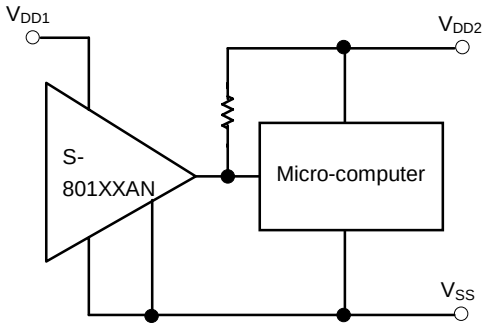


Figure 17 Reset Circuit (S-801XXAL)



(Nch open-drain output products only)

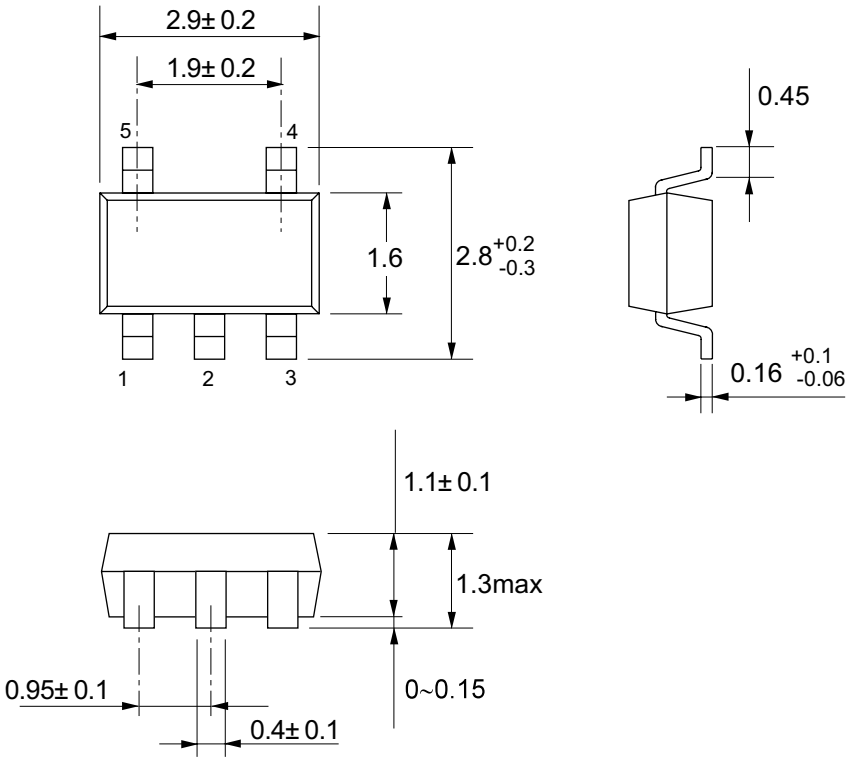
Figure 18 Reset Circuit (S-801XXAN)

■ SOT-23-5

MP005-A 991105

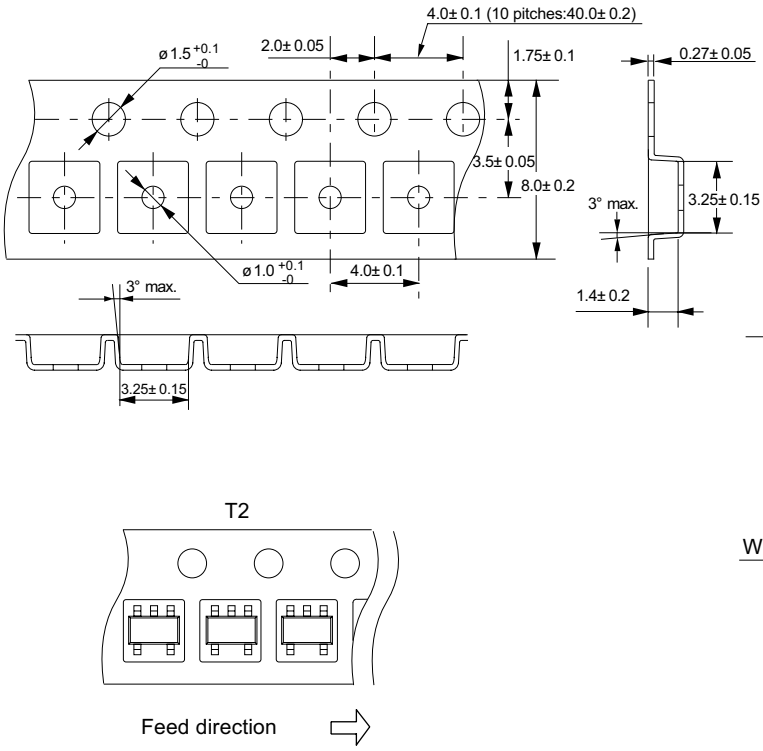
Unit: mm

●Dimensions



No.:MP005-A-P-SD-1.0

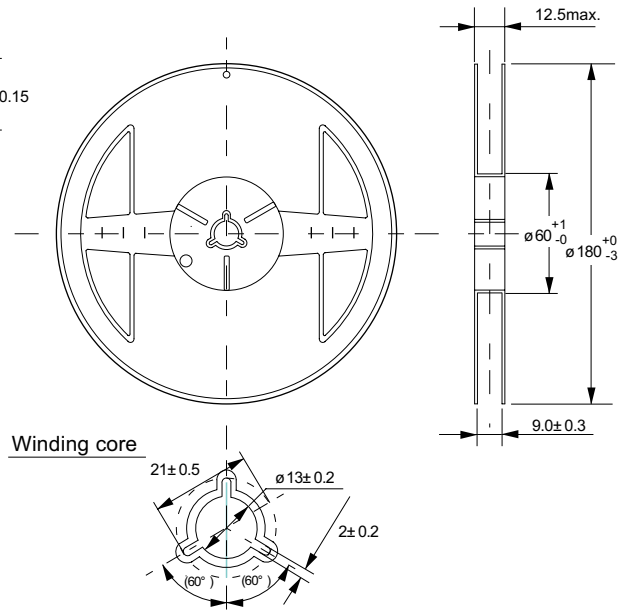
●Taping Specifications



No.:MP005-A-C-SD-1.0

●Reel Specifications

3000 pcs./reel



No.:MP005-A-R-SD-1.0

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