

Simple Interface Between D/A Converter and Microcomputer Leads to Programmable Sine-Wave Oscillator

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This application note outlines a very simple interface between the AD7542, a 12-bit CMOS D/A converter, and one of the most popular industry building blocks available, the 8-bit MCS-48 microcomputer family. The interface is used in a circuit which generates programmable low distortion sine waves. The circuit is based upon repeatedly adding a known constant to an accumulator which in turn scans a sine look-up table. The data from this table is presented to the DAC for conversion into an analog waveform. Changing the constant changes the generated output frequency.

THE INTERFACE

The AD7542 accepts data in three 4-bit nibbles over a 4-bit wide data bus. The data is stored in three 4-bit data registers until, under program control, the new 12-bit word is transferred to the DAC register to update the analog outputs (see Figure 1). Internal register selection is achieved by decoding the address inputs A0 and A1 as shown in Table I. All data loading or data transfer operations are synchronized to the rising edge of the control signal $\overline{WR}$.

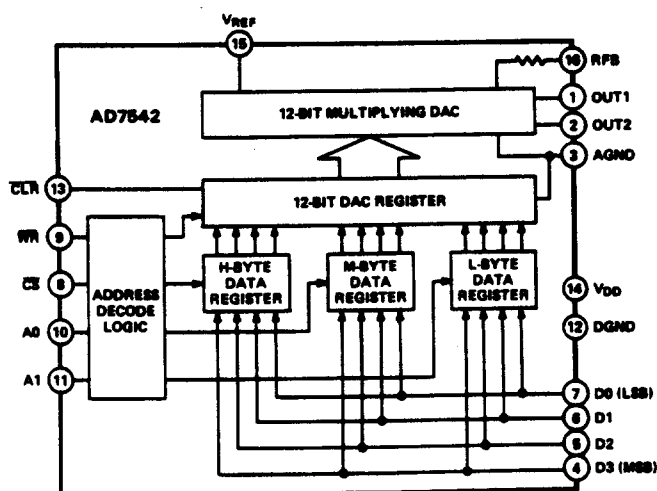


Figure 1. AD7542 Functional Block Diagram

A1 (Pin 11)	A0 (Pin 10)	Register Selected
0	0	Low Byte Register
0	1	Mid Byte Register
1	0	High Byte Register
1	1	DAC Register

Table 1. AD7542 Internal Register Decoding

On all MCS-48 microcomputers the lower half of Port 2, P20-P23, can be used for I/O expansion with a dedicated I/O expander device, the 8243. The 8243 contains four 4-bit I/O ports which serve as extension of the on-chip I/O and are addressed as ports 4-7 with their own MOV, ANL and ORL instructions.

All communications between the MCS-48 microcomputer and the 8243 occurs over P20-P23 with timing provided by an output pulse on the PROG pin of the processor. The AD7542 is interfaced to the MCS-48 microcomputer over P20-P23 and is accessed by the processor as if it were an 8243. However, only the Transfer Accumulator to Port instructions are used in the interface. Each transfer consists of two 4-bit nibbles, the first containing the "op-code" and port address and the second containing the actual 4-bits of data.

Referring to Figure 2, a high to low transition of the PROG line indicates that address and op-code information are present on P20-P23. The port address on lines P20 and P21 must be externally latched at this point in time. The MCS-48 timing ensures that the falling edge of PROG coincides with the falling edge of ALE. Thus ALE is used to latch the port address information into an external 7475-type latch. The op-code information is not used in this application. When PROG returns high, the 4-bit wide bus contains valid data. By driving the $\overline{WR}$ input of the AD7542 with the PROG line, valid data is loaded into the AD7542 at this time.

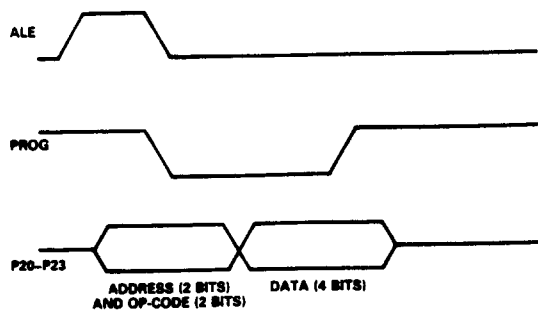


Figure 2. Expander I/O Interface Timing

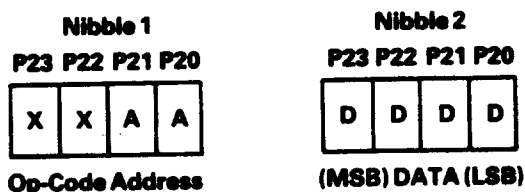


Figure 3. Basic AD7542 to MCS-48 Interface

PROGRAMMABLE SINE-WAVE GENERATOR

One method of generating sine waves is to drive an up-counter at a given clock rate, the output of the counter being applied to a look-up table containing phase-angle information. This data in turn is fed to a DAC which generates the sampled waveform. A low-pass filter is then used to smooth the output waveform. The easiest way to change the output frequency is to increase the rate at which the counter is driven. However, changing the fundamental sampling frequency has severe implications for the output filter. If the software that loads the counter, instead of incrementing it by one per loop, increases the counter by two in the same period of time, the counter fills and rolls over twice as quickly. Thus, although the rate of counter loading—the sampling frequency—remains the same, doubling the loaded value—the frequency constant—doubles the output frequency. In the same way, each integer multiple of the initial frequency constant produces a corresponding multiplication of the output frequency. This is the basis of the technique used here and is described in more detail in References 1-3. The references also include software examples for using the circuit to generate touch-tone frequencies for telecommunication applications.

The number of bits in the accumulator (or counter), m , is determined by the resolution required in output frequency variation. The number of possible output signal frequencies is $2^m - 1$, and the spacing between them is inversely proportional to 2^m . A 14-bit accumulator is sufficient for the 1Hz spacing required here. The generated output frequency is given by

$$f_s = \frac{N \cdot f_c}{2^m}$$

where: N is the frequency constant which establishes the output frequency.

f_c is the frequency of executing the loop, i.e., the sampling frequency.

m is the number of bits in the accumulator

Choosing a base frequency constant of 1 to produce a 1Hz output signal ensures that all other frequency constants N always equal the output frequency. Thus for a 14-bit counter to increment in single steps and roll over to zero once per second, requires a sampling rate of 2^{14} samples/sec (a sampling frequency of 16,384Hz). Thus each timing

A (P21)	A (P20)	Port Selected
0	0	Port 4
0	1	Port 5
1	0	Port 6
1	1	Port 7

Table II. Expander I/O Multiplexed Bus (P20-P23)

Table II shows the two nibbles of a transfer instruction. Comparing Table II with Table I, it can be seen that the address of the Low Byte register is the same as the Port 4 address in the I/O expansion mode. Thus a TRANSFER ACCUMULATOR TO PORT 4 instruction will in fact load the Low Byte register of the AD7542. A similar correspondence exists between the remaining AD7542 registers and the MCS-48 expansion ports. Only four instructions are thus required to load the AD7542:

```

MOVD P4,A  Load Low Byte register
MOVD P5,A  Load Mid Byte register
MOVD P6,A  Load High Byte register
MOVD P7,A  Load DAC register

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The basic hookup is shown in Figure 3.

The advantage of this interface lies in its simplicity. In either single or multi-DAC applications, mapping the AD7542's as I/O devices greatly simplifies both the software and the chip select decoding over what would be required if the devices were memory mapped (in external data memory).

Multiple AD7542s can be connected to P20-P23 if additional chip select lines are supplied for the additional devices. For instance using the top half of Port 2 (P24-P27) directly as chip selects allows a maximum of four AD7542s on the I/O port; using P24-P27 with a 4-to-16 line decoder (such as the 8205) allows a maximum of sixteen AD7542s on the port.

loop should take 61.035 μ s to execute. For the MCS-48 family, the external crystal frequency is divided by fifteen to provide the internal machine cycle time. A crystal of 4.9155MHz gives a machine cycle time of 3.056 μ s which means 20 machine cycles per timing loop. Any branch in the program must be tailored so that a complete loop through the program will always take 20 machine cycles.

THE SINE TABLE

The MCS-48 architecture limits the external look-up table to 256 entries. Thus, 256 bytes encode the sine functions 360° in 1.406° steps (360/256). Placing the full 360° in the look-up table simplifies the software at the expense of increased distortion in the output. The synthesis program of Reference 2 stores a quarter period (first quadrant) of the output waveform in the look-up table and gives the software required to generate the additional quadrants.

The high byte of the 14-bit accumulator is used as a pointer to reference the look-up table. The complete look-up table is shown in Table III along with the BASIC program used to generate the table on an AIM-65. The AD7542 in Figure 5 is arranged for bipolar operation with offset binary coding. To ensure that the output waveform is symmetrical around 0V, the entries in the look-up table are adjusted so that the value FFH is assigned to the greatest positive amplitude equal to ($V_{REF} - 1\text{LSB}$) for 90°, and the value 01H to the greatest negative amplitude equal to $-(V_{REF} - 1\text{LSB})$ for 270°. This allows the output for 0° and 180° to fall exactly on 80H—equivalent to 0V output for bipolar operation.

0700	80	83	86	89	0780	80	7D	7A	77
0704	8C	90	93	96	0784	74	70	6D	6A
0708	99	9C	9F	A2	0788	67	64	61	5E
070C	A5	A8	AB	AE	078C	5B	58	55	52
0710	B1	B3	B6	B9	0790	4F	4D	4A	47
0714	BC	BF	C1	C4	0794	44	41	3F	3C
0718	C7	C9	CC	CE	0798	39	37	34	32
071C	D1	D3	D5	D8	079C	2F	2D	2B	28
0720	DA	DC	DE	EO	07A0	26	24	22	20
0724	E2	E4	E6	E8	07A4	1E	1C	1A	18
0728	EA	EB	ED	EF	07A8	16	15	13	11
072C	F0	F1	F3	F4	07AC	10	0F	0D	0C
0730	F5	F6	F8	F9	07B0	0B	0A	08	07
0734	FA	FA	FB	FC	07B4	06	06	05	04
0738	FD	FD	FE	FE	07B8	03	03	02	02
073C	FE	FF	FF	FF	07BC	02	01	01	01
0740	FF	FF	FF	FF	07C0	01	01	01	01
0744	FE	FE	FE	FD	07C4	02	02	02	03
0748	FD	FC	FB	FA	07C8	03	04	05	06
074C	FA	F9	F8	F6	07CC	06	07	08	0A
0750	F5	F4	F3	F1	07D0	0B	0C	0D	0F
0754	F0	EF	ED	EB	07D4	10	11	13	15
0758	EA	E8	E6	E4	07D8	16	18	1A	1C
075C	E2	E0	DE	DC	07DC	1E	20	22	24
0760	DA	D8	D5	D3	07E0	26	28	2B	2D
0764	D1	CE	CC	C9	07E4	2F	32	34	37
0768	C7	C4	C1	BF	07E8	39	3C	3F	41
076C	BC	B9	B6	B3	07EC	44	47	4A	4D
0770	B1	AE	AB	A8	07F0	4F	52	55	58
0774	A5	A2	9F	9C	07F4	5B	5E	61	64
0778	99	96	93	90	07F8	67	6A	6D	70
077C	8C	89	86	83	07FC	74	77	7A	7D

Table IIIa. Look-Up Table for 360° of Output Waveform

```

L      = 3840
FOR X = 0 to 255
LET A = Sin[(X * 1.40625)/57.2958]
LET Y = INT(128.5 + 127 * A)
POKE L, Y
LET L = L + 1
NEXT X
END

```

Table IIIb. Basic Program for AIM-65 Used to Generate Look-Up Table

SOFTWARE AND HARDWARE

Figure 4 shows the arrangement of registers within the microcomputer. The accumulator is implemented with two 8-bit registers, Reg 0 and Reg 1. Register 0 is the least significant. The frequency constant N is stored in Reg 2 and Reg 3. Register 2 is the least significant. Both the 14-bit accumulator and the 14-bit wide frequency constant occupy the most significant 14-bits of their respective register pairs. The high byte of the 14-bit accumulator is used as the pointer for accessing the look-up table.

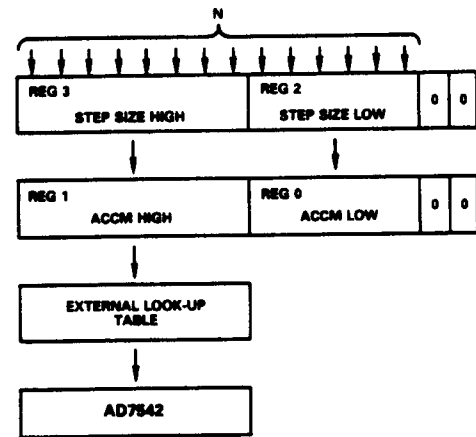


Figure 4. Register Arrangement for Program

The sequence of actions for the synthesis of a sine-wave output is shown in Table IV with the actual program listing in Table V. A circuit diagram of the synthesizer is shown in Figure 5. The 2716 EPROM contains both the program and the sine look-up table for the 8035. Program memory is all external and starts at location 000H, the address to which the processor is vectored after a Reset. The look-up table is treated as external data memory and occupies the highest page in the 2716—starting at 700H—for ease of decoding.

Bit 7 of Port 2 (P27) is used to differentiate between the high and low byte of the right-justified frequency constant N being loaded in through Port 1. A low level on P27 indicates the low byte (8LSB's) is present on P17–P10, a high level on P27 indicates the high byte (8LSB's) is present on P15–P10. For the program to work properly, the low byte of the frequency constant—with P27 low—must be present on Port 1 before a Reset is applied. Almost immediately after a Reset, the low byte is read and the program enters

a loop to allow the high byte of the frequency constant to be presented at Port 1. The program exits the loop—when P27 goes high—by reading the high byte. The frequency constant is next shifted left two places to position it properly in Registers 2 and 3 before the program enters the frequency synthesis loop properly.

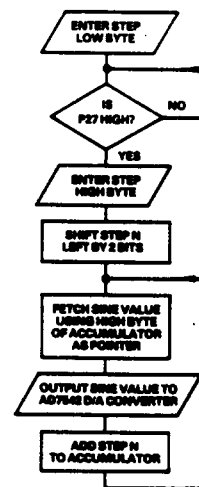


Table IV. Sequence of Action for Sine-Wave Generation

	Location	Op-Code	Mnemonic	Statement
	0000	27	CLR A	
	01	A8	MOV R0,A	Clear 14-Bit Accumulator
	02	A9	MOV R1,A	
	03	3C	MOVD P4,A	Clear 4 LSB's of DAC
	04	09	IN A,P1	Get Low Byte of Frequency Constant
LOOP 1	05	AA	MOV R2,A	
	06	0A	IN A,P2	Test for High Byte
	07	F7	RLC A	
	08	E6	JNC LOOP 1	
	09	06		
	0A	09	IN A,P1	Get High Byte of Frequency Constant
	0B	AB	MOV R3,A	
	0C	97	CLR C	
	0D	FA	MOV A,R2	Shift Frequency Constant Two Places to the Left
	0E	6A	ADD A,R2	
	0F	AA	MOV R2,A	
	10	FB	MOV A,R3	
	11	7B	ADDC A,R3	
	12	AB	MOV R3,A	
	13	97	CLR C	
	14	FA	MOV A,R2	
	15	6A	ADD A,R2	
	16	AA	MOV R2,A	
	17	FB	MOV A,R3	
	18	7B	ADDC A,R3	
LOOP 2	19	AB	MOV R3,A	
	1A	81	MOVX A,R1	Fetch Sine Value
	1B	3D	MOVD P5,A	Output Sine Value to DAC
	1C	47	SWAP A	
	1D	3E	MOVD P6,A	
	1E	3F	MOVD P7,A	
	1F	97	CLR C	
	20	F8	MOV A,R0	Update Low Byte of Accumulator
	21	6A	ADD A,R2	
	22	A8	MOV R0,A	
	23	F9	MOV A,R1	Update High Byte of Accumulator
	24	7B	ADDC A,R3	
	25	A9	MOV R1,A	
	26	00	NOP	Filler to Obtain Desired Sampling Frequency
	27	00	NOP	
	28	04	JMP LOOP 2	
	0029	1A		

Table V. Program Listing for Sine-Wave Generation

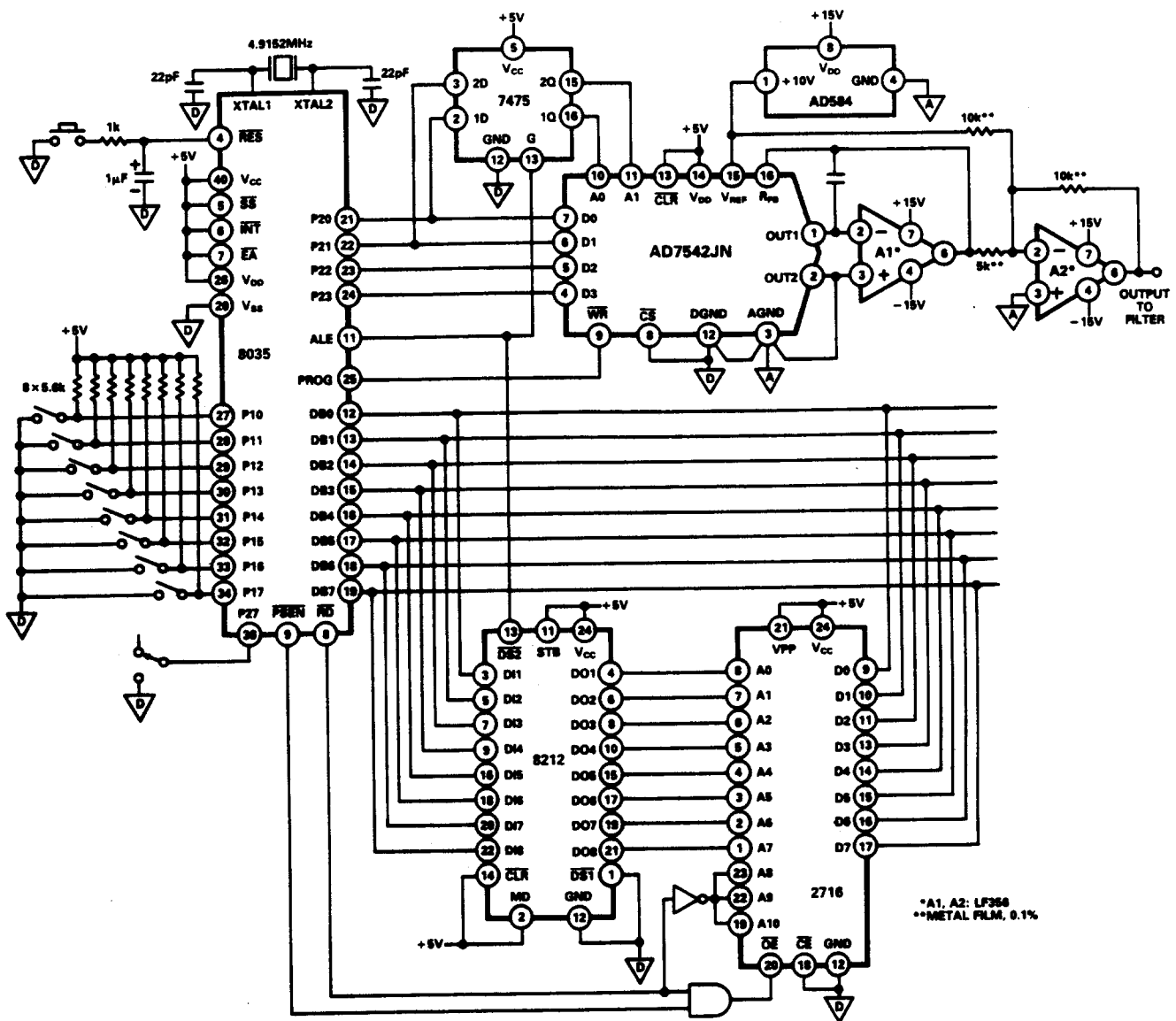


Figure 5. Circuit Diagram of Frequency Synthesizer

EXPERIMENTAL RESULTS

The filter used to smooth the output waveform from the DAC is a sixth-order active RC low-pass filter (Reference 3) and is shown in Figure 6. The cut-off frequency is 4kHz. The response is down 58dB at 8kHz, half the sampling frequency. Experimental results are shown in Table VI.

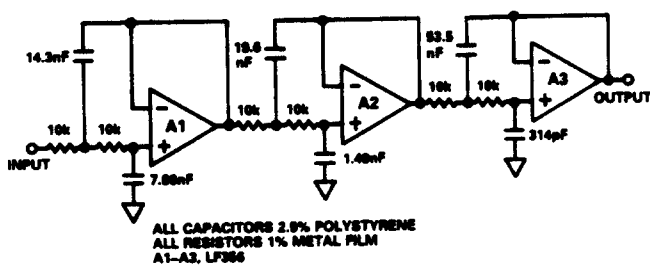


Figure 6. Low-Pass Output Filter, 4kHz Bandwidth

Input Frequency Constant N in Decimal	Output Frequency	Total Harmonic Distortion (dB)
0	0	-
1	1	-
16	16	-48
17	17	-48
32	32	-52.6
33	33	-48
64	64	-54.8
65	65	-43
128	128.01	-56.2
129	129.01	-44.7
256	256.02	-54.6
257	257.02	-45.2
512	512.05	-55.4
513	513.05	-44.1
1024	1024.1	-55
1025	1025.1	-45
2048	2048.2	-52.4
2049	2049.2	-44.8
4096	4096.4	-57
4097	4097.4	-47

Table VI. Experimental Results from Frequency Synthesizer

An interesting feature of the results in Table VI is the increased distortion of output waveforms whose frequencies are not integer power's of 2. For instance at $f_{OUT} = 1024\text{Hz}$ (2^{10}Hz) total harmonic distortion is -55dB ; at $f_{OUT} = 1025\text{Hz}$ the output distortion is -45dB , an increase of 10dB . This is due to harmonics being generated at the "carry" frequency, the frequency at which the low byte of the 14-bit accumulator (in Reg 0) generates a carry to the high byte of the accumulator (in Reg 1). When synthesizing an output frequency of 1025Hz a carry between Reg 0 and Reg 1 is generated every 64 passes through the loop. Since one pass through the loop takes $61\mu\text{s}$ a series of harmonics spaced at 256Hz intervals is added to the output spectrum causing the 10dB deterioration in total harmonic distortion. See Figures 7a and 7b.

ACKNOWLEDGMENTS

To Norm Bernstein for originally suggesting the interface.

REFERENCES

1. J.E. Galbraith, "Generate Sine Waves by Direct Table Look-Up," EDN, April 28, 1982, pg 101.
2. T.S. Kinsel and J.H. Wuorinen, "A Digital Signal Generator," IEEE Micro, Nov, 1981, pg 6.
3. H. Chamberlin, "Musical Applications of Microprocessors," Hayden, 1980, pg 369.

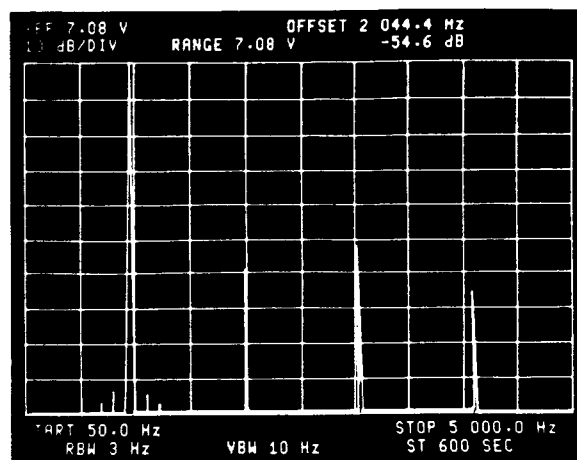


Figure 7a. Output Waveform Spectrum for $F_{OUT} = 1024\text{Hz}$

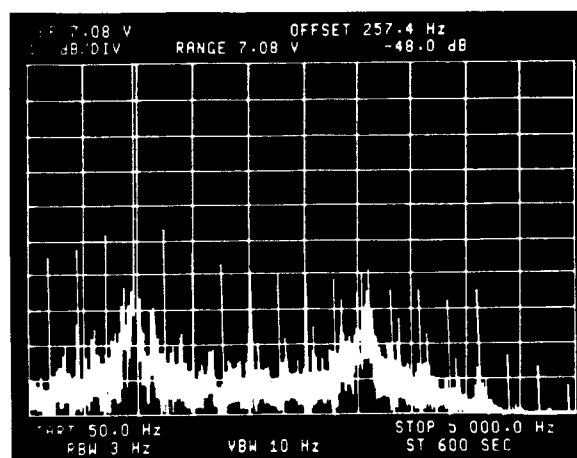


Figure 7b. Output Waveform Spectrum for $F_{OUT} = 1025\text{Hz}$