



ST2349A

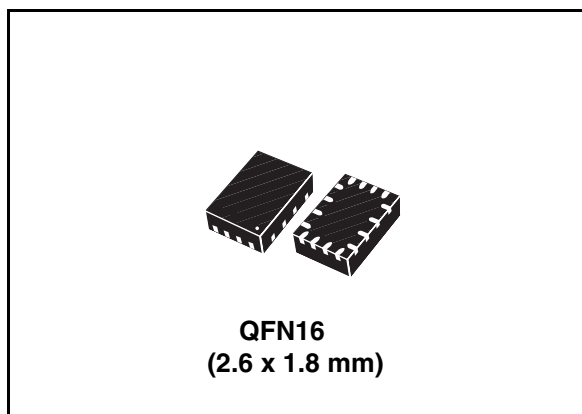
4-bit dual supply level translator without direction control pin

Features

- 18 Mbps (max) data rate when driven by a totem pole driver
- 6.8 Mbps (max) data rate when driven by an open drain pole driver
- Bi-directional level translation without direction control pin
- Wide V_L voltage range of 1.65 to 3.6 V
- Wide V_{CC} voltage range of 1.80 to 5.5 V
- Power down mode feature – when either supply is off, all I/Os are in high impedance
- Low quiescent current (max 8 μ A)
- Able to be driven by totem pole and open drain drivers
- 5.5 V tolerant enable pin
- ESD performance on all pins: ± 2 kV HBM
- Small package and footprint
QFN16 (2.6 x 1.8 mm) package

Applications

- Low voltage system level translation
- Mobile phones and other mobile devices
- I²C level translation
- UART level translation



Description

The ST2349A is a 4-bit dual supply level translator which provides the level shifting capability to allow data transfer in a multi-voltage system. Externally applied voltages, V_{CC} and V_L , set the logic levels on either side of the device. It utilizes transmission gate-based design that allows bi-directional level translation without a control pin.

The ST2349A accepts a V_L from 1.65 to 3.6 V and V_{CC} from 1.80 to 5.5 V, making it ideal for data transfer between low-voltage ASICs/PLD and higher voltage systems. This device has a tri-state output mode which can be used to disable all I/Os.

The ST2349A supports power down mode when V_{CC} is grounded/floating and the device is disabled via the OE pin.

Table 1. Device summary

Order code	Package	Packaging
ST2349AQTR	QFN16 (2.6 x 1.8 mm)	Tape and reel (3000 parts per reel)

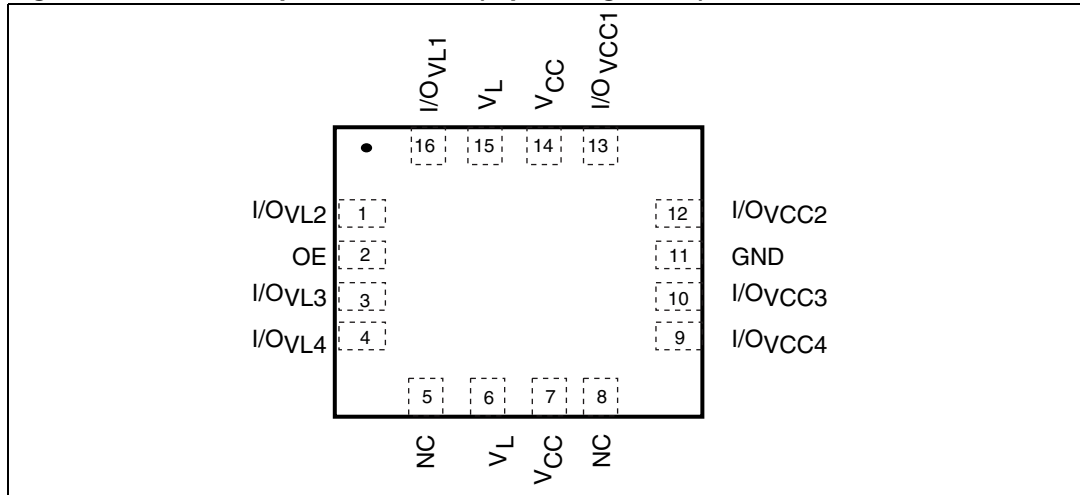
Contents

1	Pin settings	3
1.1	Pin connection	3
1.2	Pin description	3
2	Device block diagrams	4
3	Supplementary notes	5
3.1	Driver requirement	5
3.2	Load driving capability	5
3.3	Power off feature	5
3.4	Truth table	5
4	Maximum rating	6
4.1	Recommended operating conditions	6
5	Electrical characteristics	7
5.1	DC characteristics	7
5.2	AC characteristics	9
5.2.1	Device driven by open drain driver	9
5.2.2	Device driven by totem pole driver	11
6	Test circuit	13
7	Package mechanical data	15
8	Revision history	19

1 Pin settings

1.1 Pin connection

Figure 1. ST2349A pin connection (top through view)



1.2 Pin description

Table 2. ST2349A pin description

Pin number	Symbol	Name and function
1	I/OVL2	Data input/output
2	OE	Output enable
3	I/OVL3	Data input/output
4	I/OVL4	Data input/output
5	NC	No connection
6	VL	Supply voltage
7	VCC	Supply voltage
8	NC	No connection
9	I/OVCC4	Data input/output
10	I/OVCC3	Data input/output
11	GND	Ground
12	I/OVCC2	Data input/output
13	I/OVCC1	Data input/output
14	VCC	Supply voltage
15	VL	Supply voltage
16	I/OVL1	Data input/output

2 Device block diagrams

Figure 2. ST2349A block diagram

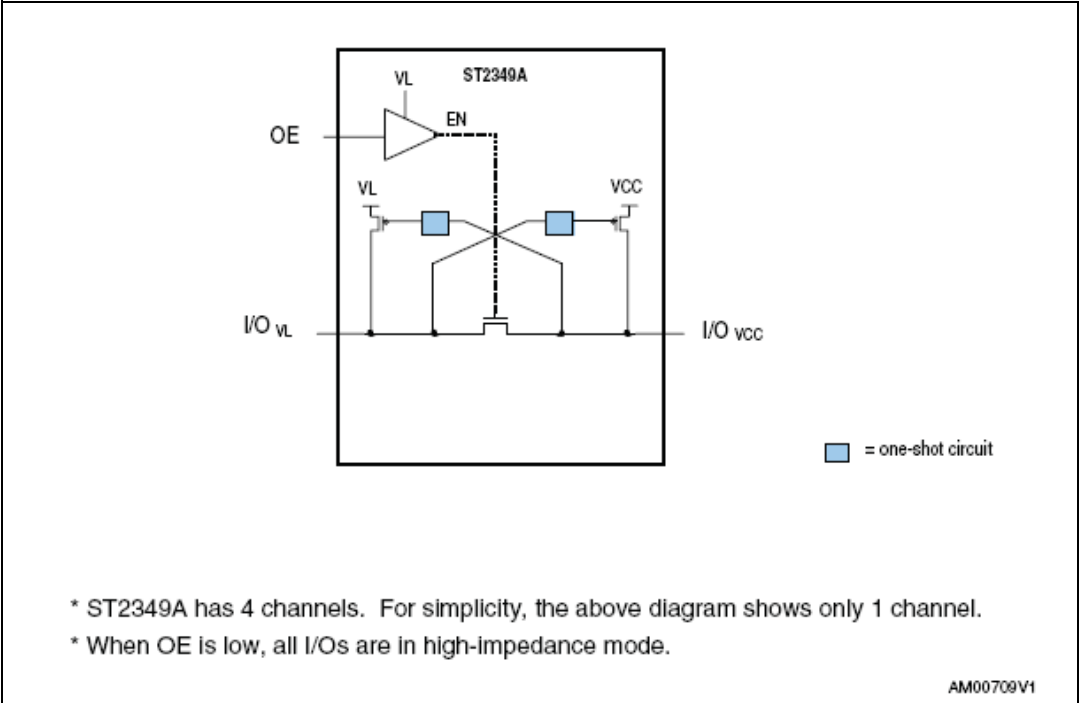
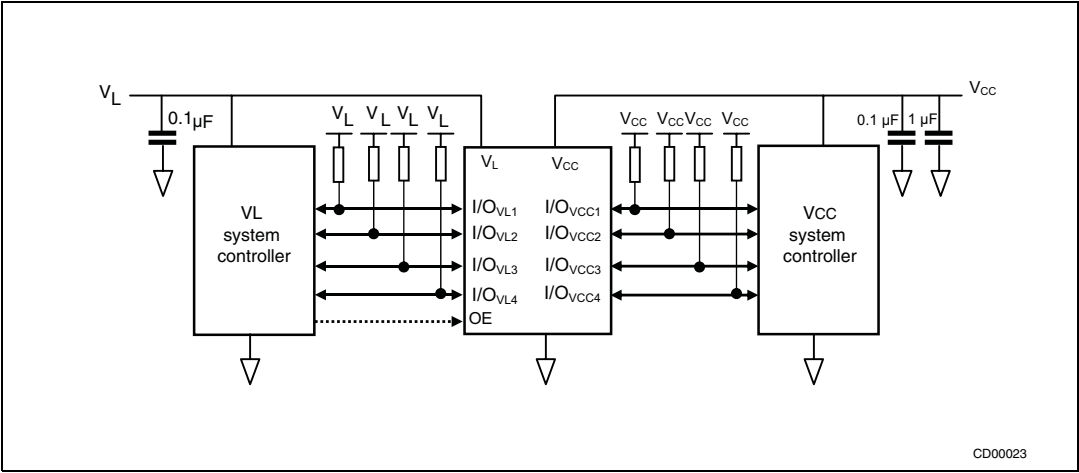


Figure 3. Application block diagram



3 Supplementary notes

3.1 Driver requirement

The ST2349A may be driven by an open drain or totem pole driver and the nature of the device's output is "open drain". It must not be used to drive a pull-down resistor since the impedance of the output at HIGH state depends on the pull-up resistor placed at the I/Os.

As the device has pull-up resistors on both the I/O_{VCC} and I/O_{VL} ports, the user needs to ensure that the driver is able to sink the required amount of current. For example, if the settings are $V_{CC} = 5.5\text{ V}$, $V_L = 4.3\text{ V}$ and the pull-up resistor is $10\text{ k}\Omega$ then the driver must be able to sink at least $(5.5\text{ V}/10\text{ k}\Omega) + (4.3\text{ V}/10\text{ k}\Omega) = 1\text{ mA}$ and still meet the V_{IL} requirements of the ST2349A.

3.2 Load driving capability

To support the open drain system, the one-shot transistor is turned on only during high transition at the output side. When it drives a high state, after the one-shot transistor is turned off, only the pull-up resistor is able to maintain the state. In this case, the resistive load is not recommended.

3.3 Power off feature

In some applications where it might be required to turn off one of the power supplies powering up the level translator, the user may turn off the V_{CC} only when the OE pin is low (device is disabled). There will be no current consumption in V_L due to floating gates or other causes, and the I/Os are in a high-impedance state in this mode.

3.4 Truth table

Table 3. Truth table

Enable	Bi-directional Input/Output	
OE	I/O _{VCC}	I/O _{VL}
H ⁽¹⁾	H ⁽²⁾	H ⁽¹⁾
H ⁽¹⁾	L	L
L	Z ⁽³⁾	Z ⁽³⁾

1. High level V_L power supply referred
2. High level V_{CC} power supply referred
3. Z = high impedance

4 Maximum rating

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_L	Supply voltage	-0.3 to 4.6	V
V_{CC}	Supply voltage	-0.3 to 6.5	V
V_{OE}	DC control input voltage	-0.3 to 6.5	V
$V_{I/OVL}$	DC I/O _{VL} input voltage (OE = GND or V_L)	-0.3 to $V_L + 0.3$	V
$V_{I/OVCC}$	DC I/O _{VCC} input voltage (OE = GND or V_L)	-0.3 to $V_{CC} + 0.3$	V
I_{IK}	DC input diode current	-20	mA
$I_{I/OVL}$	DC output current	±25	mA
$I_{I/OVCC}$	DC output current	±258	mA
I_{SCTOUT}	Short circuit duration, continuous	40	mA
P_D	Power dissipation ⁽¹⁾	500	mW
T_{STG}	Storage temperature	-65 to 150	°C
TL	Lead temperature (10 seconds)	300	°C
ESD	Electrostatic discharge protection (HBM)	±2	kV

1. 500mW: 65 °C derated to 300 mW by 10W/°C: 65 °C to 85 °C

4.1 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_L	Supply voltage	1.65		3.6	V
$V_{CC}^{(1)}$	Supply voltage	1.8		5.5	V
V_{OE}	Input voltage (OE output enable pin, V_L power supply referred)	0		3.6	V
$V_{I/OVL}$	I/O _{VL} voltage	0		V_L	V
$V_{I/OVCC}$	I/O _{VCC} voltage	0		V_{CC}	V
T_{op}	Operating temperature	-40		85	°C
dt/dV	Input rise and fall time	0		1	ns/V

1. V_{CC} must be greater than V_L .

5 Electrical characteristics

5.1 DC characteristics

Over recommended operating conditions unless otherwise noted. All typical values are at $T_A = 25\text{ }^{\circ}\text{C}$.

Table 6. DC characteristics

Symbol	Parameter	V _L	V _{CC}	Test conditions	Value					Unit
					T _A = 25 °C			-40 to 85 °C		
					Min	Typ	Max	Min	Max	
V _{IHL}	High level input voltage (I/O _{VL})	1.65	V _L to 5.5	—	1.4	—	—	1.4	—	V
		2.0			1.6	—	—	1.6	—	
		2.5			2.0	—	—	2.0	—	
		3.0			2.4	—	—	2.4	—	
		3.6			2.8	—	—	2.8	—	
V _{ILL}	Low level input voltage (I/O _{VL})	1.65	V _L to 5.5	—	—	—	0.3	—	0.3	V
		2.0			—	—	0.4	—	0.4	
		2.5			—	—	0.5	—	0.5	
		3.0			—	—	0.6	—	0.6	
		3.6			—	—	0.8	—	0.8	
V _{IHC}	High level input voltage (I/O _{VCC})	1.65 to V _{CC}	1.8	—	1.6	—	—	1.6	—	V
			2.5		2.3	—	—	2.3	—	
			3.0		2.7	—	—	2.7	—	
			3.6		3.3	—	—	3.3	—	
			4.3		3.5	—	—	3.5	—	
			5.5		4.2	—	—	4.2	—	
V _{ILC}	Low level input voltage (I/O _{VCC})	1.65 - 2.5	3 - 5.5	—	—	—	—	0.3	—	V
		2.7 - 3.6	3.6 - 5.5		—	—	—	0.5	—	
V _{IH-OE}	High level input voltage (OE)	1.65	V _L to 5.5	—	1.0	—	—	1.0	—	V
		2.0			1.2	—	—	1.2	—	
		2.5			1.4	—	—	1.4	—	
		3.0			1.6	—	—	1.6	—	
		3.6			2.0	—	—	2.0	—	

Table 6. DC characteristics (continued)

Symbol	Parameter	V _L	V _{CC}	Test conditions	Value					Unit
					T _A = 25 °C			-40 to 85 °C		
					Min	Typ	Max	Min	Max	
V _{IL-OE}	Low level input voltage (OE)	1.65	V _L to 5.5	—	—	—	0.33	—	0.33	V
		2.0			—	—	0.40	—	0.40	
		2.5			—	—	0.50	—	0.50	
		3.0			—	—	0.60	—	0.60	
		3.6			—	—	0.75	—	0.75	
V _{OLL}	Low level output voltage (I/O _{VL})	1.65 to 3.6	V _L to 5.5	IO = 1.0 mA I/O _{VCC} ≤ 0.15 V	—	—	0.40	—	0.40	V
V _{OLC}	Low level output voltage (I/O _{VCC})	1.65 to 3.6	V _L to 5.5	IO = 1.0 mA I/O _{VL} ≤ 0.15 V	—	—	0.40	—	0.40	V
I _{OE}	Control input leakage current (OE)	1.65 to 3.6	V _L to 5.5	V _{OE} = GND or V _L	—	—	±0.1	—	±0.1	µA
I _{IO_LKG}	High impedance leakage current (I/O _{VL} , I/O _{VCC})	1.65 to 3.6	V _L to 5.5	OE = GND	—	—	±0.1	—	±0.1	µA
I _{QVCC}	Quiescent supply current V _{CC}	1.65 to 3.6	V _L to 5.5	only pull-up resistor connected to I/O	—	6	6.5	—	8	µA
I _{QVL}	Quiescent supply current V _L	1.65 to 3.6	V _L to 5.5	only pull-up resistor connected to I/O	—	0.01	0.1	—	1	µA
I _{Z-VCC}	High impedance quiescent supply current V _{CC}	1.65 to 3.6	V _L to 5.5	OE = GND; only pull-up resistor connected to I/O	—	6	6.5	—	8	µA
I _{Z-VL}	High impedance quiescent supply current V _L	1.65 to 3.6	V _L to 5.5	OE = GND; only pull-up resistor connected to I/O	—	0.01	0.1	—	1	µA

5.2 AC characteristics

5.2.1 Device driven by open drain driver

Load $C_L = 15 \text{ pF}$; $R_{up} = 4.7 \text{ k}\Omega$; driver $t_r = t_f \leq 2 \text{ ns}$ over temperature range -40°C to 85°C .

Table 7. AC characteristics - test conditions: $V_L = 1.65 - 1.8 \text{ V}$

Symbol	Parameter		$V_{CC} = 1.8 - 2.5 \text{ V}$		$V_{CC} = 2.7 - 3.6 \text{ V}$		$V_{CC} = 4.3 - 5.5 \text{ V}$		Unit
			Min	Max	Min	Max	Min	Max	
t_{RVCC}	Rise time I/O_{VCC}		—	80	—	60	—	45	ns
t_{FVCC}	Fall time I/O_{VCC}		—	23.2	—	33.9	—	53.3	ns
t_{RVL}	Rise time I/O_{VL}		—	60	—	45	—	35	ns
t_{FVL}	Fall time I/O_{VL}		—	16.4	—	17.6	—	16.9	ns
$t_{I/OVL-VCC}$	Propagation delay time I/O_{VL-LH} to I/O_{VCC-LH} I/O_{VL-HL} to I/O_{VCC-HL}	t_{PLH}	—	3.4	—	2.0	—	2.0	ns
		t_{PHL}	—	13.9	—	19.1	—	30.2	ns
$t_{I/OVCC-VL}$	Propagation delay time I/O_{VCC-LH} to I/O_{VL-LH} I/O_{VCC-HL} to I/O_{VL-LH}	t_{PLH}	—	2.0	—	2.0	—	2.6	ns
		t_{PHL}	—	8.6	—	9.0	—	9.5	ns
$t_{PZL} \ t_{PZH}$ $t_{PLZ} \ t_{PHZ}$	Output enable and disable time	En	—	10	—	10	—	10	ns
		Dis	—	40	—	40	—	40	ns
D_R	Data rate ⁽¹⁾		—	1.8	—	2.2	—	3.4	MHz

1. The data rate is guaranteed based on the condition that the output I/O signal rise/fall time is less than 15% of the input I/O signal period; the input I/O signal is at 50% duty cycle and the output I/O signal duty cycle deviation not less than 30%.

Table 8. AC characteristics - test conditions: $V_L = 2.5 - 2.7 \text{ V}$

Symbol	Parameter		$V_{CC} = 2.7 - 3.6 \text{ V}$		$V_{CC} = 4.3 - 5.5 \text{ V}$		Unit
			Min	Max	Min	Max	
t_{RVCC}	Rise time I/O_{VCC}		—	70.0	—	50	ns
t_{FVCC}	Fall time I/O_{VCC}		—	14.8	—	19.1	ns
t_{RVL}	Rise time I/O_{VL}		—	50.0	—	35	ns
t_{FVL}	Fall time I/O_{VL}		—	9.8	—	10	ns
$t_{I/OVL-VCC}$	Propagation delay time I/O_{VL-LH} to I/O_{VCC-LH} I/O_{VL-HL} to I/O_{VCC-HL}	t_{PLH}	—	2.0	—	2.0	ns
		t_{PHL}	—	8.2	—	11.6	ns
$t_{I/OVCC-VL}$	Propagation delay time I/O_{VCC-LH} to I/O_{VL-LH} I/O_{VCC-HL} to I/O_{VL-LH}	t_{PLH}	—	2.0	—	2.0	ns
		t_{PHL}	—	5.3	—	5.9	ns

Table 8. AC characteristics - test conditions: $V_L = 2.5 - 2.7$ V (continued)

Symbol	Parameter		$V_{CC} = 2.7 - 3.6$ V		$V_{CC} = 4.3 - 5.5$ V		Unit
			Min	Max	Min	Max	
t_{PZL} t_{PZH} t_{PLZ} t_{PHZ}	Output enable and disable time	En	—	6	—	6	ns
		Dis	—	40	—	40	ns
D_R	Data rate ⁽¹⁾		—	2.2	—	3.0	MHz

1. The data rate is guaranteed based on the condition that the output I/O signal rise/fall time is less than 15% of the input I/O signal period; the input I/O signal is at 50% duty cycle and the output I/O signal duty cycle deviation not less than 30%.

Table 9. AC characteristics - test conditions: $V_L = 2.7 - 3.6$ V

Symbol	Parameter		V _{CC} = 4.3 – 5.5 V		Unit
			Min	Max	
t _{RVCC}	Rise time I/O _{VCC}		—	55.0	ns
t _{FVCC}	Fall time I/O _{VCC}		—	17.2	ns
t _{RVL}	Rise time I/O _{VL}		—	40.0	ns
t _{FVL}	Fall time I/O _{VL}		—	9.7	ns
t _{I/OVL-VCC}	Propagation delay time I/O _{VL} -LH to I/O _{VCC} -LH I/O _{VL} -HL to I/O _{VCC} -HL	t _{PLH}	—	2.0	ns
		t _{PHL}	—	10.6	ns
t _{I/OVCC-VL}	Propagation delay time I/O _{VCC} -LH to I/O _{VL} -LH I/O _{VCC} -HL to I/O _{VL} -HL	t _{PLH}	—	2.0	ns
		t _{PHL}	—	4.8	ns
t _{PZL} t _{PZH} t _{PLZ} t _{PHZ}	Output enable and disable time	En	—	6	ns
		Dis	—	40	ns
D _R	Data rate ⁽¹⁾	—	—	3.0	MHz

1. The data rate is guaranteed based on the condition that the output I/O signal rise/fall time is less than 15% of the input I/O signal period; the input I/O signal is at 50% duty cycle and the output I/O signal duty cycle deviation not less than 30%.

5.2.2 Device driven by totem pole driver

Load $C_L = 15 \text{ pF}$; $R_{up} = 10 \text{ k}\Omega$; driver $t_r = t_f \leq 2 \text{ ns}$ over temperature range -40°C to 85°C .

Table 10. AC characteristics - test conditions: $V_L = 1.65 - 1.8 \text{ V}$

Symbol	Parameter		$V_{CC} = 1.8 - 2.5 \text{ V}$		$V_{CC} = 2.7 - 3.6 \text{ V}$		$V_{CC} = 4.3 - 5.5 \text{ V}$		Unit
			Min	Max	Min	Max	Min	Max	
t_{RVCC}	Rise time I/O_{VCC}		—	7.2	—	4.6	—	1.4	ns
t_{FVCC}	Fall time I/O_{VCC}		—	23.2	—	33.9	—	53.3	ns
t_{RVL}	Rise time I/O_{VL}		—	5.9	—	5.7	—	5.5	ns
t_{FVL}	Fall time I/O_{VL}		—	16.4	—	17.6	—	16.9	ns
$t_{I/OVL-VCC}$	Propagation delay time I/O_{VL-LH} to I/O_{VCC-LH} I/O_{VL-HL} to I/O_{VCC-HL}	t_{PLH}	—	5.5	—	4.1	—	3.6	ns
		t_{PHL}	—	13.9	—	19.1	—	30.2	ns
$t_{I/OVCC-VL}$	Propagation delay time I/O_{VCC-LH} to I/O_{VL-LH} I/O_{VCC-HL} to I/O_{VL-HL}	t_{PLH}	—	4.5	—	3.9	—	3.6	ns
		t_{PHL}	—	8.6	—	9	—	9.5	ns
$t_{PZL} \ t_{PZH}$ $t_{PLZ} \ t_{PHZ}$	Output enable and disable time	En	—	10	—	10	—	10	ns
		Dis	—	40	—	40	—	40	ns
D_R	Data rate ⁽¹⁾		—	6.4	—	4.5	—	3	MHz

1. The data rate is guaranteed based on the condition that the output I/O signal rise/fall time is less than 15% of the input I/O signal period; the input I/O signal is at 50% duty cycle and the output I/O signal duty cycle deviation not less than 30%.

Table 11. AC characteristics - test conditions: $V_L = 2.5 - 2.7 \text{ V}$

Symbol	Parameter		$V_{CC} = 2.7 - 3.6 \text{ V}$		$V_{CC} = 4.3 - 5.5 \text{ V}$		Unit
			Min	Max	Min	Max	
t_{RVCC}	Rise time I/O_{VCC}		—	3.8	—	2.8	ns
t_{FVCC}	Fall time I/O_{VCC}		—	14.8	—	19.1	ns
t_{RVL}	Rise time I/O_{VL}		—	3.3	—	3.2	ns
t_{FVL}	Fall time I/O_{VL}		—	9.8	—	10.0	ns
$t_{I/OVL-VCC}$	Propagation delay time I/O_{VL-LH} to I/O_{VCC-LH} I/O_{VL-HL} to I/O_{VCC-HL}	t_{PLH}	—	3.2	—	2.8	ns
		t_{PHL}	—	8.2	—	11.6	ns

Table 11. AC characteristics - test conditions: $V_L = 2.5 - 2.7$ V (continued)

Symbol	Parameter		$V_{CC} = 2.7 - 3.6$ V		$V_{CC} = 4.3 - 5.5$ V		Unit
			Min	Max	Min	Max	
$t_{I/OVCC-VL}$	Propagation delay time I/O _{VCC-LH} to I/O _{VL-LH} I/O _{VCC-HL} to I/O _{VL-HL}	t_{PLH}	—	2.6	—	2.0	ns
							ns
		t_{PHL}	—	5.3	—	5.9	ns
							ns
t_{PZL} t_{PZH} t_{PLZ} t_{PHZ}	Output enable and disable time	En	—	6	—	6	ns
		Dis	—	40	—	40	ns
D_R	Data rate ⁽¹⁾		—	9	—	6.8	MHz

1. The data rate is guaranteed based on the condition that the output I/O signal rise/fall time is less than 15% of the input I/O signal period; the input I/O signal is at 50% duty cycle and the output I/O signal duty cycle deviation not less than 30%.

Table 12. AC characteristics - test conditions: $V_L = 2.7 - 3.6$ V

Symbol	Parameter		$V_{CC} = 4.3 - 5.5$ V		Unit
			Min	Max	
t_{RVCC}	Rise time I/O _{VCC}		—	2.9	ns
t_{FVCC}	Fall time I/O _{VCC}		—	17.2	ns
t_{RVL}	Rise time I/O _{VL}		—	3.0	ns
t_{FVL}	Fall time I/O _{VL}		—	9.7	ns
$t_{I/OVL-VCC}$	Propagation delay time I/O _{VL-LH} to I/O _{VCC-LH} I/O _{VL-HL} to I/O _{VCC-HL}	t_{PLH}	—	2.7	ns
		t_{PHL}	—	10.6	ns
$t_{I/OVCC-VL}$	Propagation delay time I/O _{VCC-LH} to I/O _{VL-LH} I/O _{VCC-HL} to I/O _{VL-HL}	t_{PLH}	—	1.9	ns
					ns
		t_{PHL}	—	4.8	ns
					ns
t_{PZL} t_{PZH} t_{PLZ} t_{PHZ}	Output enable and disable time	En	—	6	ns
		Dis	—	40	ns
D_R	Data rate ⁽¹⁾		—	7.2	MHz

1. The data rate is guaranteed based on the condition that the output I/O signal rise/fall time is less than 15% of the input I/O signal period; the input I/O signal is at 50% duty cycle and the output I/O signal duty cycle deviation not less than 30%.

6 Test circuit

Figure 4. Test circuit

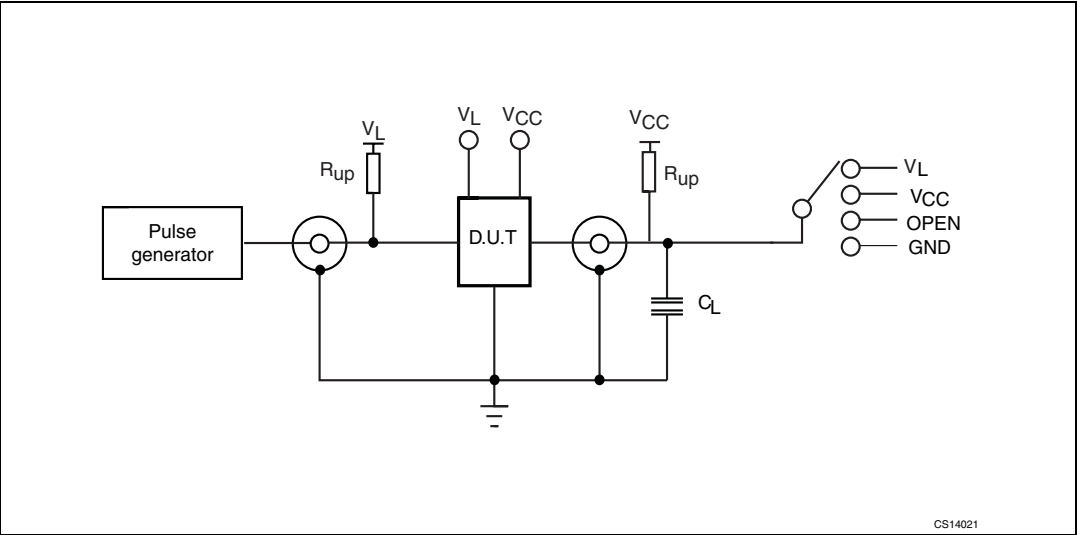


Table 13. Test circuit switches

Test	Switch		
	Driving I/O _{V_L}	Driving I/O _{V_{CC}}	Open drain driving
t _{PLH} , t _{PHL}	Open	Open	Open

Table 14. Waveform symbol value

Symbol	Driving I/O _{VL}		Driving I/O _{VCC}	
	$1.8\text{ V} \leq V_L \leq V_{CC} \leq 2.5\text{ V}$	$3.3\text{ V} \leq V_L \leq V_{CC} \leq 5.0\text{ V}$	$1.8\text{ V} \leq V_L \leq V_{CC} \leq 2.5\text{ V}$	$3.3\text{ V} \leq V_L \leq V_{CC} \leq 5.0\text{ V}$
V _{IH}	V _L	V _L	V _{CC}	V _{CC}
V _{IM}	50% V _L	50% V _L	50% V _{CC}	50% V _{CC}
V _{OM}	50% V _{CC}	50% V _{CC}	50% V _L	50% V _L
V _X	V _{OL} + 0.15V	V _{OL} + 0.3V	V _{OL} + 0.15V	V _{OL} + 0.3V
V _Y	V _{OH} - 0.15V	V _{OH} - 0.3V	V _{OH} - 0.15V	V _{OH} - 0.3V

Figure 5. Waveform - propagation delay (f = 1 MHz; 50% duty cycle)

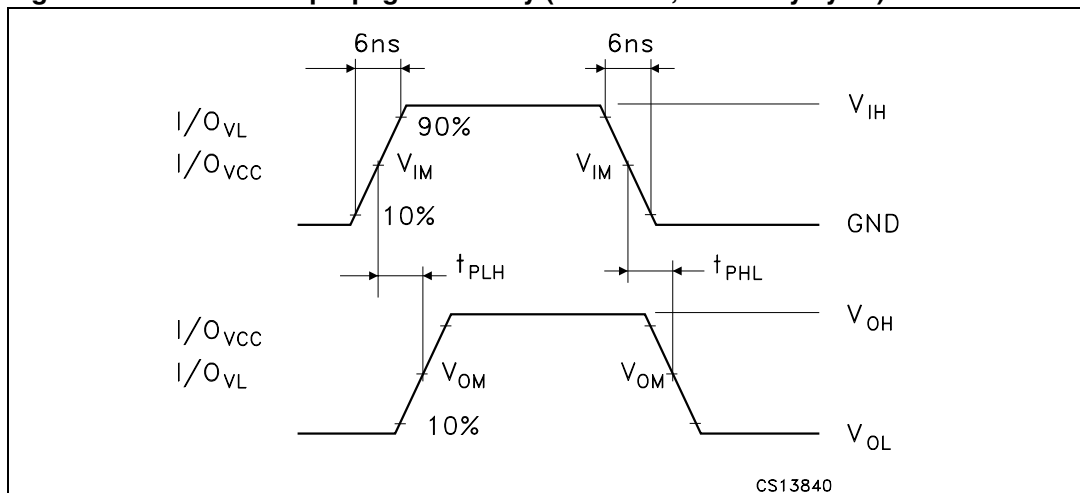
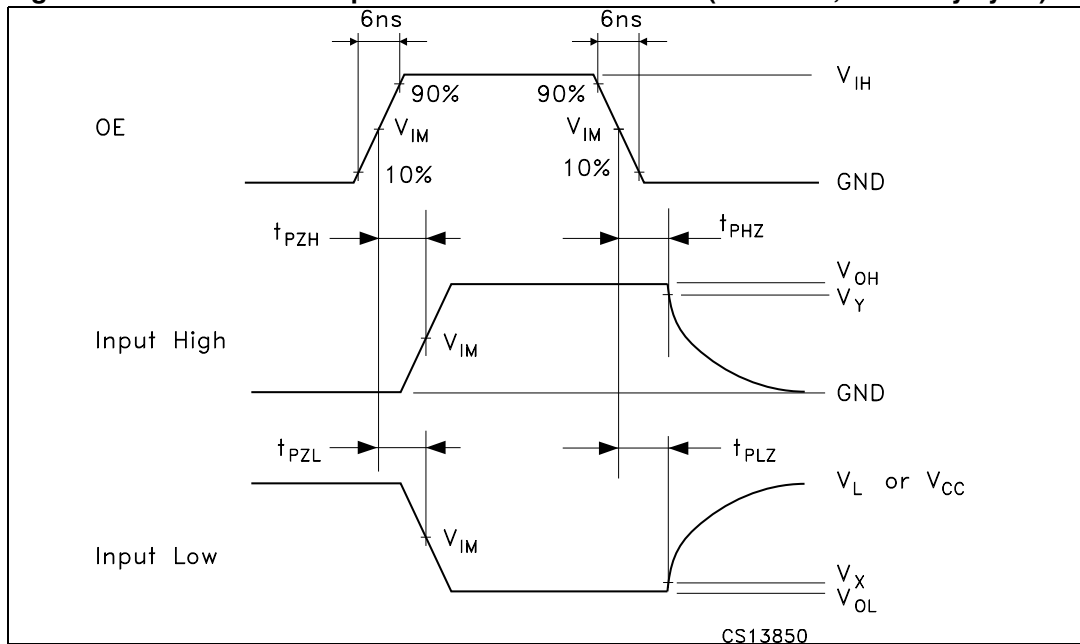


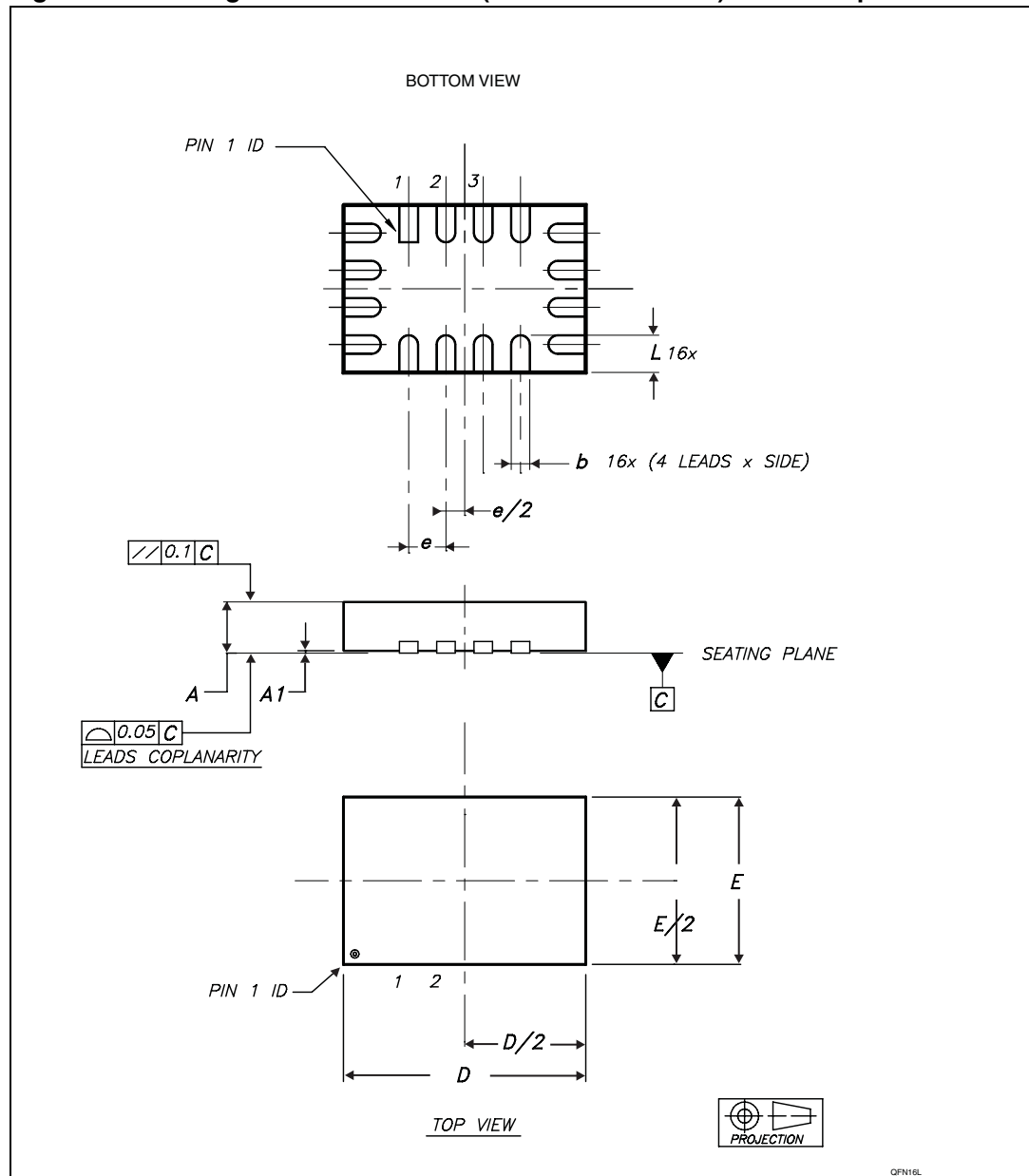
Figure 6. Waveform - output enable and disable time (f = 1 MHz; 50% duty cycle)



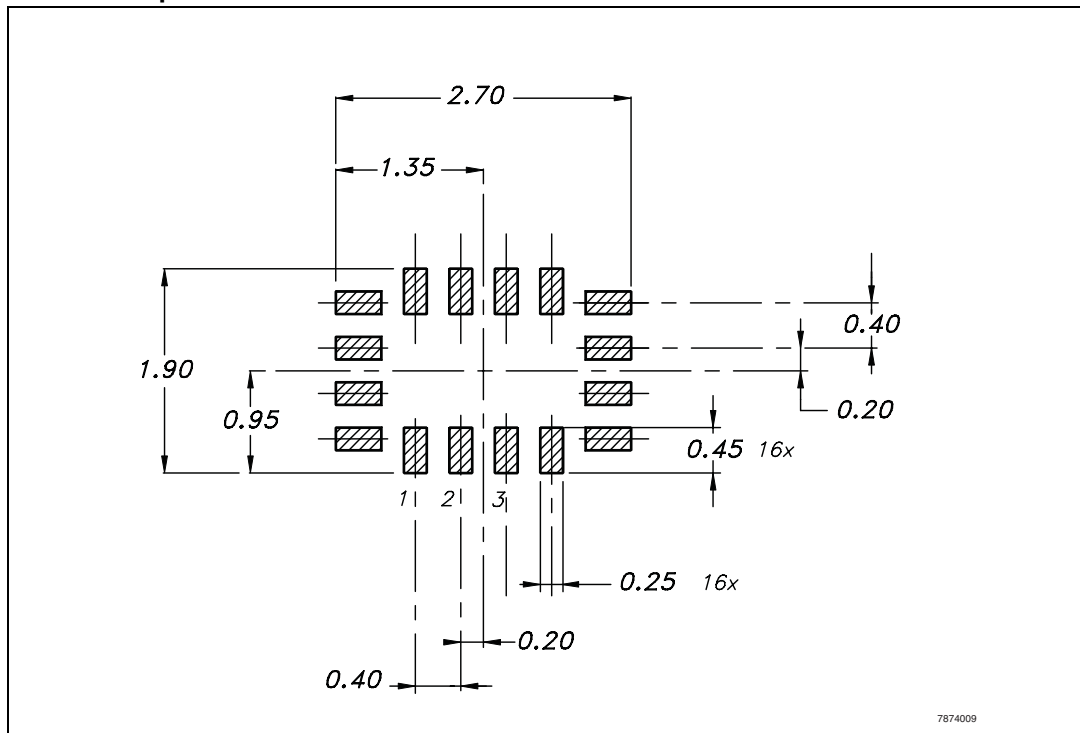
7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 7. Package outline for QFN16 (2.6 x 1.8 x 0.55 mm) - 0.40 mm pitch



1. Drawing not to scale.
2. Dimensions are in millimeters.



- <

Figure 9. Carrier tape for QFN16 (2.6 x 1.8 x 0.55 mm) - 0.40 mm pitch

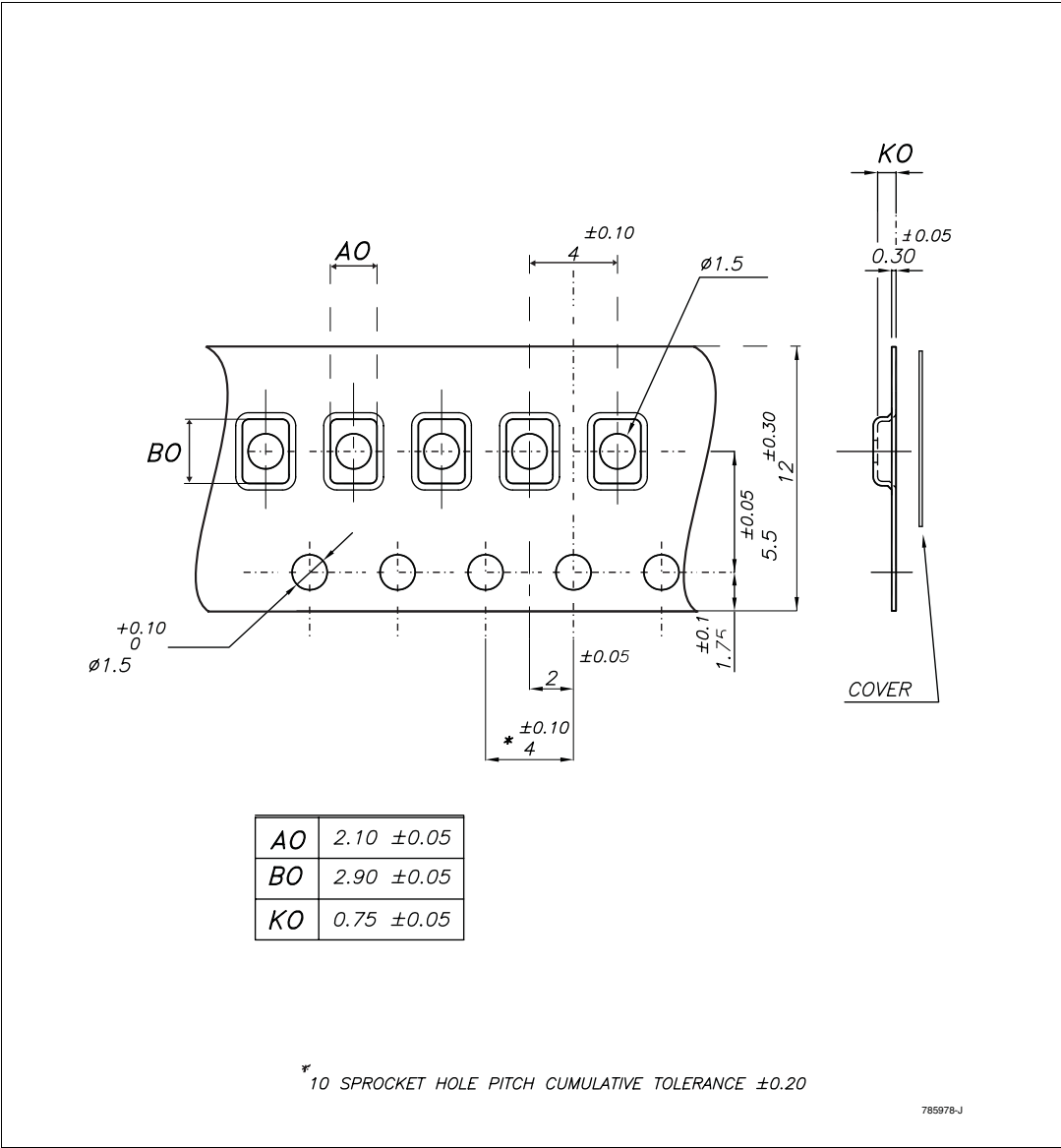
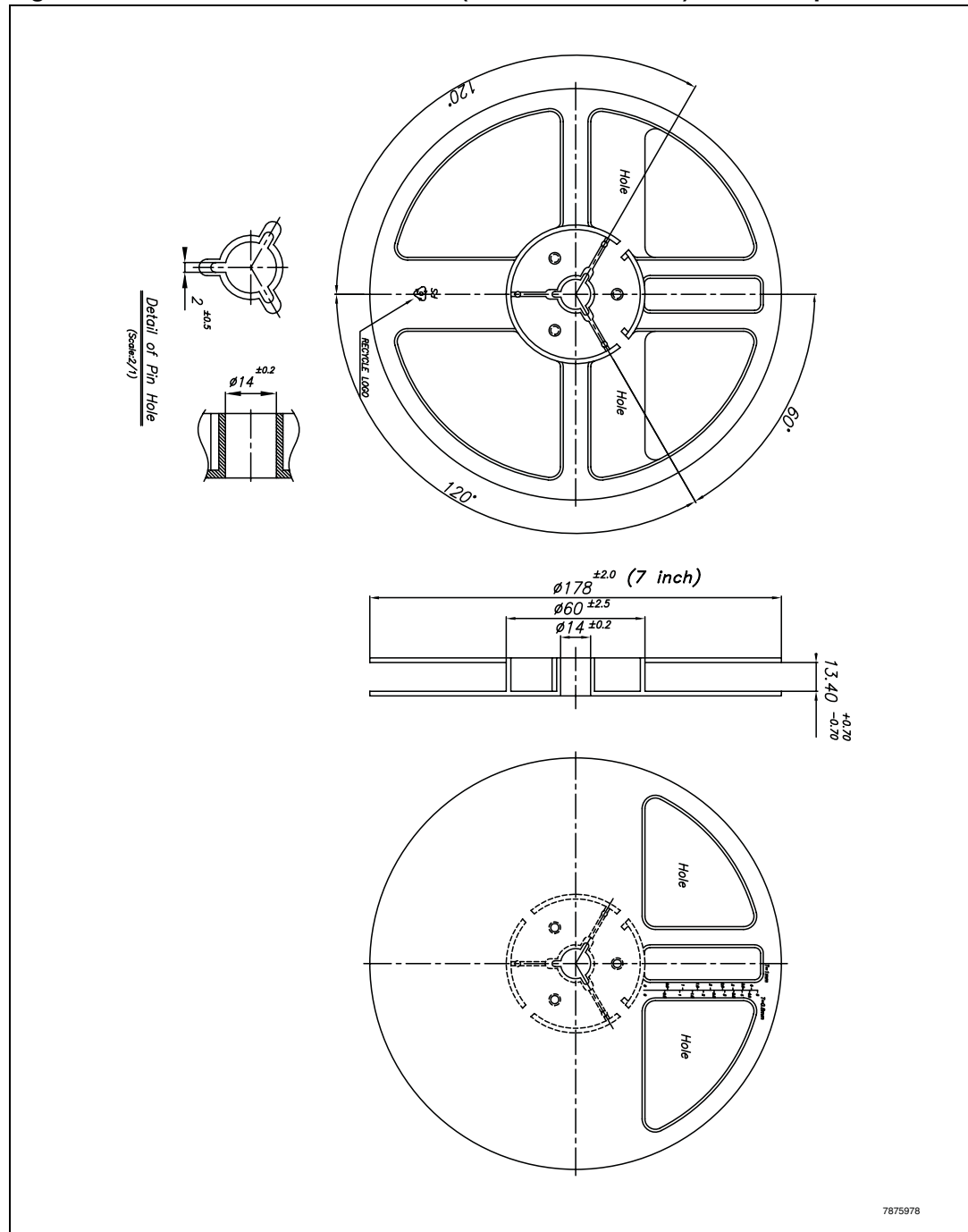


Figure 10. Reel information for QFN16 (2.6 x 1.8 x 0.55 mm) - 0.40 mm pitch



1. Drawing not to scale.
2. Dimensions are in millimeters

8 Revision history

Table 16. Document revision history

Date	Revision	Changes
16-Jul-2008	1	Initial release.
22-Jun-2009	2	Document status promoted from Preliminary data to datasheet. Content reworked to improve readability. Updated: Table 7 on page 9 , Table 8 on page 9 , Table 9 on page 10 , Table 10 on page 11 , Table 11 on page 11 and Table 12 on page 12 . Modified: ECOPACK information.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2009 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com