

MC74HC574A

Octal 3-State Noninverting D Flip-Flop

High-Performance Silicon-Gate CMOS

The MC74HC574A is identical in pinout to the LS574. The device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

Data meeting the set-up time is clocked to the outputs with the rising edge of the Clock. The Output Enable input does not affect the states of the flip-flops but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be stored even when the outputs are not enabled.

The HC574A is identical in function to the HC374A but has the flip-flop inputs on the opposite side of the package from the outputs to facilitate PC board layout.

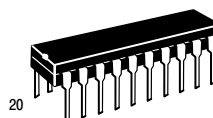
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 266 FETs or 66.5 Equivalent Gates



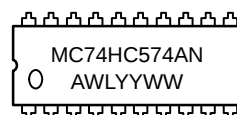
ON Semiconductor

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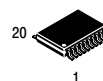
MARKING DIAGRAMS



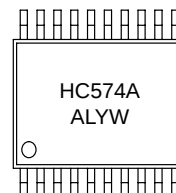
PDIP-20
N SUFFIX
CASE 783



SO-20
DW SUFFIX
CASE 751D



TSSOP-20
DT SUFFIX
CASE 948E



A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC74HC574AN	PDIP-20	1440/Box
MC74HC574ADW	SOIC-WIDE	38/Rail
MC74HC574ADWR2	SOIC-WIDE	1000/Reel
MC74HC574ADT	TSSOP-20	75/Rail
MC74HC574ADTR2	TSSOP-20	2500/Reel

MC74HC574A

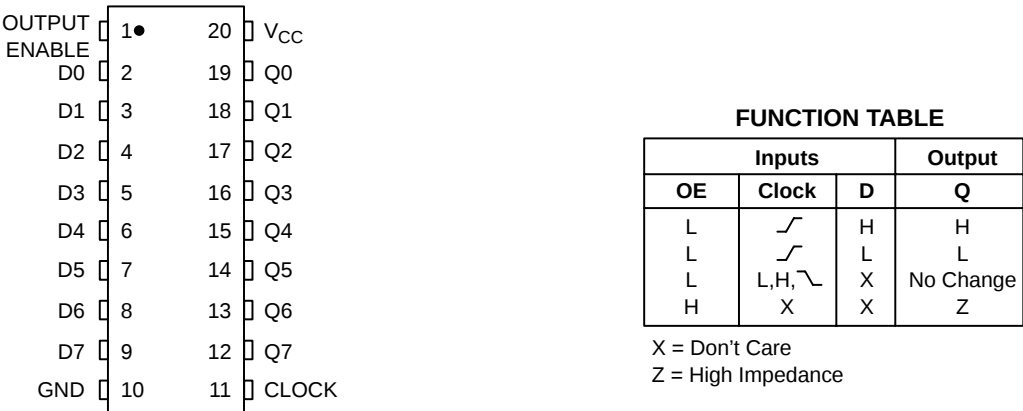


Figure 1. Pin Assignment

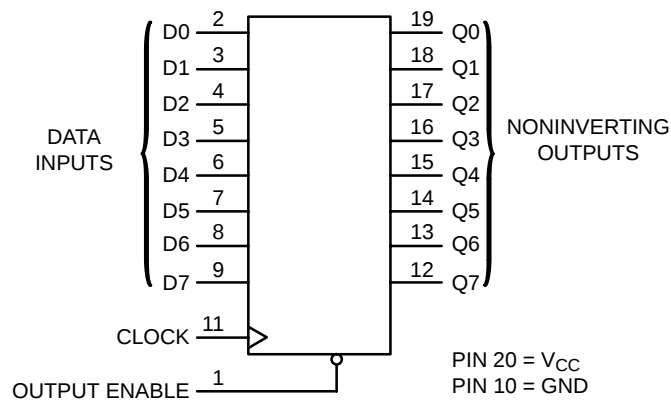


Figure 2. Logic Diagram

Design Criteria	Value	Units
Internal Gate Count*	66.5	ea.
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	μW
Speed Power Product	0.0075	pJ

*Equivalent to a two-input NAND gate.

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MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	− 0.5 to + 7.0	V
V _I	DC Input Voltage	− 0.5 to V _{CC} + 0.5	V
V _O	DC Output Voltage (Note 2)	− 0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 35	mA
I _O	DC Output Sink Current	± 35	mA
I _{CC}	DC Supply Current per Supply Pin	± 75	mA
I _{GND}	DC Ground Current per Ground Pin	± 75	mA
T _{STG}	Storage Temperature Range	− 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction Temperature under Bias	+ 150	°C
θ _{JA}	Thermal Resistance PDIP SOIC TSSOP	67 96 128	°C/W
P _D	Power Dissipation in Still Air at 85°C PDIP SOIC TSSOP	750 500 450	mW
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Index: 30% – 35%	UL–94–VO (0.125 in)	
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5)	>4000 >300 >1000	V
I _{Latch–Up}	Latch–Up Performance Above V _{CC} and Below GND at 85°C (Note 6)	± 300	mA

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Extended exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum–rated conditions is not implied.
2. I_O absolute maximum rating must be observed.
3. Tested to EIA/JESD22–A114–A.
4. Tested to EIA/JESD22–A115–A.
5. Tested to JESD22–C101–A.
6. Tested to EIA/JESD78.
7. For high frequency or heavy load considerations, see the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _I , V _O	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C
t _r , t _f	Input Rise and Fall Time (Figure 3) V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

8. Unused inputs may not be left open. All inputs must be tied to a high– or low–logic input voltage level.

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High–Level Input Voltage	V _{out} = V _{CC} – 0.1 V I _{out} ≤ 20 µA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V _{IL}	Maximum Low–Level Input Voltage	V _{out} = 0.1 V I _{out} ≤ 20 µA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V _{OH}	Minimum High–Level Output Voltage	V _{in} = V _{IH} I _{out} ≤ 20 µA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
V _{OH}	Minimum High–Level Output Voltage	V _{in} = V _{IH} I _{out} ≤ 2.4 mA I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	V
V _{OL}	Maximum Low–Level Output Voltage	V _{in} = V _{IL} I _{out} ≤ 20 µA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V _{in} = V _{IL} I _{out} ≤ 2.4 mA I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	µA
I _{OZ}	Maximum Three–State Leakage Current	Output in High–Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	6.0	± 0.5	± 5.0	± 10	µA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 µA	6.0	4.0	40	160	µA

9. Information on typical parametric values can be found in the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

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AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF; Input t_r = t_f = 6.0 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			– 55 to 25 °C	≤ 85 °C	≤ 125 °C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 3 and 6)	2.0 3.0 4.5 6.0	6.0 15 30 35	4.8 10 24 28	4.0 8.0 20 24	MHz
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q (Figures 3 and 6)	2.0 3.0 4.5 6.0	160 105 32 27	200 145 40 34	240 190 48 41	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 4 and 7)	2.0 3.0 4.5 6.0	150 100 30 26	190 125 38 33	225 150 45 38	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 4 and 7)	2.0 3.0 4.5 6.0	140 90 28 24	175 120 35 30	210 140 42 36	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, any Output (Figures 3 and 6)	2.0 3.0 4.5 6.0	60 27 12 10	75 32 15 13	90 36 18 15	ns
C _{in}	Maximum Input Capacitance		10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance, Output in High-Impedance State		15	15	15	pF

10. For propagation delays with loads other than 50 pF, and information on typical parametric values, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

C _{PD}	Power Dissipation Capacitance (Per Enabled Output)*	Typical @ 25°C, V _{CC} = 5.0 V	pF
		24	

*Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}. For load considerations, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (C_L = 50 pF; Input t_r = t_f = 6.0 ns)

Symbol	Parameter	Figure	V _{CC} Volts	Guaranteed Limit						Unit
				– 55 to 25°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
t _{su}	Minimum Setup Time, Data to Clock	5	2.0 3.0 4.6 6.0	50 40 10 9.0	 	65 50 13 11	 	75 60 15 13	 	ns
t _h	Minimum Hold Time, Clock to Data	5	2.0 3.0 4.5 6.0	5.0 5.0 5.0 5.0	 	5.0 5.0 5.0 5.0	 	5.0 5.0 5.0 5.0	 	ns
t _w	Minimum Pulse Width, Clock	3	2.0 3.0 4.5 6.0	75 60 15 13	 	95 80 19 16	 	110 90 22 19	 	ns
t _r , t _f	Maximum Input Rise and Fall Times	3	2.0 3.0 4.5 6.0	 	1000 800 500 400	 	1000 800 500 400	 	1000 800 500 400	ns

SWITCHING WAVEFORMS

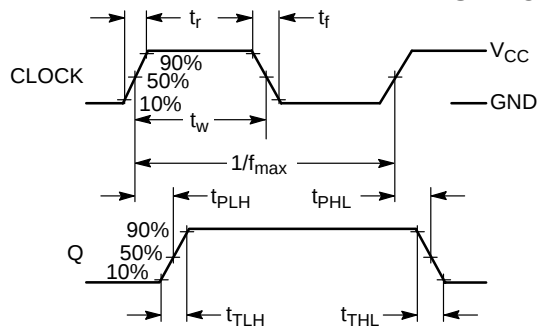


Figure 3.

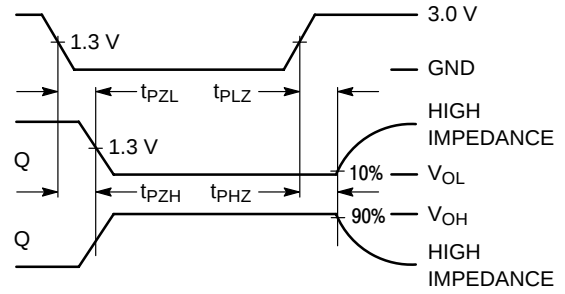


Figure 4.

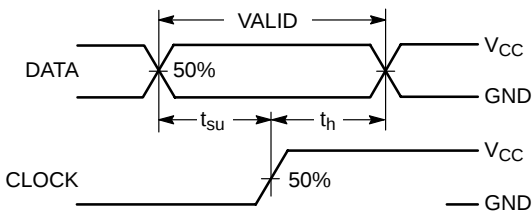
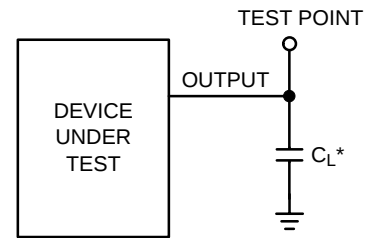
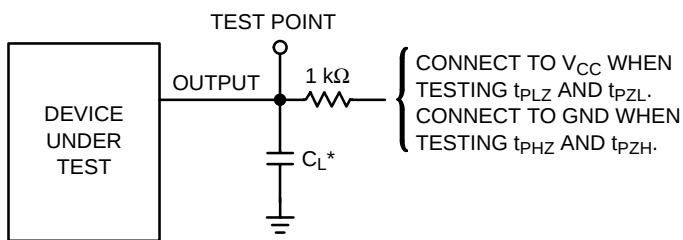


Figure 5.



*Includes all probe and jig capacitance.

Figure 6.



*Includes all probe and jig capacitance.

Figure 7. Test Circuit

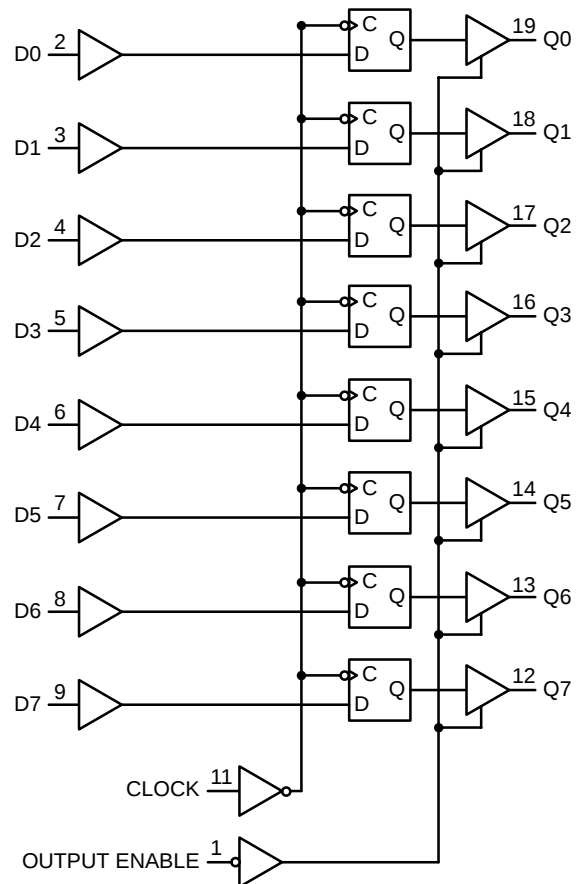
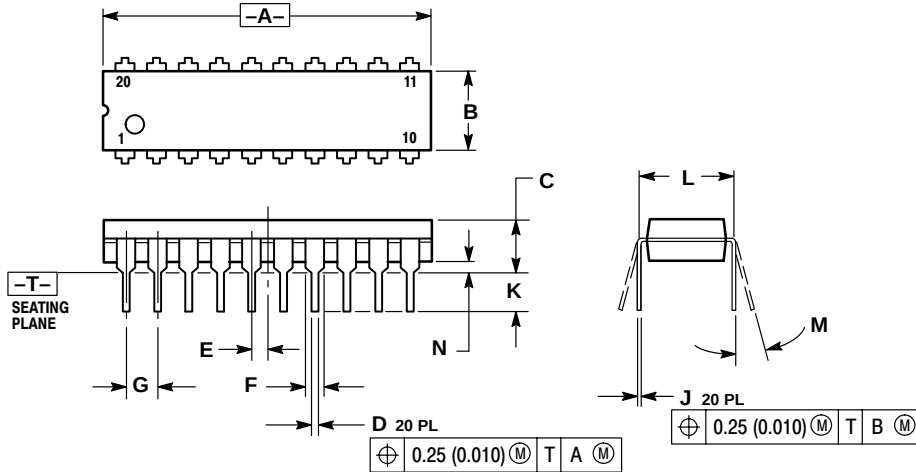


Figure 8. Expanded Logic Diagram

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PACKAGE DIMENSIONS

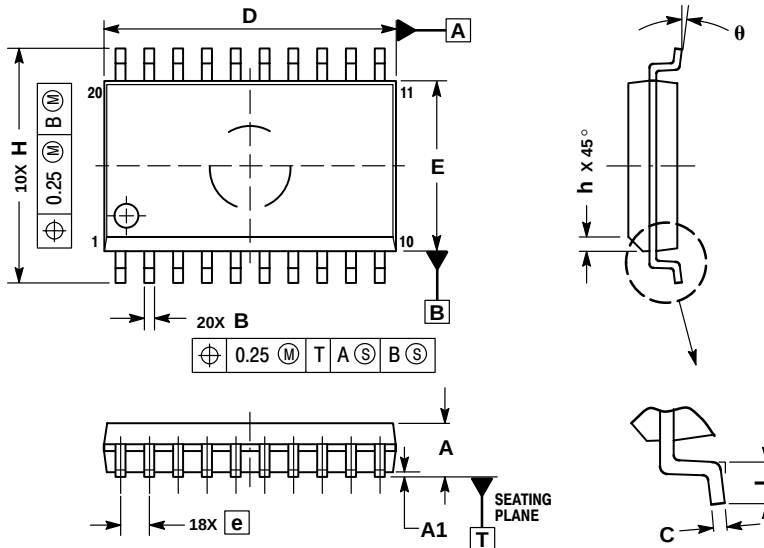
PDIP-20
N SUFFIX
PLASTIC DIP PACKAGE
CASE 738-03
ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
J	0.110	0.140	2.80	3.55
K	0.300 BSC		7.62 BSC	
L	0°	15°	0°	15°
M	0.020	0.040	0.51	1.01

SO-20
DW SUFFIX
CASE 751D-05
ISSUE F



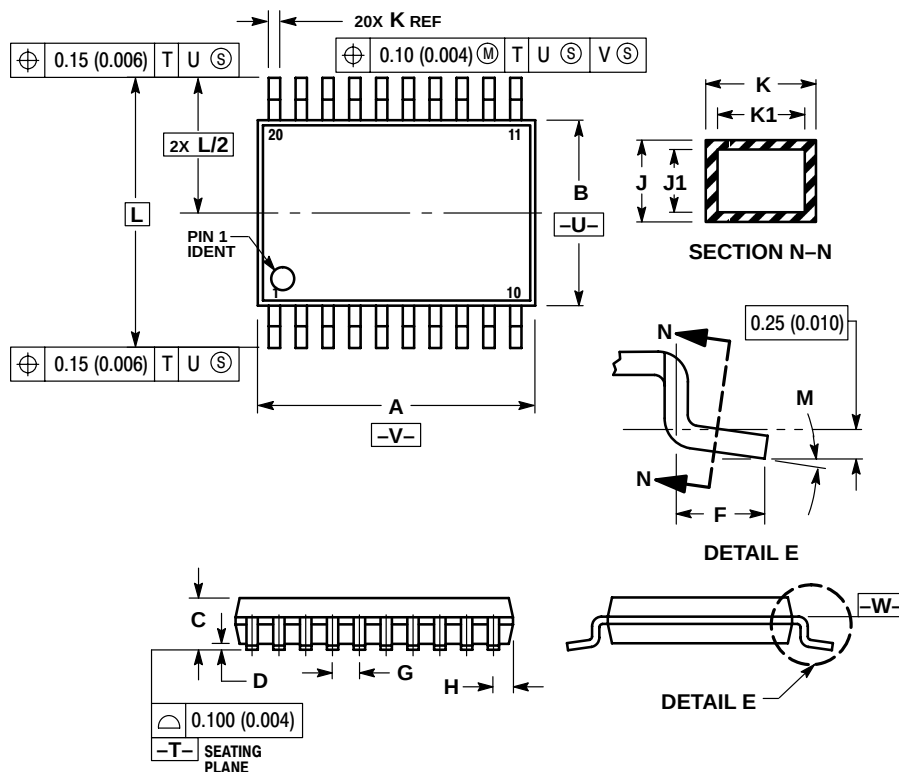
- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
 5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

MC74HC574A

PACKAGE DIMENSIONS

TSSOP-20
DT SUFFIX
 20 PIN PLASTIC TSSOP PACKAGE
 CASE 948E-02
 ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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