P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel vertical D-MOS transistor in SOT89 envelope and intended for use in relay, high-speed and line-transformer drivers, using SMD-technology.

Features

- Very low R_{DSon}
- Direct interface to C-MOS, TTL
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0,25 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	max. typ.	10 Ω 7.5 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	125 mS

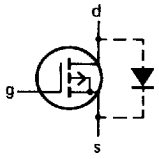
MECHANICAL DATA

Dimensions in mm

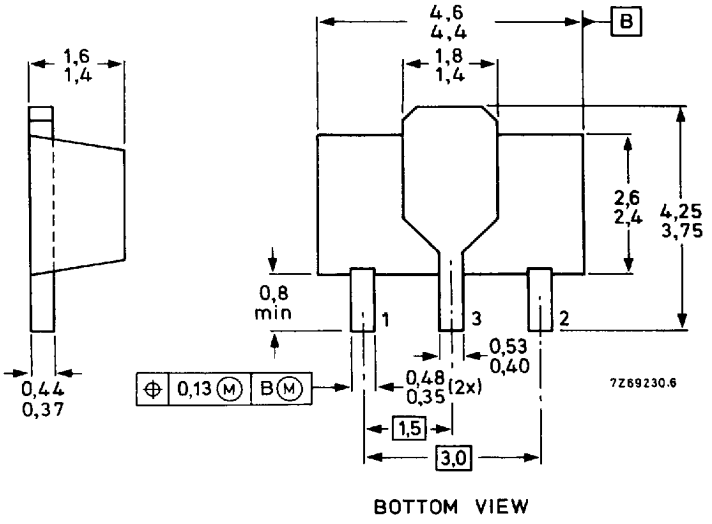
Fig. 1 SOT89.

Pinning:

1 = source
2 = gate
3 = drain



Marking: LN



BOTTOM VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.25 A
Drain current (peak)	$-I_{DM}$	max.	0.5 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Storage temperature range	T_{stg}	−65 to + 150	°C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D$ = 10 μA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	60 V
Drain-source leakage current $-V_{DS}$ = 48 V; V_{GS} = 0	$-I_{DSS}$	max.	1 μA
Gate-source leakage current $-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	max.	100 nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	max. typ..	10 Ω 7.5 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	125 mS
Input capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ. max.	30 pF 45 pF
Output capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ. max.	20 pF 30 pF
Feedback capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ. max.	5 pF 10 pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on} t_{off}	typ. typ.	4 ns 10 ns

Note:

1. Transistor mounted on a ceramic substrate: area = 2,5 cm²; thickness = 0,7 mm.

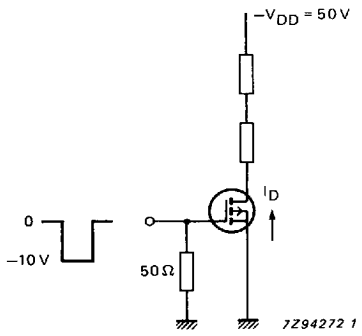


Fig. 2 Switching times test circuit.

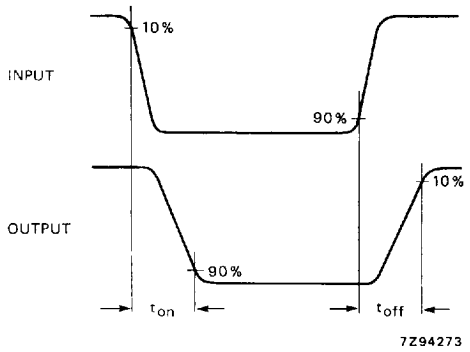


Fig. 3 Input and output waveforms.

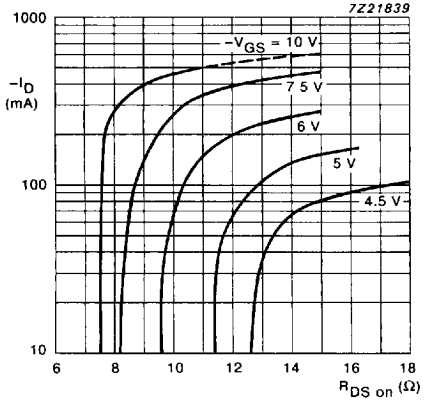


Fig.4 Drain current vs ON-resistance; T_j = 25 °C; typical values.

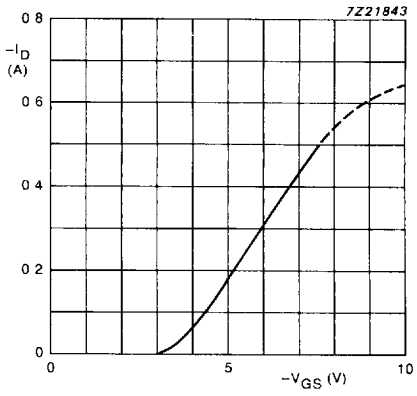


Fig.5 Transfer characteristics; T_j = 25 °C; $-V_{DS}$ = 10 V; typical values.

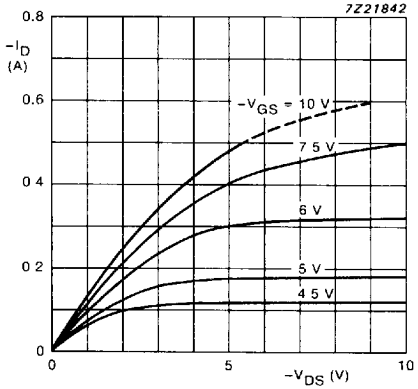


Fig.6 Output characteristics; T_j = 25 °C; typical values.