

IRF540R, IRF541R
IRF542R, IRF543R

File Number 2009

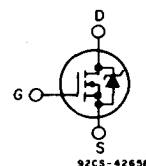
Avalanche Energy Rated N-Channel Power MOSFETs

27A and 24A, 100V-60V
 $r_{DS(on)} = 0.085\Omega$ and 0.11Ω

Features:

- Single pulse avalanche energy rated
- SOA is power-dissipation limited
- Nanosecond switching speeds
- Linear transfer characteristics
- High input impedance

TERMINAL DIAGRAM

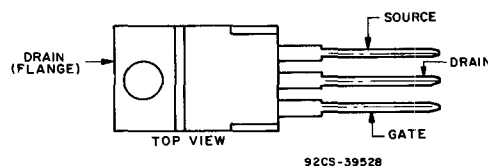


N-CHANNEL ENHANCEMENT MODE

The IRF540R, IRF541R, IRF542R and IRF543R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



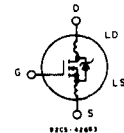
JEDEC TO-220AB

Absolute Maximum Ratings

Parameter	IRF540R	IRF541R	IRF542R	IRF543R	Units
V_{DS} Drain - Source Voltage ①	100	60	100	60	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 20\text{ K}\Omega$) ①	100	60	100	60	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	27	27	24	24	A
$I_D @ T_C = 100^\circ\text{C}$ Continuous Drain Current	17	17	15	15	A
I_{DM} Pulsed Drain Current ③	108	108	96	96	A
V_{GS} Gate - Source Voltage	± 20				V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	125 (See Fig. 14)				W
Linear Derating Factor	1.0 (See Fig. 14)				W/ $^\circ\text{C}$
E_{as} Single Pulse Avalanche Energy Rating ④	230				mJ
T_J Operating Junction and T_{stg} Storage Temperature Range	-55 to 150				$^\circ\text{C}$
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

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Electrical Characteristics @ $T_c = 25^\circ\text{C}$ (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS} Drain - Source Breakdown Voltage	IRF540R	100	—	—	V	V _{GS} = 0V I _D = 250 μ A
	IRF542R	—	—	—	—	
	IRF541R IRF543R	60	—	—	V	
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250 μ A
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	500	nA	V _{GS} = 20V
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V _{GS} = -20V
I _{OSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μ A	V _{DS} = Max. Rating, V _{GS} = 0V
		—	—	1000	μ A	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _c = 125°C
I _{D(on)} On-State Drain Current ②	IRF540R	27	—	—	A	V _{DS} > I _{D(on)} x R _{DS(on) max.} , V _{GS} = 10V
	IRF541R	—	—	—	—	
	IRF542R IRF543R	24	—	—	A	
R _{DS(on)} Static Drain-Source On-State Resistance ②	IRF540R	—	0.07	0.085	Ω	V _{GS} = 10V, I _D = 15A
	IRF541R	—	—	—	—	
	IRF542R IRF543R	—	0.09	0.11	Ω	
g _{fs} Forward Transconductance ②	ALL	6.0	10	—	S(V)	V _{DS} > I _{D(on)} x R _{DS(on) max.} , I _D = 15A
C _{iss} Input Capacitance	ALL	—	1275	—	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz
C _{oss} Output Capacitance	ALL	—	550	—	pF	See Fig. 10
C _{rss} Reverse Transfer Capacitance	ALL	—	180	—	pF	
t _{d(on)} Turn-On Delay Time	ALL	—	16	30	ns	V _{DD} $\approx$ 30V, I _D = 15A, Z ₀ = 4.7 Ω
t _r Rise Time	ALL	—	27	60	ns	See Fig. 17
t _{d(off)} Turn-Off Delay Time	ALL	—	38	80	ns	(MOSFET switching times are essentially independent of operating temperature.)
t _f Fall Time	ALL	—	14	30	ns	
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	38	60	nC	V _{GS} = 10V, I _D = 34A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q _{gs} Gate-Source Charge	ALL	—	17	—	nC	
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	21	—	nC	
L _D Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.
		—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L _S Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.


Thermal Resistance

R _{thJC} Junction-to-Case	ALL	—	—	1.0	°C/W	
R _{thCS} Case-to-Sink	ALL	—	1.0	—	°C/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	—	—	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I _S Continuous Source Current (Body Diode)	IRF540R	—	—	27	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
	IRF541R	—	—	24	A	
	IRF542R IRF543R	—	—	24	A	
I _{SM} Pulse Source Current (Body Diode) ③	IRF540R	—	—	108	A	
	IRF541R	—	—	96	A	
	IRF542R IRF543R	—	—	96	A	
V _{SD} Diode Forward Voltage ②	IRF540R	—	—	2.5	V	T _c = 25°C, I _S = 27A, V _{GS} = 0V
	IRF541R	—	—	2.3	V	T _c = 25°C, I _S = 24A, V _{GS} = 0V
t _{rr} Reverse Recovery Time	ALL	—	500	—	ns	T _J = 150°C, I _F = 27A, di/dt = 100A/ μ s
Q _{RR} Reverse Recovered Charge	ALL	—	2.9	—	μ C	T _J = 150°C, I _F = 27A, di/dt = 100A/ μ s
t _{on} Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

 ① T_J = 25°C to 150°C. ② Pulse Test: Pulse width $\leq$ 300 μ s, Duty Cycle $\leq$ 2%.

③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

 ④ V_{DD} = 25V, starting T_J = 25°C, L = 440 μ H, R_{gs} = 50 Ω , I_{peak} = 28A. See figures 15, 16.

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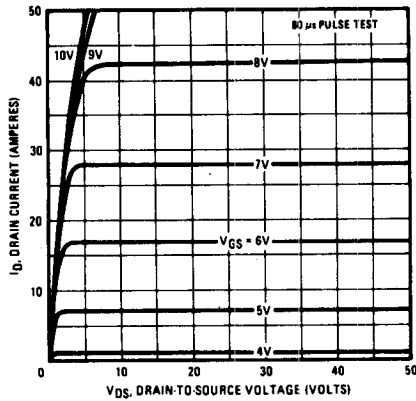


Fig. 1 - Typical Output Characteristics

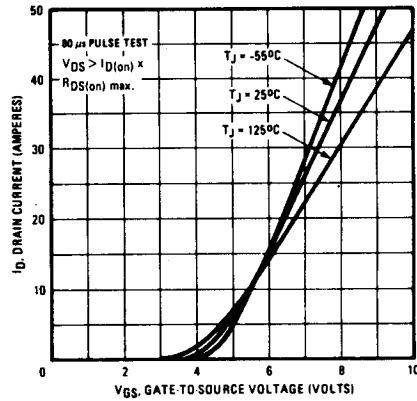


Fig. 2 - Typical Transfer Characteristics

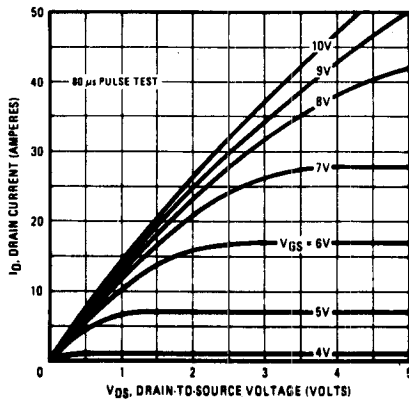


Fig. 3 - Typical Saturation Characteristics

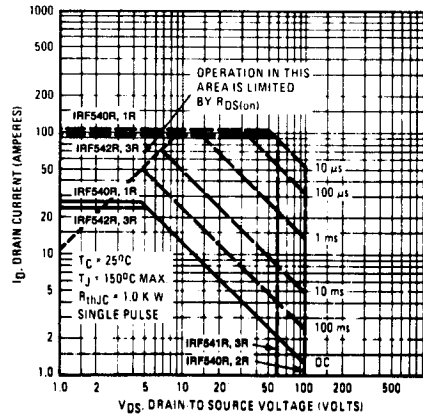


Fig. 4 - Maximum Safe Operating Area

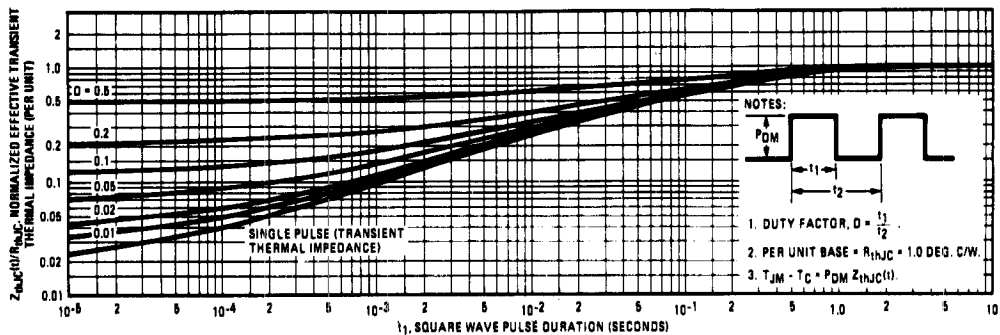


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

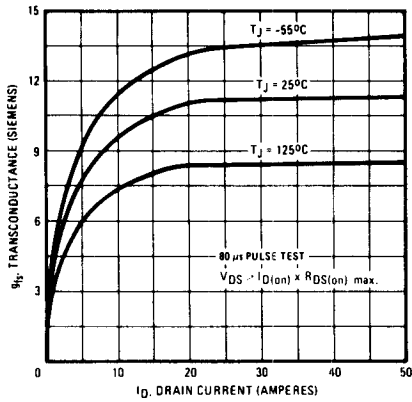


Fig. 6 – Typical Transconductance Vs. Drain Current

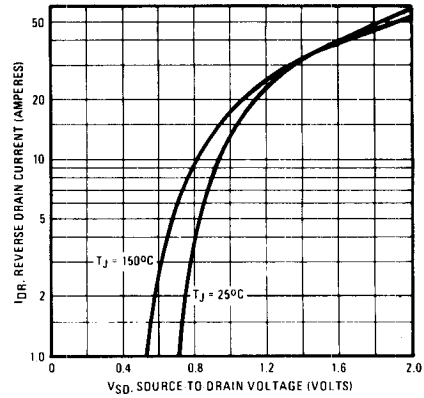


Fig. 7 – Typical Source-Drain Diode Forward Voltage

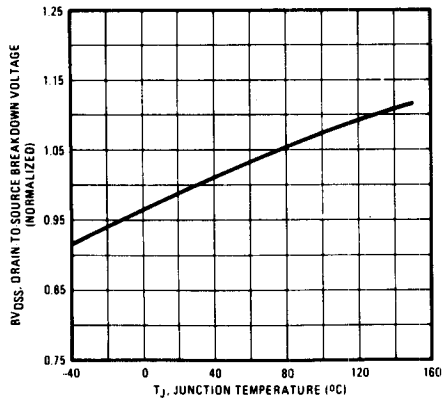


Fig. 8 – Breakdown Voltage Vs. Temperature

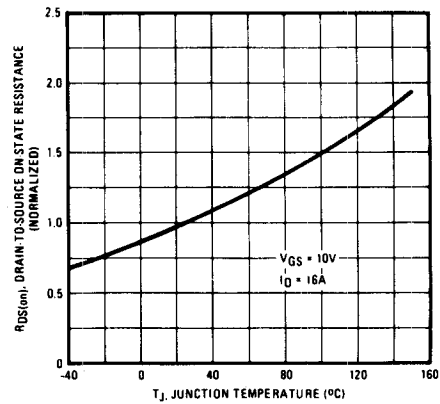


Fig. 9 – Normalized On-Resistance Vs. Temperature

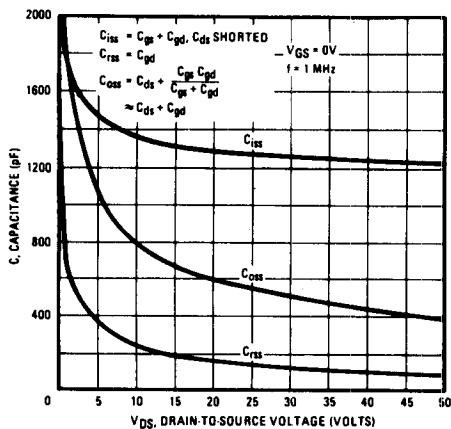


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

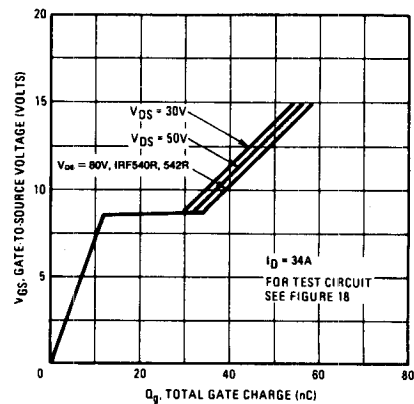


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

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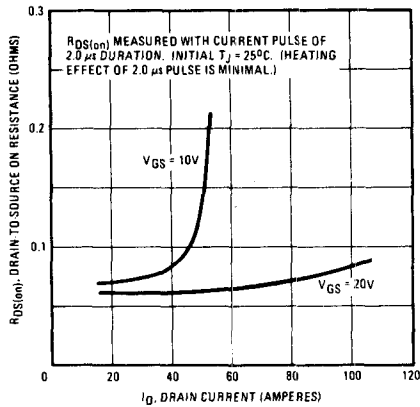


Fig. 12 — Typical On-Resistance Vs. Drain Current

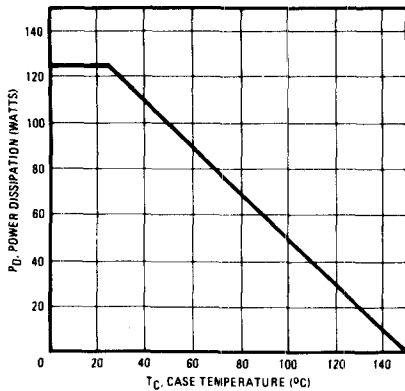


Fig. 14 — Power Vs. Temperature Derating Curve

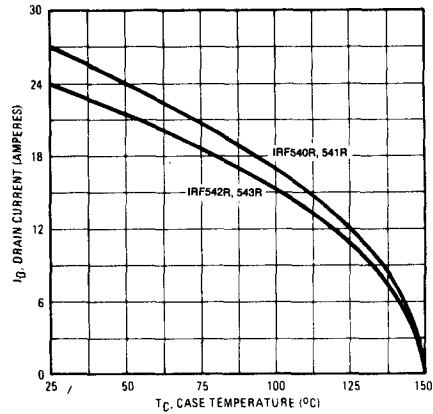


Fig. 13 — Maximum Drain Current Vs. Case Temperature

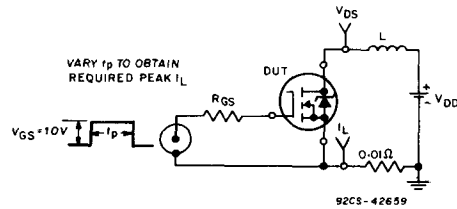


Fig. 15 — Unclamped Energy Test Circuit

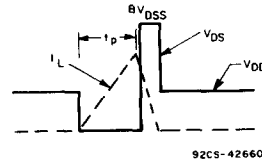


Fig. 16 — Unclamped Energy Waveforms

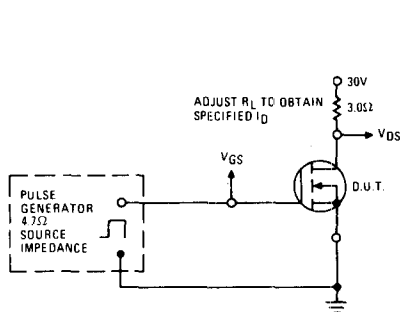


Fig. 17 — Switching Time Test Circuit

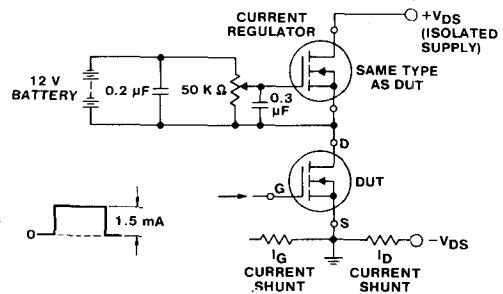


Fig. 18 — Gate Charge Test Circuit