

- Low Supply Voltage Range: 1.8 V to 3.6 V
- Ultralow-Power Consumption:
  - Active Mode: 400  $\mu$ A at 1 MHz, 2.2 V
  - Standby Mode: 1.3  $\mu$ A
  - Off Mode (RAM Retention): 0.22  $\mu$ A
- Five Power-Saving Modes
- Wake-Up From Standby Mode in Less Than 6  $\mu$ s
- 16-Bit RISC Architecture, Extended Memory, 125-ns Instruction Cycle Time
- Three Channel Internal DMA
- 12-Bit A/D Converter With Internal Reference, Sample-and-Hold and Autoscan Feature (MSP430x461x only)
- 16-Bit Timer\_A With Three Capture/Compare Registers
- 16-Bit Timer\_B With Seven Capture/Compare-With-Shadow Registers
- On-Chip Comparator
- Supply Voltage Supervisor/Monitor With Programmable Level Detection
- Basic Timer With Real Time Clock Feature
- Integrated LCD Driver up to 160 Segments With Regulated Charge Pump
- Serial Communication Interface (USART1), Select Asynchronous UART or Synchronous SPI by Software
- Universal Serial Communication Interface
  - Enhanced UART Supporting Auto-Baudrate Detection
  - IrDA Encoder and Decoder
  - Synchronous SPI
  - I2C™
- Serial Onboard Programming, Programmable Code Protection by Security Fuse
- Brownout Detector
- Family Members Include:
  - MSP430x4616, MSP430x46161†: 92KB+256B Flash or ROM Memory, 4KB RAM
  - MSP430x4617, MSP430x46171†: 92KB+256B Flash or ROM Memory, 8KB RAM
  - MSP430x4618, MSP430x46181†: 116KB+256B Flash or ROM Memory, 8KB RAM
  - MSP430x4619, MSP430x46191†: 120KB+256B Flash or ROM Memory, 4KB RAM
- For Complete Module Descriptions, Refer to the *MSP430x4xx Family User's Guide*

† The MSP430F461x1 devices are identical to the MSP430F461x devices, with the exception that the ADC12 module is not implemented.

## description

The Texas Instruments MSP430 family of ultralow-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The devices feature a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6  $\mu$ s.

The MSP430x461x(1) series are microcontroller configurations with two 16-bit timers, a high-performance 12-bit A/D converter (MSP430x461x only), one universal serial communication interface (USCI), one universal synchronous/asynchronous communication interface (USART), DMA, 80 I/O pins, and a liquid crystal display (LCD) driver with regulated charge pump.

Typical applications for this device include portable medical applications and e-meter applications.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. These devices have limited built-in ESD protection.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2009, Texas Instruments Incorporated

# MSP430x461x1, MSP430x461x MIXED SIGNAL MICROCONTROLLER

## AVAILABLE OPTIONS<sup>†</sup>

| T <sub>A</sub> | PACKAGED DEVICES <sup>‡</sup> |                 |
|----------------|-------------------------------|-----------------|
|                | PLASTIC 100-PIN TQFP (PZ)     |                 |
| -40°C to 85°C  | MSP430F4616IPZ                | MSP430F46161IPZ |
|                | MSP430F4617IPZ                | MSP430F46171IPZ |
|                | MSP430F4618IPZ                | MSP430F46181IPZ |
|                | MSP430F4619IPZ                | MSP430F46191IPZ |

<sup>†</sup> For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

<sup>‡</sup> Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

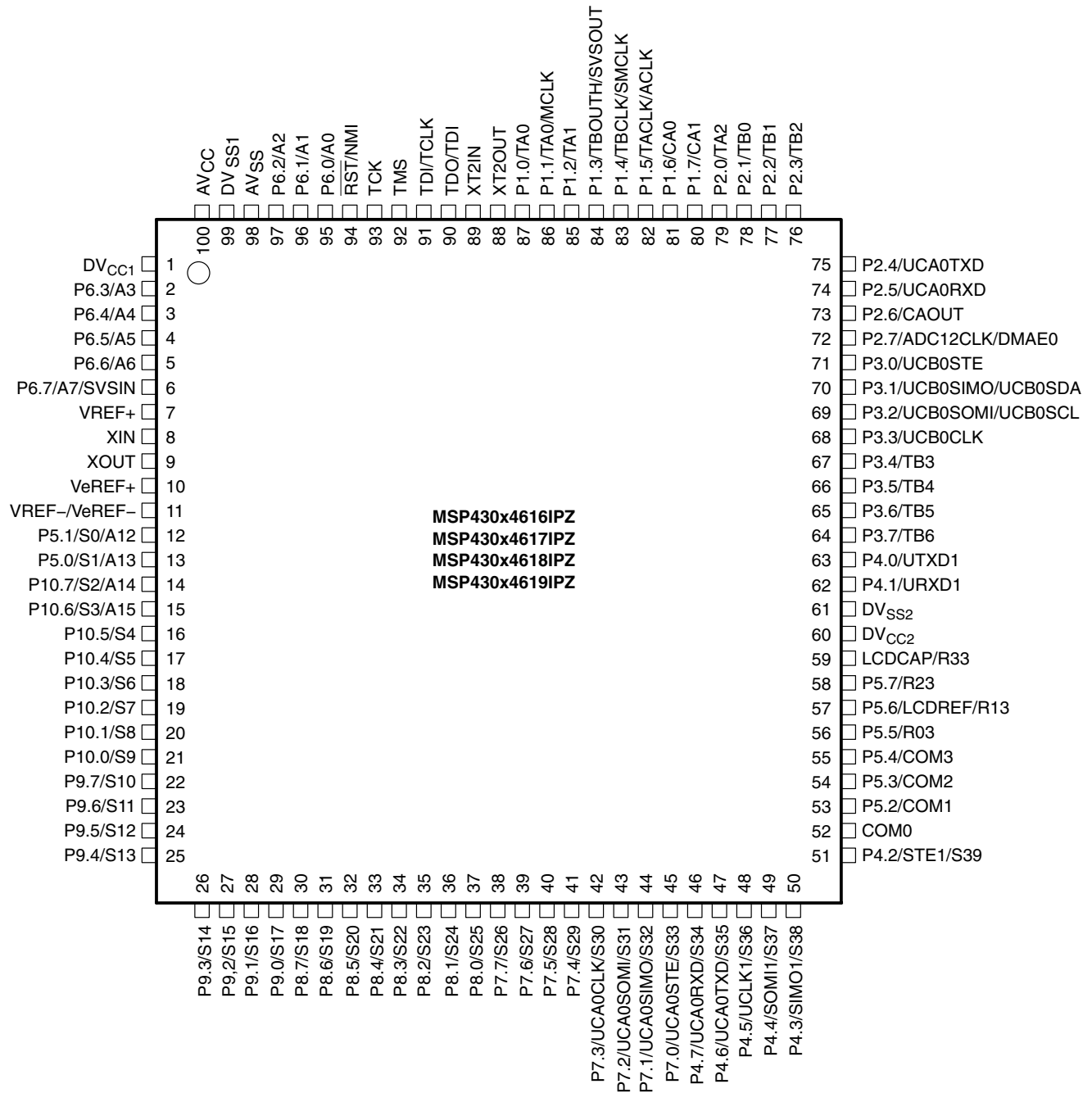
## DEVELOPMENT TOOL SUPPORT

All MSP430 microcontrollers include an Embedded Emulation Module (EEM) allowing advanced debugging and programming through easy to use development tools. Recommended hardware options include the following:

- Debugging and Programming Interface
  - MSP-FET430UIF (USB)
  - MSP-FET430PIF (Parallel Port)
- Debugging and Programming Interface with Target Board
  - MSP-FET430U100
- Stand-Alone Target Board
  - MSP-TS430PZ100
- Production Programmer
  - MSP-GANG430



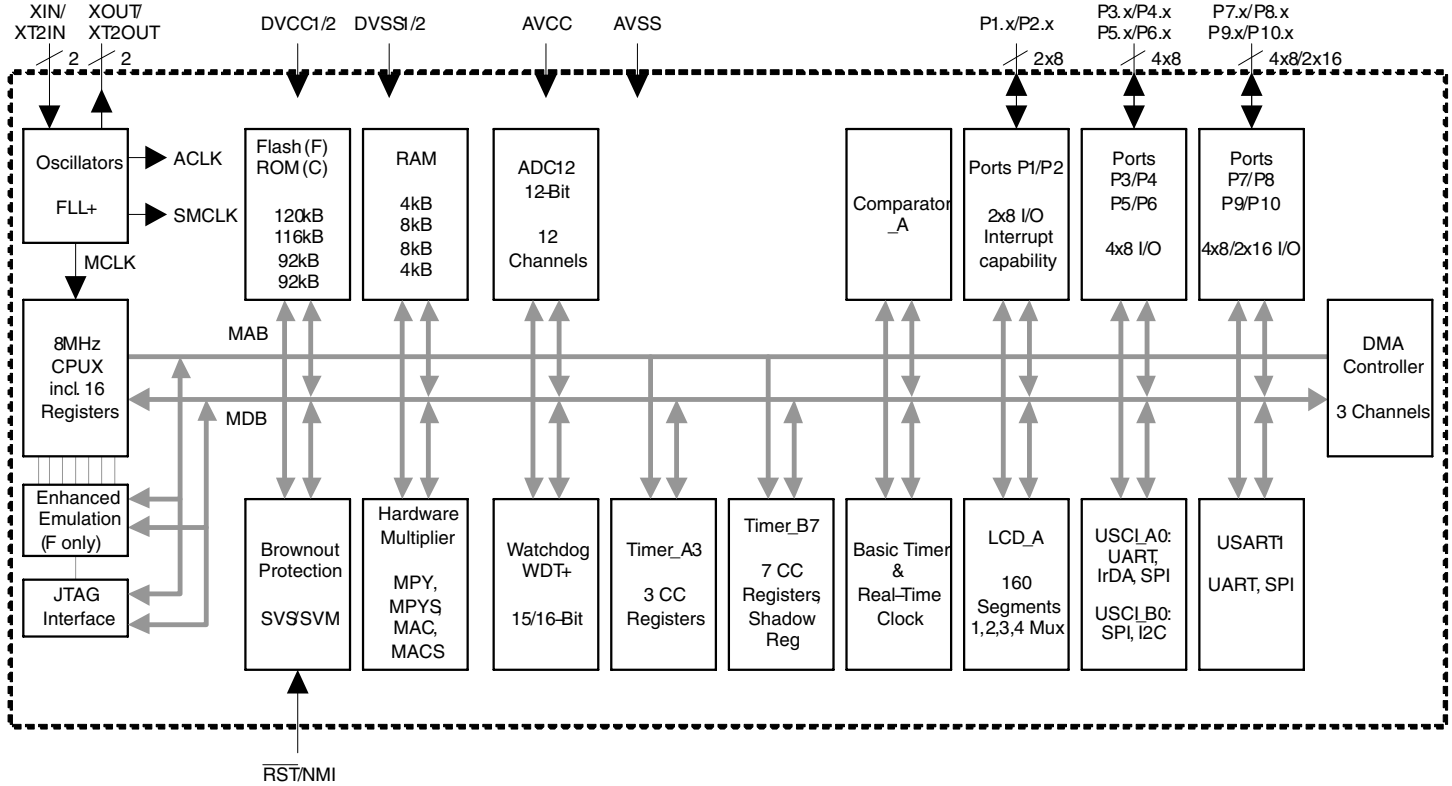
**pin designation, MSP430x461xIPZ**



**pin designation, MSP430x461x1PZ**

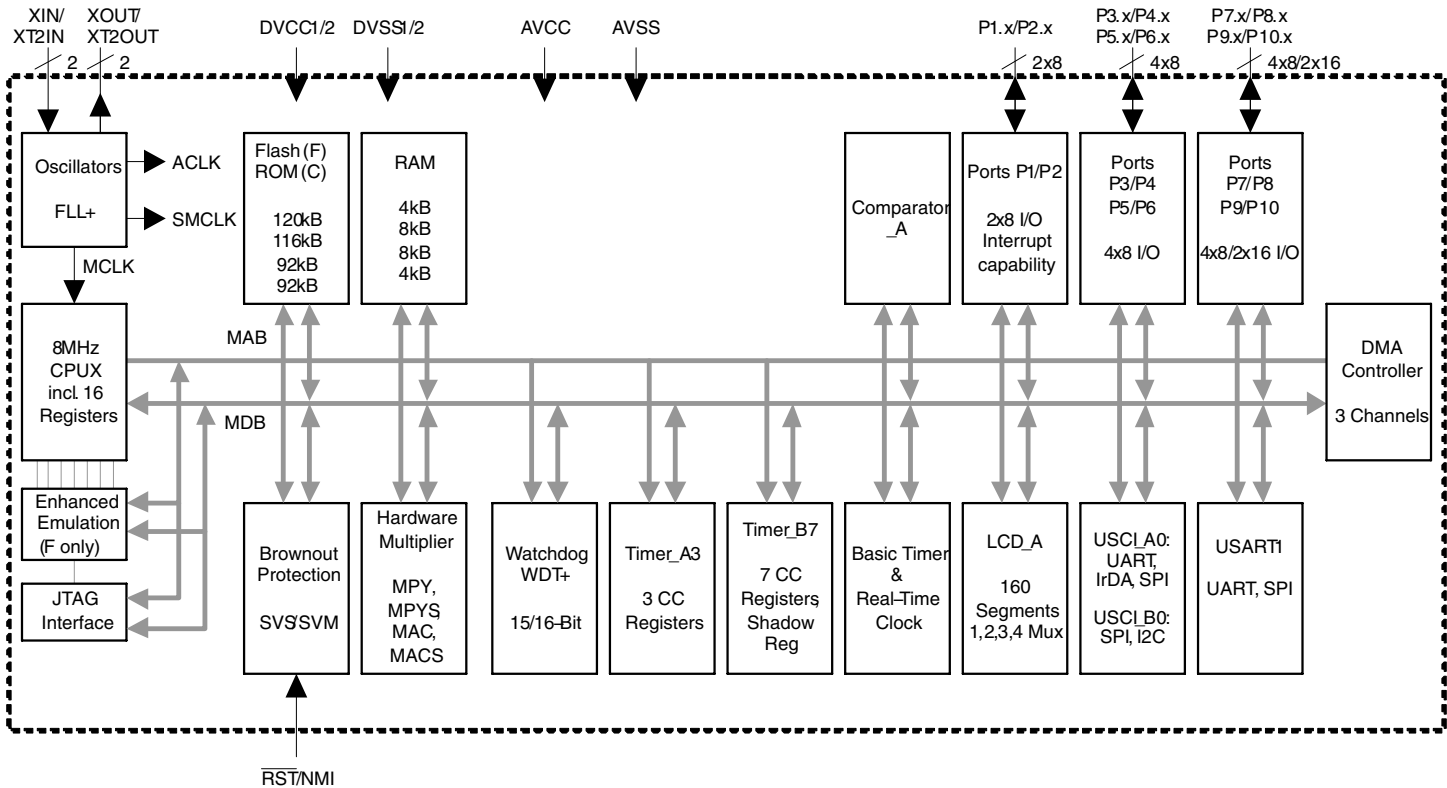


**MSP430x461x functional block diagram**



MSP430x461x1, MSP430x461x  
MIXED SIGNAL MICROCONTROLLER

MSP430x461x1 functional block diagram



**MSP430x461x Terminal Functions**

| TERMINAL                              |     | I/O | DESCRIPTION                                                                                                                                |
|---------------------------------------|-----|-----|--------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                                  | NO. |     |                                                                                                                                            |
| DV <sub>CC1</sub>                     | 1   |     | Digital supply voltage, positive terminal                                                                                                  |
| P6.3/A3                               | 2   | I/O | General-purpose digital I/O / analog input a3—12-bit ADC                                                                                   |
| P6.4/A4                               | 3   | I/O | General-purpose digital I/O / analog input a4—12-bit ADC                                                                                   |
| P6.5/A5                               | 4   | I/O | General-purpose digital I/O / analog input a5—12-bit ADC                                                                                   |
| P6.6/A6                               | 5   | I/O | General-purpose digital I/O / analog input a6—12-bit ADC                                                                                   |
| P6.7/A7/SVSIN                         | 6   | I/O | General-purpose digital I/O / analog input a7—12-bit ADC / analog input to brownout, supply voltage supervisor                             |
| V <sub>REF+</sub>                     | 7   | O   | Output of positive terminal of the reference voltage in the ADC                                                                            |
| XIN                                   | 8   | I   | Input port for crystal oscillator XT1. Standard or watch crystals can be connected.                                                        |
| XOUT                                  | 9   | O   | Output terminal of crystal oscillator XT1                                                                                                  |
| Ve <sub>REF+</sub>                    | 10  | I/O | Input for an external reference voltage to the ADC                                                                                         |
| V <sub>REF-</sub> /Ve <sub>REF-</sub> | 11  | I   | Negative terminal for the ADC reference voltage for both sources, the internal reference voltage, or an external applied reference voltage |
| P5.1/S0/A12 (see Note 1)              | 12  | I/O | General-purpose digital I/O / LCD segment output 0 / analog input a12 – 12-bit ADC                                                         |
| P5.0/S1/A13 (see Note 1)              | 13  | I/O | General-purpose digital I/O / LCD segment output 1 / analog input a13 – 12-bit ADC                                                         |
| P10.7/S2/A14 (see Note 1)             | 14  | I/O | General-purpose digital I/O / LCD segment output 2 / analog input a14 – 12-bit ADC                                                         |
| P10.6/S3/A15 (see Note 1)             | 15  | I/O | General-purpose digital I/O / LCD segment output 3 / analog input a15 – 12-bit ADC                                                         |
| P10.5/S4                              | 16  | I/O | General-purpose digital I/O / LCD segment output 4                                                                                         |
| P10.4/S5                              | 17  | I/O | General-purpose digital I/O / LCD segment output 5                                                                                         |
| P10.3/S6                              | 18  | I/O | General-purpose digital I/O / LCD segment output 6                                                                                         |
| P10.2/S7                              | 19  | I/O | General-purpose digital I/O / LCD segment output 7                                                                                         |
| P10.1/S8                              | 20  | I/O | General-purpose digital I/O / LCD segment output 8                                                                                         |
| P10.0/S9                              | 21  | I/O | General-purpose digital I/O / LCD segment output 9                                                                                         |
| P9.7/S10                              | 22  | I/O | General-purpose digital I/O / LCD segment output 10                                                                                        |
| P9.6/S11                              | 23  | I/O | General-purpose digital I/O / LCD segment output 11                                                                                        |
| P9.5/S12                              | 24  | I/O | General-purpose digital I/O / LCD segment output 12                                                                                        |
| P9.4/S13                              | 25  | I/O | General-purpose digital I/O / LCD segment output 13                                                                                        |
| P9.3/S14                              | 26  | I/O | General-purpose digital I/O / LCD segment output 14                                                                                        |
| P9.2/S15                              | 27  | I/O | General-purpose digital I/O / LCD segment output 15                                                                                        |
| P9.1/S16                              | 28  | I/O | General-purpose digital I/O / LCD segment output 16                                                                                        |
| P9.0/S17                              | 29  | I/O | General-purpose digital I/O / LCD segment output 17                                                                                        |
| P8.7/S18                              | 30  | I/O | General-purpose digital I/O / LCD segment output 18                                                                                        |
| P8.6/S19                              | 31  | I/O | General-purpose digital I/O / LCD segment output 19                                                                                        |
| P8.5/S20                              | 32  | I/O | General-purpose digital I/O / LCD segment output 20                                                                                        |
| P8.4/S21                              | 33  | I/O | General-purpose digital I/O / LCD segment output 21                                                                                        |
| P8.3/S22                              | 34  | I/O | General-purpose digital I/O / LCD segment output 22                                                                                        |

NOTE 1: Segments S0 through S3 are disabled when the LCD charge pump feature is enabled (LCDPEN = 1) and cannot be used together with the LCD charge pump. In addition, when using segments S0 through S3 with an external LCD voltage supply,  $V_{LCD} \leq AV_{CC}$ .

# MSP430x461x1, MSP430x461x MIXED SIGNAL MICROCONTROLLER

## Terminal Functions (Continued)

| TERMINAL          |     | I/O | DESCRIPTION                                                                                                                                              |
|-------------------|-----|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME              | NO. |     |                                                                                                                                                          |
| P8.2/S23          | 35  | I/O | General-purpose digital I/O / LCD segment output 23                                                                                                      |
| P8.1/S24          | 36  | I/O | General-purpose digital I/O / LCD segment output 24                                                                                                      |
| P8.0/S25          | 37  | I/O | General-purpose digital I/O / LCD segment output 25                                                                                                      |
| P7.7/S26          | 38  | I/O | General-purpose digital I/O / LCD segment output 26                                                                                                      |
| P7.6/S27          | 39  | I/O | General-purpose digital I/O / LCD segment output 27                                                                                                      |
| P7.5/S28          | 40  | I/O | General-purpose digital I/O / LCD segment output 28                                                                                                      |
| P7.4/S29          | 41  | I/O | General-purpose digital I/O / LCD segment output 29                                                                                                      |
| P7.3/UCA0CLK/S30  | 42  | I/O | General-purpose digital I/O / external clock input – USCI_A0/UART or SPI mode, clock output – USCI_A0/SPI mode / LCD segment 30                          |
| P7.2/UCA0SOMI/S31 | 43  | I/O | General-purpose digital I/O / slave out/master in of USCI_A0/SPI mode / LCD segment output 31                                                            |
| P7.1/UCA0SIMO/S32 | 44  | I/O | General-purpose digital I/O / slave in/master out of USCI_A0/SPI mode / LCD segment output 32                                                            |
| P7.0/UCA0STE/S33  | 45  | I/O | General-purpose digital I/O / slave transmit enable—USCI_A0/SPI mode / LCD segment output 33                                                             |
| P4.7/UCA0RXD/S34  | 46  | I/O | General-purpose digital I/O / receive data in – USCI_A0/UART or IrDA mode / LCD segment output 34                                                        |
| P4.6/UCA0TXD/S35  | 47  | I/O | General-purpose digital I/O / transmit data out – USCI_A0/UART or IrDA mode / LCD segment output 35                                                      |
| P4.5/UCLK1/S36    | 48  | I/O | General-purpose digital I/O / external clock input – USART1/UART or SPI mode, clock output – USART1/SPI MODE / LCD segment output 36                     |
| P4.4/SOMI1/S37    | 49  | I/O | General-purpose digital I/O / slave out/master in of USART1/SPI mode / LCD segment output 37                                                             |
| P4.3/SIMO1/S38    | 50  | I/O | General-purpose digital I/O / slave in/master out of USART1/SPI mode / LCD segment output 38                                                             |
| P4.2/STE1/S39     | 51  | I/O | General-purpose digital I/O / slave transmit enable—USART1/SPI mode / LCD segment output 39                                                              |
| COM0              | 52  | O   | COM0–3 are used for LCD backplanes.                                                                                                                      |
| P5.2/COM1         | 53  | I/O | General-purpose digital I/O / common output, COM0–3 are used for LCD backplanes.                                                                         |
| P5.3/COM2         | 54  | I/O | General-purpose digital I/O / common output, COM0–3 are used for LCD backplanes.                                                                         |
| P5.4/COM3         | 55  | I/O | General-purpose digital I/O / common output, COM0–3 are used for LCD backplanes.                                                                         |
| P5.5/R03          | 56  | I/O | General-purpose digital I/O / Input port of lowest analog LCD level (V5)                                                                                 |
| P5.6/LCDREF/R13   | 57  | I/O | General-purpose digital I/O / External reference voltage input for regulated LCD voltage / Input port of third most positive analog LCD level (V4 or V3) |
| P5.7/R23          | 58  | I/O | General-purpose digital I/O / Input port of second most positive analog LCD level (V2)                                                                   |
| LDCAP/R33         | 59  | I   | LCD capacitor connection / Input/output port of most positive analog LCD level (V1)                                                                      |
| DV <sub>CC2</sub> | 60  |     | Digital supply voltage, positive terminal                                                                                                                |
| DV <sub>SS2</sub> | 61  |     | Digital supply voltage, negative terminal                                                                                                                |
| P4.1/URXD1        | 62  | I/O | General-purpose digital I/O / receive data in—USART1/UART mode                                                                                           |
| P4.0/UTXD1        | 63  | I/O | General-purpose digital I/O / transmit data out—USART1/UART mode                                                                                         |
| P3.7/TB6          | 64  | I/O | General-purpose digital I/O / Timer_B7 CCR6. Capture: CCI6A/CCI6B input, compare: Out6 output                                                            |
| P3.6/TB5          | 65  | I/O | General-purpose digital I/O / Timer_B7 CCR5. Capture: CCI5A/CCI5B input, compare: Out5 output                                                            |
| P3.5/TB4          | 66  | I/O | General-purpose digital I/O / Timer_B7 CCR4. Capture: CCI4A/CCI4B input, compare: Out4 output                                                            |

**Terminal Functions (Continued)**

| TERMINAL                  |     | I/O | DESCRIPTION                                                                                                                                                           |
|---------------------------|-----|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                      | NO. |     |                                                                                                                                                                       |
| P3.4/TB3                  | 67  | I/O | General-purpose digital I/O / Timer_B7 CCR3. Capture: CCI3A/CCI3B input, compare: Out3 output                                                                         |
| P3.3/UCB0CLK              | 68  | I/O | General-purpose digital I/O / external clock input—USCI_B0/UART or SPI mode, clock output—USCI_B0/SPI mode                                                            |
| P3.2/UCB0SOMI/<br>UCB0SCL | 69  | I/O | General-purpose digital I/O / slave out/master in of USCI_B0/SPI mode /I2C clock—USCI_B0/I2C mode                                                                     |
| P3.1/UCB0SIMO/<br>UCB0SDA | 70  | I/O | General-purpose digital I/O / slave in/master out of USCI_B0/SPI mode, I2C data—USCI_B0/I2C mode                                                                      |
| P3.0/UCB0STE              | 71  | I/O | General-purpose digital I/O / slave transmit enable—USCI_B0/SPI mode                                                                                                  |
| P2.7/ADC12CLK/<br>DMAE0   | 72  | I/O | General-purpose digital I/O / conversion clock—12-bit ADC / DMA Channel 0 external trigger                                                                            |
| P2.6/CAOUT                | 73  | I/O | General-purpose digital I/O / Comparator_A output                                                                                                                     |
| P2.5/UCA0RXD              | 74  | I/O | General-purpose digital I/O / receive data in—USCI_A0/UART or IrDA mode                                                                                               |
| P2.4/UCA0TXD              | 75  | I/O | General-purpose digital I/O / transmit data out—USCI_A0/UART or IrDA mode                                                                                             |
| P2.3/TB2                  | 76  | I/O | General-purpose digital I/O / Timer_B7 CCR2. Capture: CCI2A/CCI2B input, compare: Out2 output                                                                         |
| P2.2/TB1                  | 77  | I/O | General-purpose digital I/O / Timer_B7 CCR1. Capture: CCI1A/CCI1B input, compare: Out1 output                                                                         |
| P2.1/TB0                  | 78  | I/O | General-purpose digital I/O / Timer_B7 CCR0. Capture: CCI0A/CCI0B input, compare: Out0 output                                                                         |
| P2.0/TA2                  | 79  | I/O | General-purpose digital I/O / Timer_A Capture: CCI2A input, compare: Out2 output                                                                                      |
| P1.7/CA1                  | 80  | I/O | General-purpose digital I/O / Comparator_A input                                                                                                                      |
| P1.6/CA0                  | 81  | I/O | General-purpose digital I/O / Comparator_A input                                                                                                                      |
| P1.5/TACLK/ACLK           | 82  | I/O | General-purpose digital I/O / Timer_A, clock signal TACLK input / ACLK output (divided by 1, 2, 4, or 8)                                                              |
| P1.4/TBCLK/SMCLK          | 83  | I/O | General-purpose digital I/O / input clock TBCLK—Timer_B7 / submain system clock SMCLK output                                                                          |
| P1.3/TBOUTH/SVSOUT        | 84  | I/O | General-purpose digital I/O / switch all PWM digital output ports to high impedance—Timer_B7 TB0 to TB6 / SVS: output of SVS comparator                               |
| P1.2/TA1                  | 85  | I/O | General-purpose digital I/O / Timer_A, Capture: CCI1A input, compare: Out1 output                                                                                     |
| P1.1/TA0/MCLK             | 86  | I/O | General-purpose digital I/O / Timer_A. Capture: CCI0B input / MCLK output.<br>Note: TA0 is only an input on this pin / BSL receive                                    |
| P1.0/TA0                  | 87  | I/O | General-purpose digital I/O / Timer_A. Capture: CCI0A input, compare: Out0 output / BSL transmit                                                                      |
| XT2OUT                    | 88  | O   | Output terminal of crystal oscillator XT2                                                                                                                             |
| XT2IN                     | 89  | I   | Input port for crystal oscillator XT2. Only standard crystals can be connected.                                                                                       |
| TDO/TDI                   | 90  | I/O | Test data output port. TDO/TDI data output or programming data input terminal                                                                                         |
| TDI/TCLK                  | 91  | I   | Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.                                                                             |
| TMS                       | 92  | I   | Test mode select. TMS is used as an input port for device programming and test.                                                                                       |
| TCK                       | 93  | I   | Test clock. TCK is the clock input port for device programming and test.                                                                                              |
| RST/NMI                   | 94  | I   | Reset input or nonmaskable interrupt input port                                                                                                                       |
| P6.0/A0                   | 95  | I/O | General-purpose digital I/O / analog input a0—12-bit ADC                                                                                                              |
| P6.1/A1                   | 96  | I/O | General-purpose digital I/O / analog input a1—12-bit ADC                                                                                                              |
| P6.2/A2                   | 97  | I/O | General-purpose digital I/O / analog input a2—12-bit ADC                                                                                                              |
| AV <sub>SS</sub>          | 98  |     | Analog supply voltage, negative terminal. Supplies SVS, brownout, oscillator, comparator_A, port 1                                                                    |
| DV <sub>SS1</sub>         | 99  |     | Digital supply voltage, negative terminal                                                                                                                             |
| AV <sub>CC</sub>          | 100 |     | Analog supply voltage, positive terminal. Supplies SVS, brownout, oscillator, comparator_A, port 1; must not power up prior to DV <sub>CC1</sub> /DV <sub>CC2</sub> . |

# MSP430x461x1, MSP430x461x MIXED SIGNAL MICROCONTROLLER

## MSP430x461x1 Terminal Functions

| TERMINAL              |     | I/O | DESCRIPTION                                                                         |
|-----------------------|-----|-----|-------------------------------------------------------------------------------------|
| NAME                  | NO. |     |                                                                                     |
| DV <sub>CC1</sub>     | 1   |     | Digital supply voltage, positive terminal                                           |
| P6.3                  | 2   | I/O | General-purpose digital I/O                                                         |
| P6.4                  | 3   | I/O | General-purpose digital I/O                                                         |
| P6.5                  | 4   | I/O | General-purpose digital I/O                                                         |
| P6.6                  | 5   | I/O | General-purpose digital I/O                                                         |
| P6.7/SVSIN            | 6   | I/O | General-purpose digital I/O / analog input to brownout, supply voltage supervisor   |
| Reserved              | 7   | O   | Reserved, do not connect externally                                                 |
| XIN                   | 8   | I   | Input port for crystal oscillator XT1. Standard or watch crystals can be connected. |
| XOUT                  | 9   | O   | Output terminal of crystal oscillator XT1                                           |
| DV <sub>SS</sub>      | 10  | I/O | Connect to DV <sub>SS</sub>                                                         |
| DV <sub>SS</sub>      | 11  | I   | Connect to DV <sub>SS</sub>                                                         |
| P5.1/S0 (see Note 2)  | 12  | I/O | General-purpose digital I/O / LCD segment output 0                                  |
| P5.0/S1 (see Note 2)  | 13  | I/O | General-purpose digital I/O / LCD segment output 1                                  |
| P10.7/S2 (see Note 2) | 14  | I/O | General-purpose digital I/O / LCD segment output 2                                  |
| P10.6/S3 (see Note 2) | 15  | I/O | General-purpose digital I/O / LCD segment output 3                                  |
| P10.5/S4              | 16  | I/O | General-purpose digital I/O / LCD segment output 4                                  |
| P10.4/S5              | 17  | I/O | General-purpose digital I/O / LCD segment output 5                                  |
| P10.3/S6              | 18  | I/O | General-purpose digital I/O / LCD segment output 6                                  |
| P10.2/S7              | 19  | I/O | General-purpose digital I/O / LCD segment output 7                                  |
| P10.1/S8              | 20  | I/O | General-purpose digital I/O / LCD segment output 8                                  |
| P10.0/S9              | 21  | I/O | General-purpose digital I/O / LCD segment output 9                                  |
| P9.7/S10              | 22  | I/O | General-purpose digital I/O / LCD segment output 10                                 |
| P9.6/S11              | 23  | I/O | General-purpose digital I/O / LCD segment output 11                                 |
| P9.5/S12              | 24  | I/O | General-purpose digital I/O / LCD segment output 12                                 |
| P9.4/S13              | 25  | I/O | General-purpose digital I/O / LCD segment output 13                                 |
| P9.3/S14              | 26  | I/O | General-purpose digital I/O / LCD segment output 14                                 |
| P9.2/S15              | 27  | I/O | General-purpose digital I/O / LCD segment output 15                                 |
| P9.1/S16              | 28  | I/O | General-purpose digital I/O / LCD segment output 16                                 |
| P9.0/S17              | 29  | I/O | General-purpose digital I/O / LCD segment output 17                                 |
| P8.7/S18              | 30  | I/O | General-purpose digital I/O / LCD segment output 18                                 |
| P8.6/S19              | 31  | I/O | General-purpose digital I/O / LCD segment output 19                                 |
| P8.5/S20              | 32  | I/O | General-purpose digital I/O / LCD segment output 20                                 |
| P8.4/S21              | 33  | I/O | General-purpose digital I/O / LCD segment output 21                                 |
| P8.3/S22              | 34  | I/O | General-purpose digital I/O / LCD segment output 22                                 |

NOTE 2: Segments S0 through S3 are disabled when the LCD charge pump feature is enabled (LCDPEN = 1) and cannot be used together with the LCD charge pump. In addition, when using segments S0 through S3 with an external LCD voltage supply,  $V_{LCD} \leq AV_{CC}$ .

**Terminal Functions (Continued)**

| TERMINAL          |     | I/O | DESCRIPTION                                                                                                                                              |
|-------------------|-----|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME              | NO. |     |                                                                                                                                                          |
| P8.2/S23          | 35  | I/O | General-purpose digital I/O / LCD segment output 23                                                                                                      |
| P8.1/S24          | 36  | I/O | General-purpose digital I/O / LCD segment output 24                                                                                                      |
| P8.0/S25          | 37  | I/O | General-purpose digital I/O / LCD segment output 25                                                                                                      |
| P7.7/S26          | 38  | I/O | General-purpose digital I/O / LCD segment output 26                                                                                                      |
| P7.6/S27          | 39  | I/O | General-purpose digital I/O / LCD segment output 27                                                                                                      |
| P7.5/S28          | 40  | I/O | General-purpose digital I/O / LCD segment output 28                                                                                                      |
| P7.4/S29          | 41  | I/O | General-purpose digital I/O / LCD segment output 29                                                                                                      |
| P7.3/UCA0CLK/S30  | 42  | I/O | General-purpose digital I/O / external clock input – USCI_A0/UART or SPI mode, clock output – USCI_A0/SPI mode / LCD segment 30                          |
| P7.2/UCA0SOMI/S31 | 43  | I/O | General-purpose digital I/O / slave out/master in of USCI_A0/SPI mode / LCD segment output 31                                                            |
| P7.1/UCA0SIMO/S32 | 44  | I/O | General-purpose digital I/O / slave in/master out of USCI_A0/SPI mode / LCD segment output 32                                                            |
| P7.0/UCA0STE/S33  | 45  | I/O | General-purpose digital I/O / slave transmit enable—USCI_A0/SPI mode / LCD segment output 33                                                             |
| P4.7/UCA0RXD/S34  | 46  | I/O | General-purpose digital I/O / receive data in – USCI_A0/UART or IrDA mode / LCD segment output 34                                                        |
| P4.6/UCA0TXD/S35  | 47  | I/O | General-purpose digital I/O / transmit data out – USCI_A0/UART or IrDA mode / LCD segment output 35                                                      |
| P4.5/UCLK1/S36    | 48  | I/O | General-purpose digital I/O / external clock input – USART1/UART or SPI mode, clock output – USART1/SPI MODE / LCD segment output 36                     |
| P4.4/SOMI1/S37    | 49  | I/O | General-purpose digital I/O / slave out/master in of USART1/SPI mode / LCD segment output 37                                                             |
| P4.3/SIMO1/S38    | 50  | I/O | General-purpose digital I/O / slave in/master out of USART1/SPI mode / LCD segment output 38                                                             |
| P4.2/STE1/S39     | 51  | I/O | General-purpose digital I/O / slave transmit enable—USART1/SPI mode / LCD segment output 39                                                              |
| COM0              | 52  | O   | COM0–3 are used for LCD backplanes.                                                                                                                      |
| P5.2/COM1         | 53  | I/O | General-purpose digital I/O / common output, COM0–3 are used for LCD backplanes.                                                                         |
| P5.3/COM2         | 54  | I/O | General-purpose digital I/O / common output, COM0–3 are used for LCD backplanes.                                                                         |
| P5.4/COM3         | 55  | I/O | General-purpose digital I/O / common output, COM0–3 are used for LCD backplanes.                                                                         |
| P5.5/R03          | 56  | I/O | General-purpose digital I/O / Input port of lowest analog LCD level (V5)                                                                                 |
| P5.6/LCDREF/R13   | 57  | I/O | General-purpose digital I/O / External reference voltage input for regulated LCD voltage / Input port of third most positive analog LCD level (V4 or V3) |
| P5.7/R23          | 58  | I/O | General-purpose digital I/O / Input port of second most positive analog LCD level (V2)                                                                   |
| LCDCAP/R33        | 59  | I   | LCD capacitor connection / Input/output port of most positive analog LCD level (V1)                                                                      |
| DV <sub>CC2</sub> | 60  |     | Digital supply voltage, positive terminal                                                                                                                |
| DV <sub>SS2</sub> | 61  |     | Digital supply voltage, negative terminal                                                                                                                |
| P4.1/URXD1        | 62  | I/O | General-purpose digital I/O / receive data in—USART1/UART mode                                                                                           |
| P4.0/UTXD1        | 63  | I/O | General-purpose digital I/O / transmit data out—USART1/UART mode                                                                                         |
| P3.7/TB6          | 64  | I/O | General-purpose digital I/O / Timer_B7 CCR6. Capture: CCI6A/CCI6B input, compare: Out6 output                                                            |
| P3.6/TB5          | 65  | I/O | General-purpose digital I/O / Timer_B7 CCR5. Capture: CCI5A/CCI5B input, compare: Out5 output                                                            |
| P3.5/TB4          | 66  | I/O | General-purpose digital I/O / Timer_B7 CCR4. Capture: CCI4A/CCI4B input, compare: Out4 output                                                            |

# MSP430x461x1, MSP430x461x

## MIXED SIGNAL MICROCONTROLLER

### Terminal Functions (Continued)

| TERMINAL                  |     | I/O | DESCRIPTION                                                                                                                                                           |
|---------------------------|-----|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                      | NO. |     |                                                                                                                                                                       |
| P3.4/TB3                  | 67  | I/O | General-purpose digital I/O / Timer_B7 CCR3. Capture: CCI3A/CCI3B input, compare: Out3 output                                                                         |
| P3.3/UCB0CLK              | 68  | I/O | General-purpose digital I/O / external clock input—USCI_B0/UART or SPI mode, clock output—USCI_B0/SPI mode                                                            |
| P3.2/UCB0SOMI/<br>UCB0SCL | 69  | I/O | General-purpose digital I/O / slave out/master in of USCI_B0/SPI mode /I2C clock—USCI_B0/I2C mode                                                                     |
| P3.1/UCB0SIMO/<br>UCB0SDA | 70  | I/O | General-purpose digital I/O / slave in/master out of USCI_B0/SPI mode, I2C data—USCI_B0/I2C mode                                                                      |
| P3.0/UCB0STE              | 71  | I/O | General-purpose digital I/O / slave transmit enable—USCI_B0/SPI mode                                                                                                  |
| P2.7/ADC12CLK/<br>DMAE0   | 72  | I/O | General-purpose digital I/O / conversion clock—12-bit ADC / DMA Channel 0 external trigger                                                                            |
| P2.6/CAOUT                | 73  | I/O | General-purpose digital I/O / Comparator_A output                                                                                                                     |
| P2.5/UCA0RXD              | 74  | I/O | General-purpose digital I/O / receive data in—USCI_A0/UART or IrDA mode                                                                                               |
| P2.4/UCA0TXD              | 75  | I/O | General-purpose digital I/O / transmit data out—USCI_A0/UART or IrDA mode                                                                                             |
| P2.3/TB2                  | 76  | I/O | General-purpose digital I/O / Timer_B7 CCR2. Capture: CCI2A/CCI2B input, compare: Out2 output                                                                         |
| P2.2/TB1                  | 77  | I/O | General-purpose digital I/O / Timer_B7 CCR1. Capture: CCI1A/CCI1B input, compare: Out1 output                                                                         |
| P2.1/TB0                  | 78  | I/O | General-purpose digital I/O / Timer_B7 CCR0. Capture: CCI0A/CCI0B input, compare: Out0 output                                                                         |
| P2.0/TA2                  | 79  | I/O | General-purpose digital I/O / Timer_A Capture: CCI2A input, compare: Out2 output                                                                                      |
| P1.7/CA1                  | 80  | I/O | General-purpose digital I/O / Comparator_A input                                                                                                                      |
| P1.6/CA0                  | 81  | I/O | General-purpose digital I/O / Comparator_A input                                                                                                                      |
| P1.5/TACLK/ACLK           | 82  | I/O | General-purpose digital I/O / Timer_A, clock signal TACLK input / ACLK output (divided by 1, 2, 4, or 8)                                                              |
| P1.4/TBCLK/SMCLK          | 83  | I/O | General-purpose digital I/O / input clock TBCLK—Timer_B7 / submain system clock SMCLK output                                                                          |
| P1.3/TBOUTH/SVSOUT        | 84  | I/O | General-purpose digital I/O / switch all PWM digital output ports to high impedance—Timer_B7 TB0 to TB6 / SVS: output of SVS comparator                               |
| P1.2/TA1                  | 85  | I/O | General-purpose digital I/O / Timer_A, Capture: CCI1A input, compare: Out1 output                                                                                     |
| P1.1/TA0/MCLK             | 86  | I/O | General-purpose digital I/O / Timer_A. Capture: CCI0B input / MCLK output.<br>Note: TA0 is only an input on this pin / BSL receive                                    |
| P1.0/TA0                  | 87  | I/O | General-purpose digital I/O / Timer_A. Capture: CCI0A input, compare: Out0 output / BSL transmit                                                                      |
| XT2OUT                    | 88  | O   | Output terminal of crystal oscillator XT2                                                                                                                             |
| XT2IN                     | 89  | I   | Input port for crystal oscillator XT2. Only standard crystals can be connected.                                                                                       |
| TDO/TDI                   | 90  | I/O | Test data output port. TDO/TDI data output or programming data input terminal                                                                                         |
| TDI/TCLK                  | 91  | I   | Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.                                                                             |
| TMS                       | 92  | I   | Test mode select. TMS is used as an input port for device programming and test.                                                                                       |
| TCK                       | 93  | I   | Test clock. TCK is the clock input port for device programming and test.                                                                                              |
| RST/NMI                   | 94  | I   | Reset input or nonmaskable interrupt input port                                                                                                                       |
| P6.0                      | 95  | I/O | General-purpose digital I/O                                                                                                                                           |
| P6.1                      | 96  | I/O | General-purpose digital I/O                                                                                                                                           |
| P6.2                      | 97  | I/O | General-purpose digital I/O                                                                                                                                           |
| AV <sub>SS</sub>          | 98  |     | Analog supply voltage, negative terminal. Supplies SVS, brownout, oscillator, comparator_A, port 1                                                                    |
| DV <sub>SS1</sub>         | 99  |     | Digital supply voltage, negative terminal                                                                                                                             |
| AV <sub>CC</sub>          | 100 |     | Analog supply voltage, positive terminal. Supplies SVS, brownout, oscillator, comparator_A, port 1; must not power up prior to DV <sub>CC1</sub> /DV <sub>CC2</sub> . |

## short-form description

### CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The MSP430x461x(1) device family uses the MSP430X CPU and is completely backward compatible with the MSP430 CPU. For a complete description of the MSP430X CPU, see the *MSP430x4xx Family User's Guide*.

### instruction set

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; Table 2 shows the address modes.

|                          |           |
|--------------------------|-----------|
| Program Counter          | PC/R0     |
| Stack Pointer            | SP/R1     |
| Status Register          | SR/CG1/R2 |
| Constant Generator       | CG2/R3    |
| General-Purpose Register | R4        |
| General-Purpose Register | R5        |
| General-Purpose Register | R6        |
| General-Purpose Register | R7        |
| General-Purpose Register | R8        |
| General-Purpose Register | R9        |
| General-Purpose Register | R10       |
| General-Purpose Register | R11       |
| General-Purpose Register | R12       |
| General-Purpose Register | R13       |
| General-Purpose Register | R14       |
| General-Purpose Register | R15       |

**Table 1. Instruction Word Formats**

|                                   |                 |                       |
|-----------------------------------|-----------------|-----------------------|
| Dual operands, source-destination | e.g., ADD R4,R5 | R4 + R5 ----> R5      |
| Single operands, destination only | e.g., CALL R8   | PC -->(TOS), R8--> PC |
| Relative jump, un/conditional     | e.g., JNE       | Jump-on-equal bit = 0 |

**Table 2. Address Mode Descriptions**

| ADDRESS MODE           | S | D | SYNTAX             | EXAMPLE          | OPERATION                     |
|------------------------|---|---|--------------------|------------------|-------------------------------|
| Register               | ● | ● | MOV Rs,Rd          | MOV R10,R11      | R10 → R11                     |
| Indexed                | ● | ● | MOV X(Rn),Y(Rm)    | MOV 2(R5),6(R6)  | M(2+R5)→ M(6+R6)              |
| Symbolic (PC relative) | ● | ● | MOV EDE,TONI       |                  | M(EDE) → M(TONI)              |
| Absolute               | ● | ● | MOV & MEM, & TCDAT |                  | M(MEM) → M(TCDAT)             |
| Indirect               | ● |   | MOV @Rn,Y(Rm)      | MOV @R10,Tab(R6) | M(R10) → M(Tab+R6)            |
| Indirect autoincrement | ● |   | MOV @Rn+,Rm        | MOV @R10+,R11    | M(R10) → R11<br>R10 + 2 → R10 |
| Immediate              | ● |   | MOV #X,TONI        | MOV #45,TONI     | #45 → M(TONI)                 |

NOTE: S = source D = destination

## operating modes

The MSP430 has one active mode and five software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
  - FLL+ loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - FLL+ loop control is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK, FLL+ loop control and DCOCLK are disabled
  - DCO's dc generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK, FLL+ loop control, and DCOCLK are disabled
  - DCO's dc generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK, FLL+ loop control, and DCOCLK are disabled
  - DCO's dc generator is disabled
  - Crystal oscillator is stopped

## interrupt vector addresses

The interrupt vectors and the power-up start address are located in the address range 0FFFFh to 0FFC0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

**Table 3. Interrupt Sources, Flags, and Vectors**

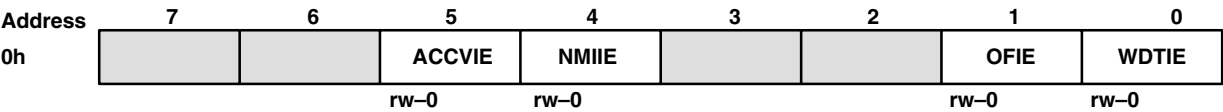
| INTERRUPT SOURCE                                         | INTERRUPT FLAG                                                                             | SYSTEM INTERRUPT                                | WORD ADDRESS | PRIORITY    |
|----------------------------------------------------------|--------------------------------------------------------------------------------------------|-------------------------------------------------|--------------|-------------|
| Power-Up<br>External Reset<br>Watchdog<br>Flash Memory   | WDTIFG<br>KEYV<br>(see Note 1 and 5)                                                       | Reset                                           | 0FFFEh       | 31, highest |
| NMI<br>Oscillator Fault<br>Flash Memory Access Violation | NMIIFG (see Notes 1 and 3)<br>OFIFG (see Notes 1 and 3)<br>ACCVIFG (see Notes 1, 2, and 5) | (Non)maskable<br>(Non)maskable<br>(Non)maskable | 0FFFCh       | 30          |
| Timer_B7                                                 | TBCCR0 CCIFG0 (see Note 2)                                                                 | Maskable                                        | 0FFFAh       | 29          |
| Timer_B7                                                 | TBCCR1 CCIFG1 ... TBCCR6 CCIFG6,<br>TBIFG (see Notes 1 and 2)                              | Maskable                                        | 0FFF8h       | 28          |
| Comparator_A                                             | CAIFG                                                                                      | Maskable                                        | 0FFF6h       | 27          |
| Watchdog Timer+                                          | WDTIFG                                                                                     | Maskable                                        | 0FFF4h       | 26          |
| USCI_A0/USCI_B0 Receive                                  | UCA0RXIFG, UCB0RXIFG (see Note 1)                                                          | Maskable                                        | 0FFF2h       | 25          |
| USCI_A0/USCI_B0 Transmit                                 | UCA0TXIFG, UCB0TXIFG (see Note 1)                                                          | Maskable                                        | 0FFF0h       | 24          |
| ADC12 (see Note 6)                                       | ADC12IFG (see Notes 1 and 2)                                                               | Maskable                                        | 0FFEEh       | 23          |
| Timer_A3                                                 | TACCR0 CCIFG0 (see Note 2)                                                                 | Maskable                                        | 0FFECCh      | 22          |
| Timer_A3                                                 | TACCR1 CCIFG1 and TACCR2 CCIFG2,<br>TAIFG (see Notes 1 and 2)                              | Maskable                                        | 0FFEAh       | 21          |
| I/O Port P1 (Eight Flags)                                | P1IFG.0 to P1IFG.7 (see Notes 1 and 2)                                                     | Maskable                                        | 0FFE8h       | 20          |
| USART1 Receive                                           | URXIFG1                                                                                    | Maskable                                        | 0FFE6h       | 19          |
| USART1 Transmit                                          | UTXIFG1                                                                                    | Maskable                                        | 0FFE4h       | 18          |
| I/O Port P2 (Eight Flags)                                | P2IFG.0 to P2IFG.7 (see Notes 1 and 2)                                                     | Maskable                                        | 0FFE2h       | 17          |
| Basic Timer1/RTC                                         | BTIFG                                                                                      | Maskable                                        | 0FFE0h       | 16          |
| DMA                                                      | DMA0IFG, DMA1IFG, DMA2IFG<br>(see Notes 1 and 2)                                           | Maskable                                        | 0FFDEh       | 15          |
| Reserved                                                 | Reserved                                                                                   | Maskable                                        | 0FFDCh       | 14          |
| Reserved                                                 | Reserved (see Note 4)                                                                      |                                                 | 0FFDAh       | 13          |
|                                                          |                                                                                            |                                                 | ...          | ...         |
|                                                          |                                                                                            |                                                 | 0FFC0h       | 0, lowest   |

- NOTES:
- Multiple source flags
  - Interrupt flags are located in the module.
  - A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh).  
(Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
  - The interrupt vectors at addresses 0FFDAh to 0FFC0h are not used in this device and can be used for regular program code if necessary.
  - Access and key violations, KEYV and ACCVIFG, only applicable to F devices.
  - ADC12 is not implemented in MSP430x461x1 devices.

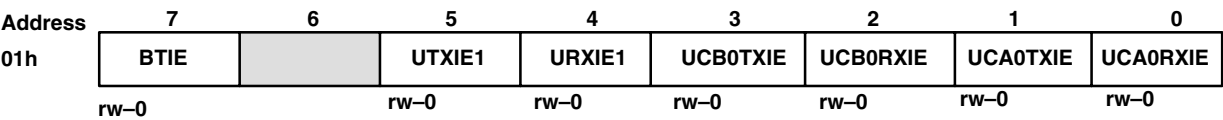
special function registers (SFRs)

The MSP430 SFRs are located in the lowest address space and are organized as byte mode registers. SFRs should be accessed with byte instructions.

interrupt enable 1 and 2



- WDTIE      Watchdog-timer interrupt enable. Inactive if watchdog mode is selected.  
            Active if watchdog timer is configured as a general-purpose timer.
- OFIE      Oscillator-fault-interrupt enable
- NMIIE      Nonmaskable-interrupt enable
- ACCVIE      Flash access violation interrupt enable



- UCA0RXIE      USCI\_A0 receive-interrupt enable
- UCA0TXIE      USCI\_A0 transmit-interrupt enable
- UCB0RXIE      USCI\_B0 receive-interrupt enable
- UCB0TXIE      USCI\_B0 transmit-interrupt enable
- URXIE1      USART1 UART and SPI receive-interrupt enable
- UTXIE1      USART1 UART and SPI transmit-interrupt enable
- BTIE      Basic timer interrupt enable

## interrupt flag register 1 and 2

| Address | 7 | 6 | 5 | 4      | 3 | 2 | 1     | 0      |
|---------|---|---|---|--------|---|---|-------|--------|
| 02h     |   |   |   | NMIIFG |   |   | OFIFG | WDTIFG |
|         |   |   |   | rw-0   |   |   | rw-1  | rw-(0) |

- WDTIFG: Set on watchdog timer overflow (in watchdog mode) or security key violation  
Reset on  $V_{CC}$  power-on or a reset condition at the  $\overline{RST}/NMI$  pin in reset mode
- OFIFG: Flag set on oscillator fault
- NMIIFG: Set via  $\overline{RST}/NMI$  pin

| Address | 7     | 6 | 5       | 4       | 3         | 2         | 1         | 0         |
|---------|-------|---|---------|---------|-----------|-----------|-----------|-----------|
| 03h     | BTIFG |   | UTXIFG1 | URXIFG1 | UCB0TXIFG | UCB0RXIFG | UCA0TXIFG | UCA0RXIFG |
|         | rw-0  |   | rw-1    | rw-0    | rw-0      | rw-0      | rw-0      | rw-0      |

- UCA0RXIFG USCI\_A0 receive-interrupt flag
- UCA0TXIFG USCI\_A0 transmit-interrupt flag
- UCB0RXIFG USCI\_B0 receive-interrupt flag
- UCB0TXIFG USCI\_B0 transmit-interrupt flag
- URXIFG0: USART1: UART and SPI receive flag
- UTXIFG0: USART1: UART and SPI transmit flag
- BTIFG: Basic timer flag

## module enable registers 1 and 2

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|---|
| 04h     |   |   |   |   |   |   |   |   |

| Address | 7 | 6 | 5     | 4               | 3 | 2 | 1 | 0 |
|---------|---|---|-------|-----------------|---|---|---|---|
| 05h     |   |   | UTXE1 | URXE1<br>USPIE1 |   |   |   |   |
|         |   |   | rw-0  | rw-0            |   |   |   |   |

- URXE1: USART1: UART mode receive enable
- UTXE1: USART1: UART mode transmit enable
- USPIE1: USART1: SPI mode transmit and receive enable

- Legend**
- rw:** Bit can be read and written.
- rw-0,1:** Bit can be read and written. It is Reset or Set by PUC.
- rw-(0,1):** Bit can be read and written. It is Reset or Set by POR.
-  SFR bit is not present in device

# MSP430x461x1, MSP430x461x MIXED SIGNAL MICROCONTROLLER

## memory organization

|                                         |           | <b>MSP430F4616<br/>MSP430F46161</b> | <b>MSP430F4617<br/>MSP430F46171</b> | <b>MSP430F4618<br/>MSP430F46181</b> | <b>MSP430F4619<br/>MSP430F46191</b> |
|-----------------------------------------|-----------|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|
| Memory                                  | Size      | 92KB                                | 92KB                                | 116KB                               | 120KB                               |
| Main: interrupt vector                  | Flash     | 0FFFFh – 0FFC0h                     | 0FFFFh – 0FFC0h                     | 0FFFFh – 0FFC0h                     | 0FFFFh – 0FFC0h                     |
| Main: code memory                       | Flash     | 018FFFh – 002100h                   | 019FFFh – 003100h                   | 01FFFFh – 003100h                   | 01FFFFh – 002100h                   |
| RAM (Total)                             | Size      | 4KB                                 | 8KB                                 | 8KB                                 | 4KB                                 |
|                                         |           | 020FFh – 01100h                     | 030FFh – 01100h                     | 030FFh – 01100h                     | 020FFh – 01100h                     |
| Extended                                | Size      | 2KB                                 | 6KB                                 | 6KB                                 | 2KB                                 |
|                                         |           | 020FFh – 01900h                     | 030FFh – 01900h                     | 030FFh – 01900h                     | 020FFh – 01900h                     |
| Mirrored                                | Size      | 2KB                                 | 2KB                                 | 2KB                                 | 2KB                                 |
|                                         |           | 018FFh – 01100h                     | 018FFh – 01100h                     | 018FFh – 01100h                     | 018FFh – 01100h                     |
| Information memory                      | Size      | 256 Byte                            | 256 Byte                            | 256 Byte                            | 256 Byte                            |
|                                         | Flash     | 010FFh – 01000h                     | 010FFh – 01000h                     | 010FFh – 01000h                     | 010FFh – 01000h                     |
| Boot memory                             | Size      | 1KB                                 | 1KB                                 | 1KB                                 | 1KB                                 |
|                                         | ROM       | 0FFFh – 0C00h                       | 0FFFh – 0C00h                       | 0FFFh – 0C00h                       | 0FFFh – 0C00h                       |
| RAM<br>(mirrored at<br>018FFh – 01100h) | Size      | 2KB                                 | 2KB                                 | 2KB                                 | 2KB                                 |
|                                         |           | 09FFh – 0200h                       | 09FFh – 0200h                       | 09FFh – 0200h                       | 09FFh – 0200h                       |
| Peripherals                             | 16 bit    | 01FFh – 0100h                       | 01FFh – 0100h                       | 01FFh – 0100h                       | 01FFh – 0100h                       |
|                                         | 8 bit     | 0FFh – 010h                         | 0FFh – 010h                         | 0FFh – 010h                         | 0FFh – 010h                         |
|                                         | 8-bit SFR | 0Fh – 00h                           | 0Fh – 00h                           | 0Fh – 00h                           | 0Fh – 00h                           |

## bootstrap loader (BSL)

The MSP430 BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. A bootstrap loader security key is provided at address 0FFBEh to disable the BSL completely or to disable the erasure of the flash if an invalid password is supplied. The BSL is optional for ROM-based devices. For complete description of the features of the BSL and its implementation, see the application report *Features of the MSP430 Bootstrap Loader*, literature number SLAA089.

| BSLKEY          | DESCRIPTION                                                  |
|-----------------|--------------------------------------------------------------|
| 00000h          | Erasure of flash disabled if an invalid password is supplied |
| 0AA55h          | BSL disabled                                                 |
| any other value | BSL enabled                                                  |

| BSL FUNCTION  | PZ PACKAGE PINS |
|---------------|-----------------|
| Data Transmit | 87/A7 – P1.0    |
| Data Receive  | 86/E7 – P1.1    |

## flash memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0 to n. Segments A and B are also called *information memory*.
- New devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory prior to the first use.

## peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x4xx Family User's Guide*, literature number SLAU056.

## DMA controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC12 conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode without having to awaken to move data to or from a peripheral.

## oscillator and system clock

The clock system in the MSP430x461x(1) family of devices is supported by the FLL+ module, which includes support for a 32768-Hz watch crystal oscillator, an internal digitally controlled oscillator (DCO), and a high frequency crystal oscillator. The FLL+ clock module is designed to meet the requirements of both low system cost and low power consumption. The FLL+ features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6  $\mu$ s. The FLL+ module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high-frequency crystal
- Main clock (MCLK), the system clock used by the CPU
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, or ACLK/8

## brownout, supply voltage supervisor

The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The supply voltage supervisor (SVS) circuitry detects if the supply voltage drops below a user selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM, the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However,  $V_{CC}$  may not have ramped to  $V_{CC(min)}$  at that time. The user must insure the default FLL+ settings are not changed until  $V_{CC}$  reaches  $V_{CC(min)}$ . If desired, the SVS circuit can be used to determine when  $V_{CC}$  reaches  $V_{CC(min)}$ .

## digital I/O

There are ten 8-bit I/O ports implemented—ports P1 through P10:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Ports P7/P8 and P9/P10 can be accessed word-wise as ports PA and PB respectively.

## Basic Timer1 and Real-Time Clock (RTC)

The Basic Timer1 has two independent 8-bit timers that can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. Basic Timer1 is extended to provide an integrated real-time clock (RTC). An internal calendar compensates for months with less than 31 days and includes leap-year correction.

### **LCD\_A drive with regulated charge pump**

The LCD\_A driver generates the segment and common signals required to drive an LCD display. The LCD\_A controller has dedicated data memory to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-MUX, 3-MUX, and 4-MUX LCDs are supported by this peripheral. The module can provide a LCD voltage independent of the supply voltage with its integrated charge pump. Furthermore it is possible to control the level of the LCD voltage and, thus, contrast by software.

### **watchdog timer (WDT+)**

The primary function of the WDT+ module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

### **universal serial communication interface (USCI)**

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols like SPI (3 or 4 pin), I2C and asynchronous communication protocols like UART, enhanced UART with automatic baudrate detection, and IrDA.

The USCI\_A0 module provides support for SPI (3 or 4 pin), UART, enhanced UART and IrDA.

The USCI\_B0 module provides support for SPI (3 or 4 pin) and I2C.

### **USART1**

The hardware universal synchronous/asynchronous receive transmit (USART) peripheral module is used for serial data communication. The USART supports synchronous SPI (3 or 4 pin) and asynchronous UART communication protocols, using double-buffered transmit and receive channels.

### **hardware multiplier**

The multiplication operation is supported by a dedicated peripheral module. The module performs  $16 \times 16$ ,  $16 \times 8$ ,  $8 \times 16$ , and  $8 \times 8$  bit operations. The module is capable of supporting signed and unsigned multiplication, as well as signed and unsigned multiply and accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

## Timer\_A3

Timer\_A3 is a 16-bit timer/counter with three capture/compare registers. Timer\_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer\_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

| TIMER_A3 SIGNAL CONNECTIONS |                        |                      |                 |                            |                      |
|-----------------------------|------------------------|----------------------|-----------------|----------------------------|----------------------|
| INPUT PIN<br>NUMBER         | DEVICE INPUT<br>SIGNAL | MODULE INPUT<br>NAME | MODULE<br>BLOCK | MODULE<br>OUTPUT<br>SIGNAL | OUTPUT PIN<br>NUMBER |
| PZ                          |                        |                      |                 |                            | PZ                   |
| 82/B9 - P1.5                | TACLK                  | TACLK                | Timer           | NA                         |                      |
|                             | ACLK                   | ACLK                 |                 |                            |                      |
|                             | SMCLK                  | SMCLK                |                 |                            |                      |
| 82/B9 - P1.5                | TACLK                  | INCLK                | CCR0            | TA0                        |                      |
| 87/A7 - P1.0                | TA0                    | CCI0A                |                 |                            | 87/A7 - P1.0         |
| 86/E7 - P1.1                | TA0                    | CCI0B                |                 |                            |                      |
|                             | DV <sub>SS</sub>       | GND                  |                 |                            |                      |
|                             | DV <sub>CC</sub>       | V <sub>CC</sub>      | CCR1            | TA1                        |                      |
| 85/D7 - P1.2                | TA1                    | CCI1A                |                 |                            | 85/D7 - P1.2         |
|                             | CAOUT (internal)       | CCI1B                |                 |                            | ADC12 (internal)     |
|                             | DV <sub>SS</sub>       | GND                  |                 |                            |                      |
|                             | DV <sub>CC</sub>       | V <sub>CC</sub>      | CCR2            | TA2                        |                      |
| 79/A10 - P2.0               | TA2                    | CCI2A                |                 |                            | 79/A10 - P2.0        |
|                             | ACLK (internal)        | CCI2B                |                 |                            |                      |
|                             | DV <sub>SS</sub>       | GND                  |                 |                            |                      |
|                             | DV <sub>CC</sub>       | V <sub>CC</sub>      |                 |                            |                      |

## Timer\_B7

Timer\_B7 is a 16-bit timer/counter with seven capture/compare registers. Timer\_B7 can support multiple capture/compares, PWM outputs, and interval timing. Timer\_B7 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

| TIMER_B7 SIGNAL CONNECTIONS |                     |                   |              |                      |                   |
|-----------------------------|---------------------|-------------------|--------------|----------------------|-------------------|
| INPUT PIN NUMBER            | DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | OUTPUT PIN NUMBER |
| PZ                          |                     |                   |              |                      | PZ                |
| 83/B8 - P1.4                | TBCLK               | TBCLK             | Timer        | NA                   |                   |
|                             | ACLK                | ACLK              |              |                      |                   |
|                             | SMCLK               | SMCLK             |              |                      |                   |
| 83/B8 - P1.4                | TBCLK               | INCLK             |              |                      |                   |
| 78/D8 - P2.1                | TB0                 | CCI0A             | CCR0         | TB0                  | 78/D8 - P2.1      |
| 78/D8 - P2.1                | TB0                 | CCI0B             |              |                      | ADC12 (internal)  |
|                             | DV <sub>SS</sub>    | GND               |              |                      |                   |
|                             | DV <sub>CC</sub>    | V <sub>CC</sub>   |              |                      |                   |
| 77/E8 - P2.2                | TB1                 | CCI1A             | CCR1         | TB1                  | 77/E8 - P2.2      |
| 77/E8 - P2.2                | TB1                 | CCI1B             |              |                      | ADC12 (internal)  |
|                             | DV <sub>SS</sub>    | GND               |              |                      |                   |
|                             | DV <sub>CC</sub>    | V <sub>CC</sub>   |              |                      |                   |
| 76/A11 - P2.3               | TB2                 | CCI2A             | CCR2         | TB2                  | 76/A11 - P2.3     |
| 76/A11 - P2.3               | TB2                 | CCI2B             |              |                      |                   |
|                             | DV <sub>SS</sub>    | GND               |              |                      |                   |
|                             | DV <sub>CC</sub>    | V <sub>CC</sub>   |              |                      |                   |
| 67/E12 - P3.4               | TB3                 | CCI3A             | CCR3         | TB3                  | 67/E12 - P3.4     |
| 67/E12 - P3.4               | TB3                 | CCI3B             |              |                      |                   |
|                             | DV <sub>SS</sub>    | GND               |              |                      |                   |
|                             | DV <sub>CC</sub>    | V <sub>CC</sub>   |              |                      |                   |
| 66/G9 - P3.5                | TB4                 | CCI4A             | CCR4         | TB4                  | 66/G9 - P3.5      |
| 66/G9 - P3.5                | TB4                 | CCI4B             |              |                      |                   |
|                             | DV <sub>SS</sub>    | GND               |              |                      |                   |
|                             | DV <sub>CC</sub>    | V <sub>CC</sub>   |              |                      |                   |
| 65/F11 - P3.6               | TB5                 | CCI5A             | CCR5         | TB5                  | 65/F11 - P3.6     |
| 65/F11 - P3.6               | TB5                 | CCI5B             |              |                      |                   |
|                             | DV <sub>SS</sub>    | GND               |              |                      |                   |
|                             | DV <sub>CC</sub>    | V <sub>CC</sub>   |              |                      |                   |
| 64/F12 - P3.7               | TB6                 | CCI6A             | CCR6         | TB6                  | 64/F12 - P3.7     |
|                             | ACLK (internal)     | CCI6B             |              |                      |                   |
|                             | DV <sub>SS</sub>    | GND               |              |                      |                   |
|                             | DV <sub>CC</sub>    | V <sub>CC</sub>   |              |                      |                   |

### **Comparator\_A**

The primary function of the comparator\_A module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

### **ADC12 (MSP430x461x Only)**

The ADC12 module supports fast, 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator and a 16 word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

**peripheral file map**

| <b>PERIPHERALS WITH WORD ACCESS</b> |                                       |         |       |
|-------------------------------------|---------------------------------------|---------|-------|
| <b>Watchdog+</b>                    | Watchdog timer control                | WDTCTL  | 0120h |
| <b>Timer_B7</b>                     | Capture/compare register 6            | TBCCR6  | 019Eh |
|                                     | Capture/compare register 5            | TBCCR5  | 019Ch |
|                                     | Capture/compare register 4            | TBCCR4  | 019Ah |
|                                     | Capture/compare register 3            | TBCCR3  | 0198h |
|                                     | Capture/compare register 2            | TBCCR2  | 0196h |
|                                     | Capture/compare register 1            | TBCCR1  | 0194h |
|                                     | Capture/compare register 0            | TBCCR0  | 0192h |
|                                     | Timer_B register                      | TBR     | 0190h |
|                                     | Capture/compare control 6             | TBCCTL6 | 018Eh |
|                                     | Capture/compare control 5             | TBCCTL5 | 018Ch |
|                                     | Capture/compare control 4             | TBCCTL4 | 018Ah |
|                                     | Capture/compare control 3             | TBCCTL3 | 0188h |
|                                     | Capture/compare control 2             | TBCCTL2 | 0186h |
|                                     | Capture/compare control 1             | TBCCTL1 | 0184h |
|                                     | Capture/compare control 0             | TBCCTL0 | 0182h |
|                                     | Timer_B control                       | TBCTL   | 0180h |
|                                     | Timer_B interrupt vector              | TBIV    | 011Eh |
| <b>Timer_A3</b>                     | Capture/compare register 2            | TACCR2  | 0176h |
|                                     | Capture/compare register 1            | TACCR1  | 0174h |
|                                     | Capture/compare register 0            | TACCR0  | 0172h |
|                                     | Timer_A register                      | TAR     | 0170h |
|                                     | Capture/compare control 2             | TACCTL2 | 0166h |
|                                     | Capture/compare control 1             | TACCTL1 | 0164h |
|                                     | Capture/compare control 0             | TACCTL0 | 0162h |
|                                     | Timer_A control                       | TACTL   | 0160h |
|                                     | Timer_A interrupt vector              | TAIV    | 012Eh |
| <b>Hardware Multiplier</b>          | Sum extend                            | SUMEXT  | 013Eh |
|                                     | Result high word                      | RESHI   | 013Ch |
|                                     | Result low word                       | RESLO   | 013Ah |
|                                     | Second operand                        | OP2     | 0138h |
|                                     | Multiply signed + accumulate/operand1 | MACS    | 0136h |
|                                     | Multiply + accumulate/operand1        | MAC     | 0134h |
|                                     | Multiply signed/operand1              | MPYS    | 0132h |
|                                     | Multiply unsigned/operand1            | MPY     | 0130h |
| <b>Flash</b><br>(F devices only)    | Flash control 3                       | FCTL3   | 012Ch |
|                                     | Flash control 2                       | FCTL2   | 012Ah |
|                                     | Flash control 1                       | FCTL1   | 0128h |

# MSP430x461x1, MSP430x461x MIXED SIGNAL MICROCONTROLLER

## peripheral file map (continued)

| PERIPHERALS WITH WORD ACCESS (CONTINUED) |                                   |         |       |
|------------------------------------------|-----------------------------------|---------|-------|
| <b>DMA</b>                               | DMA module control 0              | DMACTL0 | 0122h |
|                                          | DMA module control 1              | DMACTL1 | 0124h |
|                                          | DMA interrupt vector              | DMAIV   | 0126h |
| <b>DMA Channel 0</b>                     | DMA channel 0 control             | DMA0CTL | 01D0h |
|                                          | DMA channel 0 source address      | DMA0SA  | 01D2h |
|                                          | DMA channel 0 destination address | DMA0DA  | 01D6h |
|                                          | DMA channel 0 transfer size       | DMA0SZ  | 01DAh |
| <b>DMA Channel 1</b>                     | DMA channel 1 control             | DMA1CTL | 01DCh |
|                                          | DMA channel 1 source address      | DMA1SA  | 01DEh |
|                                          | DMA channel 1 destination address | DMA1DA  | 01E2h |
|                                          | DMA channel 1 transfer size       | DMA1SZ  | 01E6h |
| <b>DMA Channel 2</b>                     | DMA channel 2 control             | DMA2CTL | 01E8h |
|                                          | DMA channel 2 source address      | DMA2SA  | 01EAh |
|                                          | DMA channel 2 destination address | DMA2DA  | 01EEh |
|                                          | DMA channel 2 transfer size       | DMA2SZ  | 01F2h |



**peripheral file map (continued)**

| <b>PERIPHERALS WITH WORD ACCESS (CONTINUED)</b>                                         |                                |            |       |
|-----------------------------------------------------------------------------------------|--------------------------------|------------|-------|
| <b>ADC12</b><br><i>See also Peripherals<br/>With Byte Access<br/>(MSP430x461x only)</i> | Conversion memory 15           | ADC12MEM15 | 015Eh |
|                                                                                         | Conversion memory 14           | ADC12MEM14 | 015Ch |
|                                                                                         | Conversion memory 13           | ADC12MEM13 | 015Ah |
|                                                                                         | Conversion memory 12           | ADC12MEM12 | 0158h |
|                                                                                         | Conversion memory 11           | ADC12MEM11 | 0156h |
|                                                                                         | Conversion memory 10           | ADC12MEM10 | 0154h |
|                                                                                         | Conversion memory 9            | ADC12MEM9  | 0152h |
|                                                                                         | Conversion memory 8            | ADC12MEM8  | 0150h |
|                                                                                         | Conversion memory 7            | ADC12MEM7  | 014Eh |
|                                                                                         | Conversion memory 6            | ADC12MEM6  | 014Ch |
|                                                                                         | Conversion memory 5            | ADC12MEM5  | 014Ah |
|                                                                                         | Conversion memory 4            | ADC12MEM4  | 0148h |
|                                                                                         | Conversion memory 3            | ADC12MEM3  | 0146h |
|                                                                                         | Conversion memory 2            | ADC12MEM2  | 0144h |
|                                                                                         | Conversion memory 1            | ADC12MEM1  | 0142h |
|                                                                                         | Conversion memory 0            | ADC12MEM0  | 0140h |
|                                                                                         | Interrupt-vector-word register | ADC12IV    | 01A8h |
|                                                                                         | Inerrupt-enable register       | ADC12IE    | 01A6h |
|                                                                                         | Inerrupt-flag register         | ADC12IFG   | 01A4h |
|                                                                                         | Control register 1             | ADC12CTL1  | 01A2h |
|                                                                                         | Control register 0             | ADC12CTL0  | 01A0h |
| <b>Port PA</b>                                                                          | Port PA selection              | PASEL      | 03Eh  |
|                                                                                         | Port PA direction              | PADIR      | 03Ch  |
|                                                                                         | Port PA output                 | PAOUT      | 03Ah  |
|                                                                                         | Port PA input                  | PAIN       | 038h  |
| <b>Port PB</b>                                                                          | Port PB selection              | PBSEL      | 00Eh  |
|                                                                                         | Port PB direction              | PBDIR      | 00Ch  |
|                                                                                         | Port PB output                 | PBOUT      | 00Ah  |
|                                                                                         | Port PB input                  | PBIN       | 008h  |

# MSP430x461x1, MSP430x461x MIXED SIGNAL MICROCONTROLLER

## peripheral file map (continued)

| PERIPHERALS WITH BYTE ACCESS                                                         |                                |             |      |
|--------------------------------------------------------------------------------------|--------------------------------|-------------|------|
| <b>LCD_A</b>                                                                         | LCD Voltage Control 1          | LCDVCTL1    | 0AFh |
|                                                                                      | LCD Voltage Control 0          | LCDVCTL0    | 0AEh |
|                                                                                      | LCD Voltage Port Control 1     | LCDAPCTL1   | 0ADh |
|                                                                                      | LCD Voltage Port Control 0     | LCDAPCTL0   | 0ACh |
|                                                                                      | LCD memory 20                  | LCDM20      | 0A4h |
|                                                                                      | :                              | :           | :    |
|                                                                                      | LCD memory 16                  | LCDM16      | 0A0h |
|                                                                                      | LCD memory 15                  | LCDM15      | 09Fh |
|                                                                                      | :                              | :           | :    |
|                                                                                      | LCD memory 1                   | LCDM1       | 091h |
|                                                                                      | LCD control and mode           | LCDCTL      | 090h |
| <b>ADC12</b><br>(Memory control registers require byte access)<br>(MSP430x461x only) | ADC memory-control register 15 | ADC12MCTL15 | 08Fh |
|                                                                                      | ADC memory-control register 14 | ADC12MCTL14 | 08Eh |
|                                                                                      | ADC memory-control register 13 | ADC12MCTL13 | 08Dh |
|                                                                                      | ADC memory-control register 12 | ADC12MCTL12 | 08Ch |
|                                                                                      | ADC memory-control register 11 | ADC12MCTL11 | 08Bh |
|                                                                                      | ADC memory-control register 10 | ADC12MCTL10 | 08Ah |
|                                                                                      | ADC memory-control register 9  | ADC12MCTL9  | 089h |
|                                                                                      | ADC memory-control register 8  | ADC12MCTL8  | 088h |
|                                                                                      | ADC memory-control register 7  | ADC12MCTL7  | 087h |
|                                                                                      | ADC memory-control register 6  | ADC12MCTL6  | 086h |
|                                                                                      | ADC memory-control register 5  | ADC12MCTL5  | 085h |
|                                                                                      | ADC memory-control register 4  | ADC12MCTL4  | 084h |
|                                                                                      | ADC memory-control register 3  | ADC12MCTL3  | 083h |
|                                                                                      | ADC memory-control register 2  | ADC12MCTL2  | 082h |
|                                                                                      | ADC memory-control register 1  | ADC12MCTL1  | 081h |
|                                                                                      | ADC memory-control register 0  | ADC12MCTL0  | 080h |
| <b>USART1</b>                                                                        | Transmit buffer                | U1TXBUF     | 07Fh |
|                                                                                      | Receive buffer                 | U1RXBUF     | 07Eh |
|                                                                                      | Baud rate                      | U1BR1       | 07Dh |
|                                                                                      | Baud rate                      | U1BR0       | 07Ch |
|                                                                                      | Modulation control             | U1MCTL      | 07Bh |
|                                                                                      | Receive control                | U1RCTL      | 07Ah |
|                                                                                      | Transmit control               | U1TCTL      | 079h |
|                                                                                      | USART control                  | U1CTL       | 078h |

**peripheral file map (continued)**

| <b>PERIPHERALS WITH BYTE ACCESS (CONTINUED)</b> |                                                 |           |       |
|-------------------------------------------------|-------------------------------------------------|-----------|-------|
| <b>USCI</b>                                     | USCI I2C Slave Address                          | UCBI2CSA  | 011Ah |
|                                                 | USCI I2C Own Address                            | UCBI2COA  | 0118h |
|                                                 | USCI Synchronous Transmit Buffer                | UCBTXBUF  | 06Fh  |
|                                                 | USCI Synchronous Receive Buffer                 | UCBRXBUF  | 06Eh  |
|                                                 | USCI Synchronous Status                         | UCBSTAT   | 06Dh  |
|                                                 | USCI I2C Interrupt Enable                       | UCBI2CIE  | 06Ch  |
|                                                 | USCI Synchronous Bit Rate 1                     | UCBBR1    | 06Bh  |
|                                                 | USCI Synchronous Bit Rate 0                     | UCBBR0    | 06Ah  |
|                                                 | USCI Synchronous Control 1                      | UCBCTL1   | 069h  |
|                                                 | USCI Synchronous Control 0                      | UCBCTL0   | 068h  |
|                                                 | USCI Transmit Buffer                            | UCATXBUF  | 067h  |
|                                                 | USCI Receive Buffer                             | UCARXBUF  | 066h  |
|                                                 | USCI Status                                     | UCASTAT   | 065h  |
|                                                 | USCI Modulation Control                         | UCAMCTL   | 064h  |
|                                                 | USCI Baud Rate 1                                | UCABR1    | 063h  |
|                                                 | USCI Baud Rate 0                                | UCABR0    | 062h  |
|                                                 | USCI Control 1                                  | UCACTL1   | 061h  |
|                                                 | USCI Control 0                                  | UCACTL0   | 060h  |
|                                                 | USCI IrDA Receive Control                       | UCAIRRCTL | 05Fh  |
|                                                 | USCI IrDA Transmit Control                      | UCAIRTCTL | 05Eh  |
|                                                 | USCI LIN Control                                | UCAABCTL  | 05Dh  |
| <b>Comparator_A</b>                             | Comparator_A port disable                       | CAPD      | 05Bh  |
|                                                 | Comparator_A control 2                          | CACTL2    | 05Ah  |
|                                                 | Comparator_A control 1                          | CACTL1    | 059h  |
| <b>BrownOUT, SVS</b>                            | SVS control register (Reset by brownout signal) | SVSCTL    | 056h  |
| <b>FLL+Clock</b>                                | FLL+ Control 1                                  | FLL_CTL1  | 054h  |
|                                                 | FLL+ Control 0                                  | FLL_CTL0  | 053h  |
|                                                 | System clock frequency control                  | SCFQCTL   | 052h  |
|                                                 | System clock frequency integrator               | SCFI1     | 051h  |
|                                                 | System clock frequency integrator               | SCFI0     | 050h  |
| <b>RTC (Basic Timer 1)</b>                      | Real Time Clock Year High Byte                  | RTCYEARH  | 04Fh  |
|                                                 | Real Time Clock Year Low Byte                   | RTCYEARL  | 04Eh  |
|                                                 | Real Time Clock Month                           | RTCMON    | 04Dh  |
|                                                 | Real Time Clock Day of Month                    | RTCDAY    | 04Ch  |
|                                                 | Basic Timer1 Counter 2                          | BTCNT2    | 047h  |
|                                                 | Basic Timer1 Counter 1                          | BTCNT1    | 046h  |
|                                                 | Real Time Counter 4                             | RTCNT4    | 045h  |
|                                                 | (Real Time Clock Day of Week)                   | (RTCDOW)  |       |
|                                                 | Real Time Counter 3                             | RTCNT3    | 044h  |
|                                                 | (Real Time Clock Hour)                          | (RTCHOUR) |       |
|                                                 | Real Time Counter 2                             | RTCNT2    | 043h  |
|                                                 | (Real Time Clock Minute)                        | (RTCMIN)  |       |
|                                                 | Real Time Counter 1                             | RTCNT1    | 042h  |
|                                                 | (Real Time Clock Second)                        | (RTCSEC)  |       |
|                                                 | Real Time Clock Control                         | RTCCTL    | 041h  |
|                                                 | Basic Timer1 Control                            | BTCTL     | 040h  |

# MSP430x461x1, MSP430x461x MIXED SIGNAL MICROCONTROLLER

## peripheral file map (continued)

| PERIPHERALS WITH BYTE ACCESS (CONTINUED) |                               |        |      |
|------------------------------------------|-------------------------------|--------|------|
| <b>Port P10</b>                          | Port P10 selection            | P10SEL | 00Fh |
|                                          | Port P10 direction            | P10DIR | 00Dh |
|                                          | Port P10 output               | P10OUT | 00Bh |
|                                          | Port P10 input                | P10IN  | 009h |
| <b>Port P9</b>                           | Port P9 selection             | P9SEL  | 00Eh |
|                                          | Port P9 direction             | P9DIR  | 00Ch |
|                                          | Port P9 output                | P9OUT  | 00Ah |
|                                          | Port P9 input                 | P9IN   | 008h |
| <b>Port P8</b>                           | Port P8 selection             | P8SEL  | 03Fh |
|                                          | Port P8 direction             | P8DIR  | 03Dh |
|                                          | Port P8 output                | P8OUT  | 03Bh |
|                                          | Port P8 input                 | P8IN   | 039h |
| <b>Port P7</b>                           | Port P7 selection             | P7SEL  | 03Eh |
|                                          | Port P7 direction             | P7DIR  | 03Ch |
|                                          | Port P7 output                | P7OUT  | 03Ah |
|                                          | Port P7 input                 | P7IN   | 038h |
| <b>Port P6</b>                           | Port P6 selection             | P6SEL  | 037h |
|                                          | Port P6 direction             | P6DIR  | 036h |
|                                          | Port P6 output                | P6OUT  | 035h |
|                                          | Port P6 input                 | P6IN   | 034h |
| <b>Port P5</b>                           | Port P5 selection             | P5SEL  | 033h |
|                                          | Port P5 direction             | P5DIR  | 032h |
|                                          | Port P5 output                | P5OUT  | 031h |
|                                          | Port P5 input                 | P5IN   | 030h |
| <b>Port P4</b>                           | Port P4 selection             | P4SEL  | 01Fh |
|                                          | Port P4 direction             | P4DIR  | 01Eh |
|                                          | Port P4 output                | P4OUT  | 01Dh |
|                                          | Port P4 input                 | P4IN   | 01Ch |
| <b>Port P3</b>                           | Port P3 selection             | P3SEL  | 01Bh |
|                                          | Port P3 direction             | P3DIR  | 01Ah |
|                                          | Port P3 output                | P3OUT  | 019h |
|                                          | Port P3 input                 | P3IN   | 018h |
| <b>Port P2</b>                           | Port P2 selection             | P2SEL  | 02Eh |
|                                          | Port P2 interrupt enable      | P2IE   | 02Dh |
|                                          | Port P2 interrupt-edge select | P2IES  | 02Ch |
|                                          | Port P2 interrupt flag        | P2IFG  | 02Bh |
|                                          | Port P2 direction             | P2DIR  | 02Ah |
|                                          | Port P2 output                | P2OUT  | 029h |
|                                          | Port P2 input                 | P2IN   | 028h |
| <b>Port P1</b>                           | Port P1 selection             | P1SEL  | 026h |
|                                          | Port P1 interrupt enable      | P1IE   | 025h |
|                                          | Port P1 interrupt-edge select | P1IES  | 024h |
|                                          | Port P1 interrupt flag        | P1IFG  | 023h |
|                                          | Port P1 direction             | P1DIR  | 022h |
|                                          | Port P1 output                | P1OUT  | 021h |
|                                          | Port P1 input                 | P1IN   | 020h |

---

peripheral file map (continued)

| PERIPHERALS WITH BYTE ACCESS (CONTINUED) |                        |      |      |
|------------------------------------------|------------------------|------|------|
| Special functions                        | SFR module enable 2    | ME2  | 005h |
|                                          | SFR module enable 1    | ME1  | 004h |
|                                          | SFR interrupt flag 2   | IFG2 | 003h |
|                                          | SFR interrupt flag 1   | IFG1 | 002h |
|                                          | SFR interrupt enable 2 | IE2  | 001h |
|                                          | SFR interrupt enable 1 | IE1  | 000h |

# MSP430x461x1, MSP430x461x MIXED SIGNAL MICROCONTROLLER

## absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>

|                                                            |                            |
|------------------------------------------------------------|----------------------------|
| Voltage range applied at $V_{CC}$ to $V_{SS}$              | –0.3 V to 4.1 V            |
| Voltage range applied to any pin (see Note)                | –0.3 V to $V_{CC} + 0.3$ V |
| Diode current at any device terminal                       | ±2 mA                      |
| Storage temperature range, $T_{stg}$ : Unprogrammed device | –55°C to 150°C             |
| Programmed device                                          | –40°C to 85°C              |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltages referenced to  $V_{SS}$ . The JTAG fuse-blow voltage,  $V_{FB}$ , is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.

## recommended operating conditions

|                                                                                                                                          |                           | MIN               | NOM  | MAX    | UNITS |
|------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|-------------------|------|--------|-------|
| Supply voltage during program execution (see Note 1), $V_{CC}$ ( $AV_{CC} = DV_{CC1/2} = V_{CC}$ )                                       | MSP430x461x(1)            | 1.8               |      | 3.6    | V     |
| Supply voltage during flash memory programming (see Note 1), $V_{CC}$ ( $AV_{CC} = DV_{CC1/2} = V_{CC}$ )                                | MSP430F461x(1)            | 2.7               |      | 3.6    | V     |
| Supply voltage during program execution, SVS enabled and PORON = 1 (see Note 1 and Note 2), $V_{CC}$ ( $AV_{CC} = DV_{CC1/2} = V_{CC}$ ) | MSP430x461x(1)            | 2                 |      | 3.6    | V     |
| Supply voltage (see Note 1), $V_{SS}$ ( $AV_{SS} = DV_{SS1/2} = V_{SS}$ )                                                                |                           | 0                 |      | 0      | V     |
| Operating free-air temperature range, $T_A$                                                                                              | MSP430x461x(1)            | –40               |      | 85     | °C    |
| LFXT1 crystal frequency, $f_{(LFXT1)}$ (see Note 2)                                                                                      | LF selected, XTS_FLL = 0  | Watch crystal     |      | 32.768 | kHz   |
|                                                                                                                                          | XT1 selected, XTS_FLL = 1 | Ceramic resonator |      | 450    |       |
|                                                                                                                                          | XT1 selected, XTS_FLL = 1 | Crystal           |      | 1000   |       |
| XT2 crystal frequency, $f_{(XT2)}$                                                                                                       | Ceramic resonator         |                   | 450  | 8000   | kHz   |
|                                                                                                                                          | Crystal                   |                   | 1000 | 8000   |       |
| Processor frequency (signal MCLK), $f_{(System)}$                                                                                        | $V_{CC} = 1.8$ V          |                   | DC   | 3.0    | MHz   |
|                                                                                                                                          | $V_{CC} = 2.0$ V          |                   | DC   | 4.6    |       |
|                                                                                                                                          | $V_{CC} = 3.6$ V          |                   | DC   | 8.0    |       |

- NOTES: 1. It is recommended to power  $AV_{CC}$  and  $DV_{CC}$  from the same source. A maximum difference of 0.3 V between  $AV_{CC}$  and  $DV_{CC}$  can be tolerated during power up and operation.
2. The minimum operating supply voltage is defined according to the trip point where POR is going active by decreasing the supply voltage. POR is going inactive when the supply voltage is raised above the minimum supply voltage plus the hysteresis of the SVS circuitry.
3. In LF mode, the LFXT1 oscillator requires a watch crystal. In XT1 mode, LFXT1 accepts a ceramic resonator or a crystal.

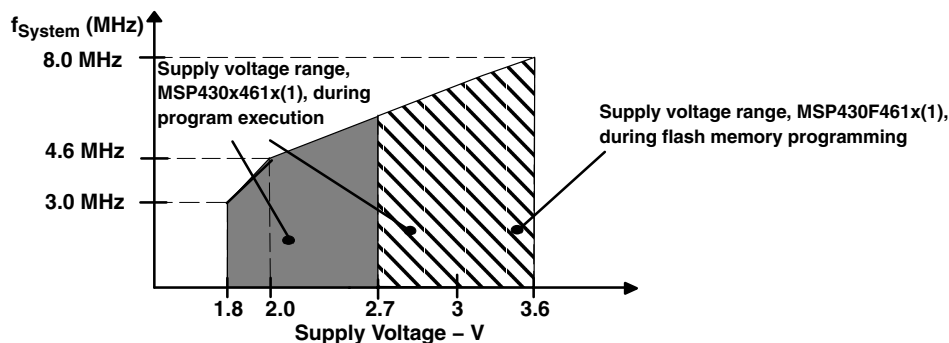


Figure 1. Frequency vs Supply Voltage, Typical Characteristic

**electrical characteristics over recommended operating free-air temperature (unless otherwise noted)**

**supply current into AV<sub>CC</sub> + DV<sub>CC</sub> excluding external current**

| PARAMETER           |                                                                                                                                                                                                                                                                                                    | TEST CONDITIONS        | V <sub>CC</sub>                | MIN                   | TYP  | MAX | UNIT |
|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|--------------------------------|-----------------------|------|-----|------|
| I <sub>(AM)</sub>   | Active mode (see Note 1 and Note 4)<br>f <sub>(MCLK)</sub> = f <sub>(SMCLK)</sub> = 1 MHz,<br>f <sub>(ACLK)</sub> = 32,768 Hz<br>XTS=0, SELM=(0,1)<br>(F461x(1): Program executes from flash)                                                                                                      | C461x(1)               | T <sub>A</sub> = −40°C to 85°C | 2.2 V                 | 280  | 370 | μA   |
|                     |                                                                                                                                                                                                                                                                                                    |                        | 3 V                            | 470                   | 580  |     |      |
|                     |                                                                                                                                                                                                                                                                                                    | F461x(1)               | T <sub>A</sub> = −40°C to 85°C | 2.2 V                 | 400  | 480 | μA   |
|                     |                                                                                                                                                                                                                                                                                                    |                        | 3 V                            | 600                   | 740  |     |      |
| I <sub>(LPM0)</sub> | Low-power mode (LPM0)<br>(see Note 1 and Note 4)                                                                                                                                                                                                                                                   | x461x(1)               | T <sub>A</sub> = −40°C to 85°C | 2.2 V                 | 45   | 70  | μA   |
|                     |                                                                                                                                                                                                                                                                                                    |                        | 3 V                            | 75                    | 110  |     |      |
| I <sub>(LPM2)</sub> | Low-power mode (LPM2),<br>f <sub>(MCLK)</sub> = f <sub>(SMCLK)</sub> = 0 MHz,<br>f <sub>(ACLK)</sub> = 32,768 Hz, SCG0 = 0 (see Note 2 and Note 4)                                                                                                                                                 |                        | T <sub>A</sub> = −40°C to 85°C | 2.2 V                 | 11   | 20  | μA   |
|                     |                                                                                                                                                                                                                                                                                                    |                        | 3 V                            | 17                    | 24   |     |      |
| I <sub>(LPM3)</sub> | Low-power mode (LPM3)<br>f <sub>(MCLK)</sub> = f <sub>(SMCLK)</sub> = 0 MHz,<br>f <sub>(ACLK)</sub> = 32,768 Hz, SCG0 = 1<br>Basic Timer1 enabled, ACLK selected<br>LCD_A enabled, LCDCPEN = 0;<br>(static mode; f <sub>LCD</sub> = f <sub>(ACLK)</sub> /32)<br>(see Note 2 and Note 3 and Note 4) | T <sub>A</sub> = −40°C | 2.2 V                          | 1.3                   | 4.0  | μA  |      |
|                     |                                                                                                                                                                                                                                                                                                    |                        |                                | T <sub>A</sub> = 25°C | 1.3  |     | 4.0  |
|                     |                                                                                                                                                                                                                                                                                                    |                        |                                | T <sub>A</sub> = 60°C | 2.22 |     | 6.5  |
|                     |                                                                                                                                                                                                                                                                                                    |                        |                                | T <sub>A</sub> = 85°C | 6.5  |     | 15.0 |
|                     |                                                                                                                                                                                                                                                                                                    | T <sub>A</sub> = −40°C | 3 V                            | 1.9                   | 5.0  |     |      |
|                     |                                                                                                                                                                                                                                                                                                    |                        |                                | T <sub>A</sub> = 25°C | 1.9  |     | 5.0  |
|                     |                                                                                                                                                                                                                                                                                                    |                        |                                | T <sub>A</sub> = 60°C | 2.5  |     | 7.5  |
|                     |                                                                                                                                                                                                                                                                                                    |                        |                                | T <sub>A</sub> = 85°C | 7.5  |     | 18.0 |
| I <sub>(LPM3)</sub> | Low-power mode (LPM3)<br>f <sub>(MCLK)</sub> = f <sub>(SMCLK)</sub> = 0 MHz,<br>f <sub>(ACLK)</sub> = 32,768 Hz, SCG0 = 1<br>Basic Timer1 enabled, ACLK selected<br>LCD_A enabled, LCDCPEN = 0;<br>(4-mux mode; f <sub>LCD</sub> = f <sub>(ACLK)</sub> /32)<br>(see Note 2 and Note 3 and Note 4)  | T <sub>A</sub> = −40°C | 2.2 V                          | 1.5                   | 5.5  | μA  |      |
|                     |                                                                                                                                                                                                                                                                                                    |                        |                                | T <sub>A</sub> = 25°C | 1.5  |     | 5.5  |
|                     |                                                                                                                                                                                                                                                                                                    |                        |                                | T <sub>A</sub> = 60°C | 2.8  |     | 7.0  |
|                     |                                                                                                                                                                                                                                                                                                    |                        |                                | T <sub>A</sub> = 85°C | 7.2  |     | 17.0 |
|                     |                                                                                                                                                                                                                                                                                                    | T <sub>A</sub> = −40°C | 3 V                            | 2.5                   | 6.5  |     |      |
|                     |                                                                                                                                                                                                                                                                                                    |                        |                                | T <sub>A</sub> = 25°C | 2.5  |     | 6.5  |
|                     |                                                                                                                                                                                                                                                                                                    |                        |                                | T <sub>A</sub> = 60°C | 3.2  |     | 8.0  |
|                     |                                                                                                                                                                                                                                                                                                    |                        |                                | T <sub>A</sub> = 85°C | 8.5  |     | 20.0 |
| I <sub>(LPM4)</sub> | Low-power mode (LPM4)<br>f <sub>(MCLK)</sub> = 0 MHz, f <sub>(SMCLK)</sub> = 0 MHz,<br>f <sub>(ACLK)</sub> = 0 Hz, SCG0 = 1<br>(see Note 2 and Note 4)                                                                                                                                             | T <sub>A</sub> = −40°C | 2.2 V                          | 0.13                  | 1.0  | μA  |      |
|                     |                                                                                                                                                                                                                                                                                                    |                        |                                | T <sub>A</sub> = 25°C | 0.22 |     | 1.0  |
|                     |                                                                                                                                                                                                                                                                                                    |                        |                                | T <sub>A</sub> = 60°C | 0.9  |     | 2.5  |
|                     |                                                                                                                                                                                                                                                                                                    |                        |                                | T <sub>A</sub> = 85°C | 4.3  |     | 12.5 |
|                     |                                                                                                                                                                                                                                                                                                    | T <sub>A</sub> = −40°C | 3 V                            | 0.13                  | 1.6  |     |      |
|                     |                                                                                                                                                                                                                                                                                                    |                        |                                | T <sub>A</sub> = 25°C | 0.3  |     | 1.6  |
|                     |                                                                                                                                                                                                                                                                                                    |                        |                                | T <sub>A</sub> = 60°C | 1.1  |     | 3.0  |
|                     |                                                                                                                                                                                                                                                                                                    |                        |                                | T <sub>A</sub> = 85°C | 5.0  |     | 15.0 |

- NOTES: 1. Timer\_B is clocked by f<sub>(DCOCLK)</sub> = f<sub>(DCO)</sub> = 1 MHz. All inputs are tied to 0 V or to V<sub>CC</sub>. Outputs do not source or sink any current.  
2. All inputs are tied to 0 V or to V<sub>CC</sub>. Outputs do not source or sink any current.  
3. The LPM3 currents are characterized with a Micro Crystal CC4V-T1A (9 pF) crystal and OSCCAPx = 1h.  
4. Current for brownout included.

Current consumption of active mode versus system frequency, F version:

$$I_{(AM)} = I_{(AM)} [1 \text{ MHz}] \times f_{(\text{System})} [\text{MHz}]$$

Current consumption of active mode versus supply voltage, F version:

$$I_{(AM)} = I_{(AM)} [3 \text{ V}] + 200 \mu\text{A/V} \times (V_{\text{CC}} - 3 \text{ V})$$

# MSP430x461x1, MSP430x461x MIXED SIGNAL MICROCONTROLLER

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

## Schmitt-trigger inputs – Ports P1 to P10, $\overline{\text{RST}}/\text{NMI}$ , JTAG (TCK, TMS, TDI/TCLK, TDO/TDI)

| PARAMETER        |                                                                 | V <sub>CC</sub> | MIN | TYP | MAX  | UNIT |
|------------------|-----------------------------------------------------------------|-----------------|-----|-----|------|------|
| V <sub>IT+</sub> | Positive-going input threshold voltage                          | 2.2 V           | 1.1 |     | 1.55 | V    |
|                  |                                                                 | 3 V             | 1.5 |     | 1.98 |      |
| V <sub>IT–</sub> | Negative-going input threshold voltage                          | 2.2 V           | 0.4 |     | 0.9  | V    |
|                  |                                                                 | 3 V             | 0.9 |     | 1.3  |      |
| V <sub>hys</sub> | Input voltage hysteresis (V <sub>IT+</sub> – V <sub>IT–</sub> ) | 2.2 V           | 0.3 |     | 1.1  | V    |
|                  |                                                                 | 3 V             | 0.5 |     | 1    |      |

## inputs Px.x, TA<sub>x</sub>, TB<sub>x</sub>

| PARAMETER            |                                                            | TEST CONDITIONS                                                                         | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|----------------------|------------------------------------------------------------|-----------------------------------------------------------------------------------------|-----------------|-----|-----|-----|------|
| t <sub>(int)</sub>   | External interrupt timing                                  | Port P1, P2: P1.x to P2.x, external trigger signal for the interrupt flag, (see Note 1) | 2.2 V           | 62  |     |     | ns   |
|                      |                                                            |                                                                                         | 3 V             | 50  |     |     |      |
| t <sub>(cap)</sub>   | Timer_A, Timer_B capture timing                            | TA0, TA1, TA2<br>TB0, TB1, TB2, TB3, TB4, TB5, TB6                                      | 2.2 V           | 62  |     |     | ns   |
|                      |                                                            |                                                                                         | 3 V             | 50  |     |     |      |
| f <sub>(TAext)</sub> | Timer_A, Timer_B clock frequency externally applied to pin | TACLK, TBCLK, INCLK: t <sub>(H)</sub> = t <sub>(L)</sub>                                | 2.2 V           |     |     | 8   | MHz  |
| f <sub>(TBext)</sub> |                                                            |                                                                                         | 3 V             |     |     | 10  |      |
| f <sub>(TAint)</sub> | Timer_A, Timer_B clock frequency                           | SMCLK or ACLK signal selected                                                           | 2.2 V           |     |     | 8   | MHz  |
| f <sub>(TBint)</sub> |                                                            |                                                                                         | 3 V             |     |     | 10  |      |

NOTES: 1. The external signal sets the interrupt flag every time the minimum t<sub>(int)</sub> parameters are met. It may be set even with trigger signals shorter than t<sub>(int)</sub>.

## leakage current – Ports P1 to P10 (see Note 1)

| PARAMETER              |                 | TEST CONDITIONS                                                     | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|------------------------|-----------------|---------------------------------------------------------------------|-----------------|-----|-----|-----|------|
| I <sub>lkg(Px.y)</sub> | Leakage current | Port Px V <sub>(Px.y)</sub> (see Note 2)<br>(1 ≤ x ≤ 10, 0 ≤ y ≤ 7) | 2.2 V/3 V       |     |     | ±50 | nA   |

NOTES: 1. The leakage current is measured with V<sub>SS</sub> or V<sub>CC</sub> applied to the corresponding pin(s), unless otherwise noted.  
2. The port pin must be selected as input.

**electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)**

**outputs – Ports P1 to P10**

| PARAMETER                                 | TEST CONDITIONS                             | V <sub>CC</sub> | MIN                   | TYP | MAX                   | UNIT |
|-------------------------------------------|---------------------------------------------|-----------------|-----------------------|-----|-----------------------|------|
| V <sub>OH</sub> High-level output voltage | I <sub>OH(max)</sub> = –1.5 mA (see Note 1) | 2.2 V           | V <sub>CC</sub> –0.25 |     | V <sub>CC</sub>       | V    |
|                                           | I <sub>OH(max)</sub> = –6 mA (see Note 2)   | 2.2 V           | V <sub>CC</sub> –0.6  |     | V <sub>CC</sub>       |      |
|                                           | I <sub>OH(max)</sub> = –1.5 mA (see Note 1) | 3 V             | V <sub>CC</sub> –0.25 |     | V <sub>CC</sub>       |      |
|                                           | I <sub>OH(max)</sub> = –6 mA (see Note 2)   | 3 V             | V <sub>CC</sub> –0.6  |     | V <sub>CC</sub>       |      |
| V <sub>OL</sub> Low-level output voltage  | I <sub>OL(max)</sub> = 1.5 mA (see Note 1)  | 2.2 V           | V <sub>SS</sub>       |     | V <sub>SS</sub> +0.25 | V    |
|                                           | I <sub>OL(max)</sub> = 6 mA (see Note 2)    | 2.2 V           | V <sub>SS</sub>       |     | V <sub>SS</sub> +0.6  |      |
|                                           | I <sub>OL(max)</sub> = 1.5 mA, (see Note 1) | 3 V             | V <sub>SS</sub>       |     | V <sub>SS</sub> +0.25 |      |
|                                           | I <sub>OL(max)</sub> = 6 mA (see Note 2)    | 3 V             | V <sub>SS</sub>       |     | V <sub>SS</sub> +0.6  |      |

NOTES: 1. The maximum total current, I<sub>OH(max)</sub> and I<sub>OL(max)</sub>, for all outputs combined, should not exceed ±12 mA to satisfy the maximum specified voltage drop.  
2. The maximum total current, I<sub>OH(max)</sub> and I<sub>OL(max)</sub>, for all outputs combined, should not exceed ±48 mA to satisfy the maximum specified voltage drop.

**output frequency**

| PARAMETER                                                                    | TEST CONDITIONS                                                               | MIN                                                             | TYP | MAX           | UNIT          |
|------------------------------------------------------------------------------|-------------------------------------------------------------------------------|-----------------------------------------------------------------|-----|---------------|---------------|
| f <sub>(P<sub>x</sub>.y)</sub> (1 ≤ x ≤ 10, 0 ≤ y ≤ 7)                       | C <sub>L</sub> = 20 pF, V <sub>CC</sub> = 2.2 V                               | DC                                                              |     | 10            | MHz           |
|                                                                              | I <sub>L</sub> = ±1.5 mA, V <sub>CC</sub> = 3 V                               | DC                                                              |     | 12            | MHz           |
| f <sub>(MCLK)</sub> P1.1/TA0/MCLK,<br>f <sub>(SMCLK)</sub> P1.4/TBCLK/SMCLK, | C <sub>L</sub> = 20 pF                                                        | V <sub>CC</sub> = 2.2 V                                         |     | 10            | MHz           |
| f <sub>(ACLK)</sub> P1.5/TACLK/ACLK                                          |                                                                               | V <sub>CC</sub> = 3 V                                           |     | 12            | MHz           |
| t <sub>(Xdc)</sub> Duty cycle of output frequency                            | P1.5/TACLK/ACLK,<br>C <sub>L</sub> = 20 pF<br>V <sub>CC</sub> = 2.2 V / 3 V   | f <sub>(ACLK)</sub> = f <sub>(LFXT1)</sub> = f <sub>(XT1)</sub> |     | 40%           | 60%           |
|                                                                              |                                                                               | f <sub>(ACLK)</sub> = f <sub>(LFXT1)</sub> = f <sub>(LF)</sub>  |     | 30%           | 70%           |
|                                                                              |                                                                               | f <sub>(ACLK)</sub> = f <sub>(LFXT1)</sub>                      |     | 50%           |               |
|                                                                              | P1.1/TA0/MCLK,<br>C <sub>L</sub> = 20 pF,<br>V <sub>CC</sub> = 2.2 V / 3 V    | f <sub>(MCLK)</sub> = f <sub>(XT1)</sub>                        |     | 40%           | 60%           |
|                                                                              |                                                                               | f <sub>(MCLK)</sub> = f <sub>(DCOCLK)</sub>                     |     | 50%–<br>15 ns | 50%+<br>15 ns |
|                                                                              | P1.4/TBCLK/SMCLK,<br>C <sub>L</sub> = 20 pF,<br>V <sub>CC</sub> = 2.2 V / 3 V | f <sub>(SMCLK)</sub> = f <sub>(XT2)</sub>                       |     | 40%           | 60%           |
|                                                                              |                                                                               | f <sub>(SMCLK)</sub> = f <sub>(DCOCLK)</sub>                    |     | 50%–<br>15 ns | 50%+<br>15 ns |

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)  
typical characteristics – outputs

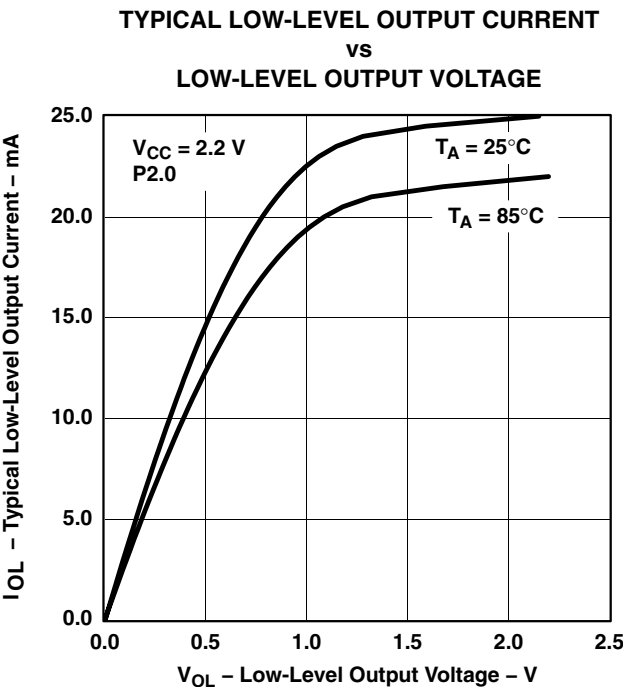


Figure 2

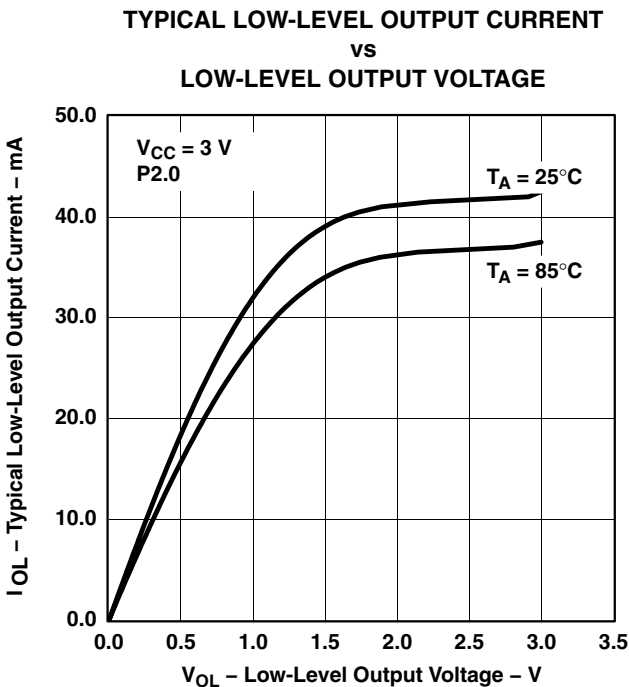


Figure 3

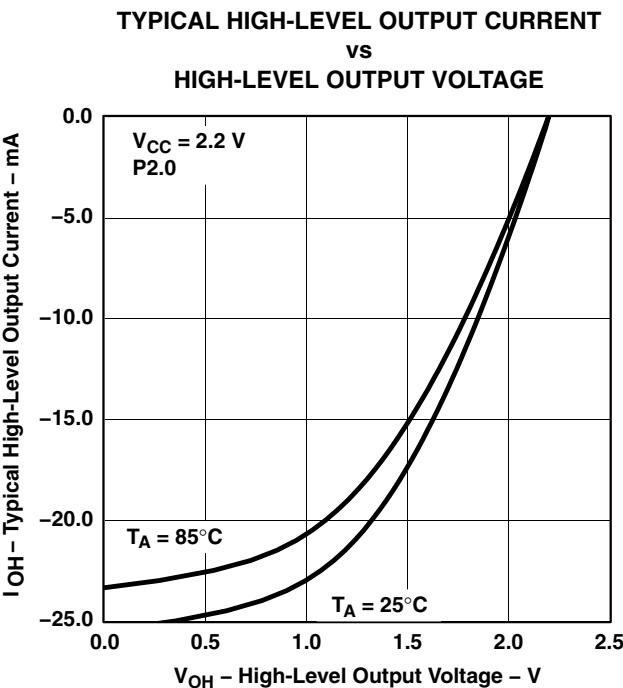


Figure 4

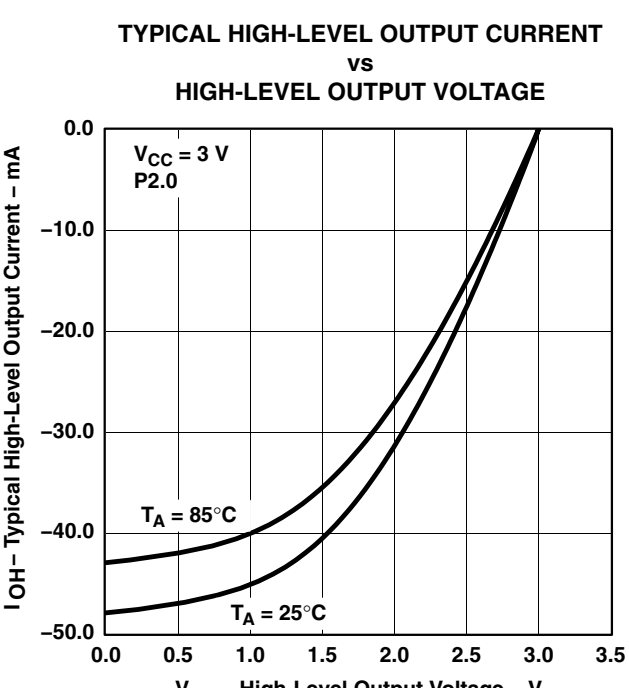


Figure 5

**electrical characteristics over recommended operating free-air temperature (unless otherwise noted)**

**wake-up LPM3**

| PARAMETER                       | TEST CONDITIONS | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|---------------------------------|-----------------|-----------------|-----|-----|-----|------|
| t <sub>d(LPM3)</sub> Delay time | f = 1 MHz       | 2.2 V/3 V       |     |     | 6   | μs   |
|                                 | f = 2 MHz       |                 |     |     | 6   |      |
|                                 | f = 3 MHz       |                 |     |     | 6   |      |

**RAM**

| PARAMETER | TEST CONDITIONS         | MIN | TYP | MAX | UNIT |
|-----------|-------------------------|-----|-----|-----|------|
| VRAMh     | CPU halted (see Note 1) | 1.6 |     |     | V    |

NOTE 1: This parameter defines the minimum supply voltage when the data in program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

# MSP430x461x1, MSP430x461x MIXED SIGNAL MICROCONTROLLER

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

## LCD\_A

| PARAMETER            |                                             | TEST CONDITIONS                                                                                                                                                     | V <sub>CC</sub> | MIN | TYP             | MAX  | UNIT |
|----------------------|---------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-----|-----------------|------|------|
| V <sub>CC(LCD)</sub> | Supply voltage (see Note 2)                 | Charge pump enabled (LCDPEN = 1; VLCDx > 0000)                                                                                                                      |                 | 2.2 |                 | 3.6  | V    |
| I <sub>CC(LCD)</sub> | Supply current (see Note 2)                 | V <sub>LCD(typ)</sub> =3 V; LCDPEN = 1, VLCDx= 1000; all segments on, f <sub>LCD</sub> = f <sub>ACLK</sub> /32, no LCD connected (see Note 4) T <sub>A</sub> = 25°C | 2.2 V           |     | 3               |      | μA   |
| C <sub>LCD</sub>     | Capacitor on LCDCAP (see Note 1 and Note 3) | Charge pump enabled (LCDPEN = 1; VLCDx > 0000)                                                                                                                      |                 | 4.7 |                 |      | μF   |
| f <sub>LCD</sub>     | LCD frequency                               |                                                                                                                                                                     |                 |     |                 | 1.1  | kHz  |
| V <sub>LCD</sub>     | LCD voltage (see Note 3)                    | VLCDx = 0000                                                                                                                                                        |                 |     | V <sub>CC</sub> |      | V    |
|                      |                                             | VLCDx = 0001                                                                                                                                                        |                 |     | 2.60            |      |      |
|                      |                                             | VLCDx = 0010                                                                                                                                                        |                 |     | 2.66            |      |      |
|                      |                                             | VLCDx = 0011                                                                                                                                                        |                 |     | 2.72            |      |      |
|                      |                                             | VLCDx = 0100                                                                                                                                                        |                 |     | 2.78            |      |      |
|                      |                                             | VLCDx = 0101                                                                                                                                                        |                 |     | 2.84            |      |      |
|                      |                                             | VLCDx = 0110                                                                                                                                                        |                 |     | 2.90            |      |      |
|                      |                                             | VLCDx = 0111                                                                                                                                                        |                 |     | 2.96            |      |      |
|                      |                                             | VLCDx = 1000                                                                                                                                                        |                 |     | 3.02            |      |      |
|                      |                                             | VLCDx = 1001                                                                                                                                                        |                 |     | 3.08            |      |      |
|                      |                                             | VLCDx = 1010                                                                                                                                                        |                 |     | 3.14            |      |      |
|                      |                                             | VLCDx = 1011                                                                                                                                                        |                 |     | 3.20            |      |      |
|                      |                                             | VLCDx = 1100                                                                                                                                                        |                 |     | 3.26            |      |      |
|                      |                                             | VLCDx = 1101                                                                                                                                                        |                 |     | 3.32            |      |      |
|                      |                                             | VLCDx = 1110                                                                                                                                                        |                 |     | 3.38            |      |      |
|                      |                                             | VLCDx = 1111                                                                                                                                                        |                 |     | 3.44            | 3.60 |      |
| R <sub>LCD</sub>     | LCD driver output impedance                 | V <sub>LCD</sub> =3 V; CPEN = 1; VLCDx = 1000, I <sub>LOAD</sub> = ± 10 μA                                                                                          | 2.2 V           |     |                 | 10   | kΩ   |

- NOTES: 1. Enabling the internal charge pump with an external capacitor smaller than the minimum specified might damage the device.  
2. Refer to the supply current specifications I<sub>(LPM3)</sub> for additional current specifications with the LCD\_A module active.  
3. Segments S0 through S3 are disabled when the LCD charge pump feature is enabled (LCDPEN = 1) and cannot be used together with the LCD charge pump. In addition, when using segments S0 through S3 with an external LCD voltage supply, V<sub>LCD</sub> ≤ AV<sub>CC</sub>.  
4. Connecting an actual display will increase the current consumption depending on the size of the LCD.

**electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)**

**Comparator\_A (see Note 1)**

| PARAMETER                         |                                                 | TEST CONDITIONS                                                                             | MIN                                  | TYP  | MAX        | UNIT          |
|-----------------------------------|-------------------------------------------------|---------------------------------------------------------------------------------------------|--------------------------------------|------|------------|---------------|
| $I_{(CC)}$                        |                                                 | CAON=1, CARSEL=0, CAREF=0                                                                   | $V_{CC} = 2.2\text{ V}$              | 25   | 40         | $\mu\text{A}$ |
|                                   |                                                 |                                                                                             | $V_{CC} = 3\text{ V}$                | 45   | 60         |               |
| $I_{(\text{Refladder/RefDiode})}$ |                                                 | CAON=1, CARSEL=0, CAREF=1/2/3,<br>No load at P1.6/CA0 and<br>P1.7/CA1                       | $V_{CC} = 2.2\text{ V}$              | 30   | 50         | $\mu\text{A}$ |
|                                   |                                                 |                                                                                             | $V_{CC} = 3\text{ V}$                | 45   | 71         |               |
| $V_{(\text{Ref025})}$             | Voltage @ $0.25\text{ V}_{CC}$ node<br>$V_{CC}$ | PCA0=1, CARSEL=1, CAREF=1,<br>No load at P1.6/CA0 and P1.7/CA1                              | $V_{CC} = 2.2\text{ V} / 3\text{ V}$ | 0.23 | 0.24       | 0.25          |
| $V_{(\text{Ref050})}$             | Voltage @ $0.5\text{ V}_{CC}$ node<br>$V_{CC}$  | PCA0=1, CARSEL=1, CAREF=2,<br>No load at P1.6/CA0 and P1.7/CA1                              | $V_{CC} = 2.2\text{ V} / 3\text{ V}$ | 0.47 | 0.48       | 0.5           |
| $V_{(\text{RefVT})}$              |                                                 | PCA0=1, CARSEL=1, CAREF=3,<br>No load at P1.6/CA0 and P1.7/CA1;<br>$T_A = 85^\circ\text{C}$ | $V_{CC} = 2.2\text{ V}$              | 390  | 480        | 540           |
|                                   |                                                 |                                                                                             | $V_{CC} = 3\text{ V}$                | 400  | 490        | 550           |
| $V_{IC}$                          | Common-mode input<br>voltage range              | CAON=1                                                                                      | $V_{CC} = 2.2\text{ V} / 3\text{ V}$ | 0    | $V_{CC}-1$ | V             |
| $V_P-V_S$                         | Offset voltage                                  | See Note 2                                                                                  | $V_{CC} = 2.2\text{ V} / 3\text{ V}$ | -30  | 30         | mV            |
| $V_{hys}$                         | Input hysteresis                                | CAON = 1                                                                                    | $V_{CC} = 2.2\text{ V} / 3\text{ V}$ | 0    | 0.7        | 1.4           |
| $t_{(\text{response LH})}$        |                                                 | $T_A = 25^\circ\text{C}$ ,<br>Overdrive 10 mV, without filter: CAF = 0                      | $V_{CC} = 2.2\text{ V}$              | 160  | 210        | 300           |
|                                   |                                                 |                                                                                             | $V_{CC} = 3\text{ V}$                | 80   | 150        | 240           |
|                                   |                                                 | $T_A = 25^\circ\text{C}$<br>Overdrive 10 mV, with filter: CAF = 1                           | $V_{CC} = 2.2\text{ V}$              | 1.4  | 1.9        | 3.4           |
|                                   |                                                 |                                                                                             | $V_{CC} = 3\text{ V}$                | 0.9  | 1.5        | 2.6           |
| $t_{(\text{response HL})}$        |                                                 | $T_A = 25^\circ\text{C}$<br>Overdrive 10 mV, without filter: CAF = 0                        | $V_{CC} = 2.2\text{ V}$              | 130  | 210        | 300           |
|                                   |                                                 |                                                                                             | $V_{CC} = 3\text{ V}$                | 80   | 150        | 240           |
|                                   |                                                 | $T_A = 25^\circ\text{C}$ ,<br>Overdrive 10 mV, with filter: CAF = 1                         | $V_{CC} = 2.2\text{ V}$              | 1.4  | 1.9        | 3.4           |
|                                   |                                                 |                                                                                             | $V_{CC} = 3\text{ V}$                | 0.9  | 1.5        | 2.6           |

- NOTES: 1. The leakage current for the Comparator\_A terminals is identical to  $I_{(kg(Px.x))}$  specification.  
2. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator\_A inputs on successive measurements. The two successive measurements are then summed together.

typical characteristics

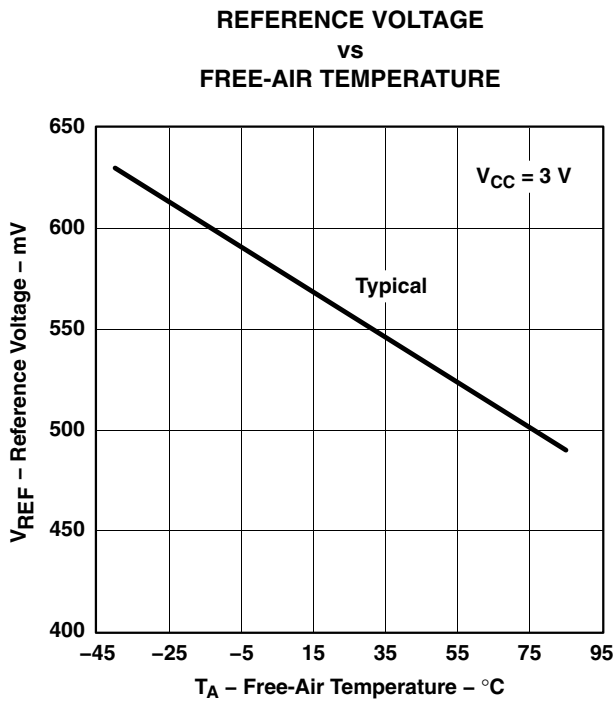


Figure 6.  $V_{(RefVT)}$  vs Temperature

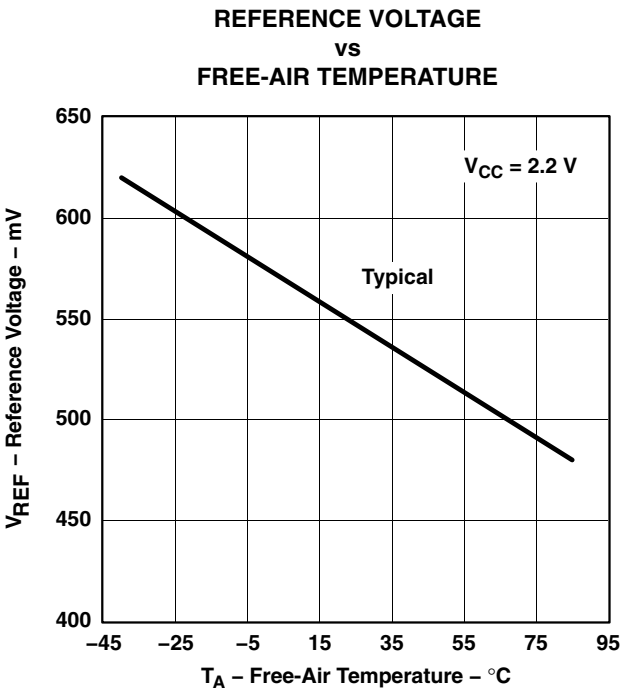


Figure 7.  $V_{(RefVT)}$  vs Temperature

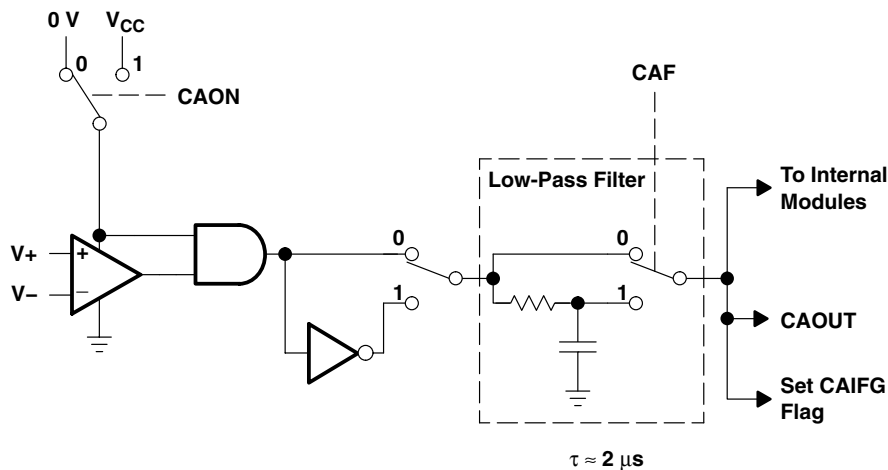


Figure 8. Block Diagram of Comparator\_A Module

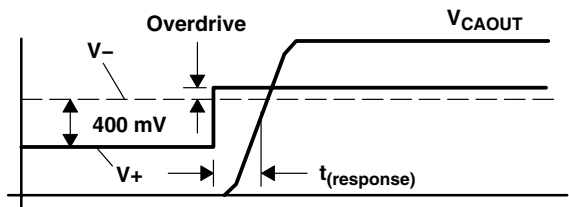


Figure 9. Overdrive Definition

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

POR/brownout reset (BOR) (see Note 1)

| PARAMETER         | TEST CONDITIONS                                                                                                    | MIN | TYP                       | MAX  | UNIT    |
|-------------------|--------------------------------------------------------------------------------------------------------------------|-----|---------------------------|------|---------|
| $t_{d(BOR)}$      |                                                                                                                    |     |                           | 2000 | $\mu s$ |
| $V_{CC(start)}$   | $dV_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 10)                                                                    |     | $0.7 \times V_{(B\_IT-)}$ |      | V       |
| $V_{(B\_IT-)}$    | $dV_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 10 through Figure 12)                                                  |     |                           | 1.79 | V       |
| $V_{hys(B\_IT-)}$ | $dV_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 10)                                                                    | 70  | 130                       | 210  | mV      |
| $t_{(reset)}$     | Pulse length needed at $\overline{RST}/NMI$ pin to accepted reset internally, $V_{CC} = 2.2 \text{ V}/3 \text{ V}$ | 2   |                           |      | $\mu s$ |

- NOTES: 1. The current consumption of the brownout module is already included in the  $I_{CC}$  current consumption data.  
2. The voltage level  $V_{(B\_IT-)} + V_{hys(B\_IT-)}$  is  $\leq 1.89 \text{ V}$ .  
3. During power up, the CPU begins code execution following a period of  $t_{d(BOR)}$  after  $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$ . The default FLL+ settings must not be changed until  $V_{CC} \geq V_{CC(min)}$ , where  $V_{CC(min)}$  is the minimum supply voltage for the desired operating frequency. See the *MSP430x4xx Family User's Guide* for more information on the brownout/SVS circuit.

### typical characteristics

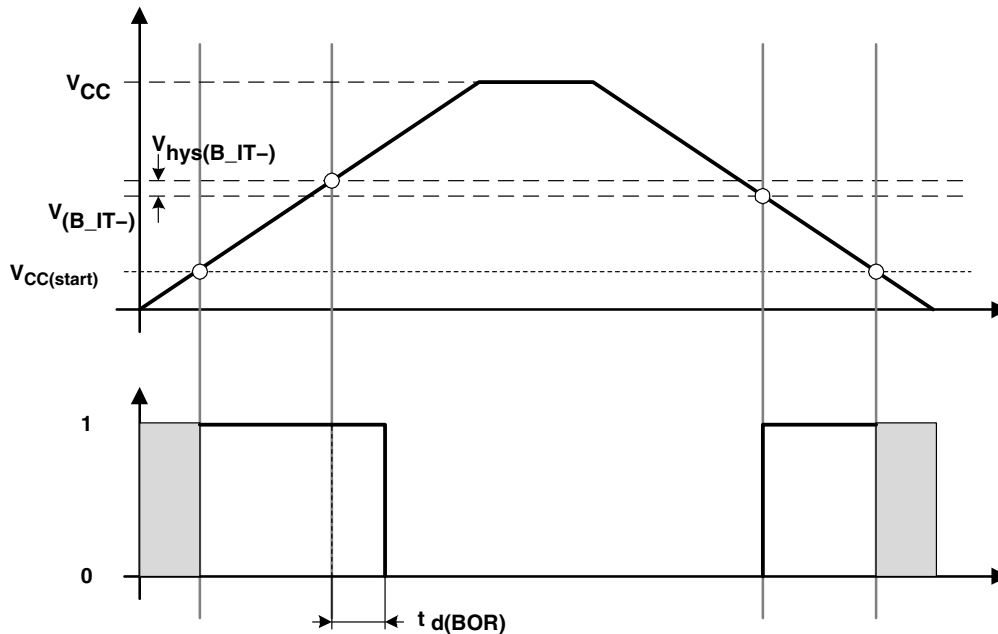


Figure 10. POR/Brownout Reset (BOR) vs Supply Voltage

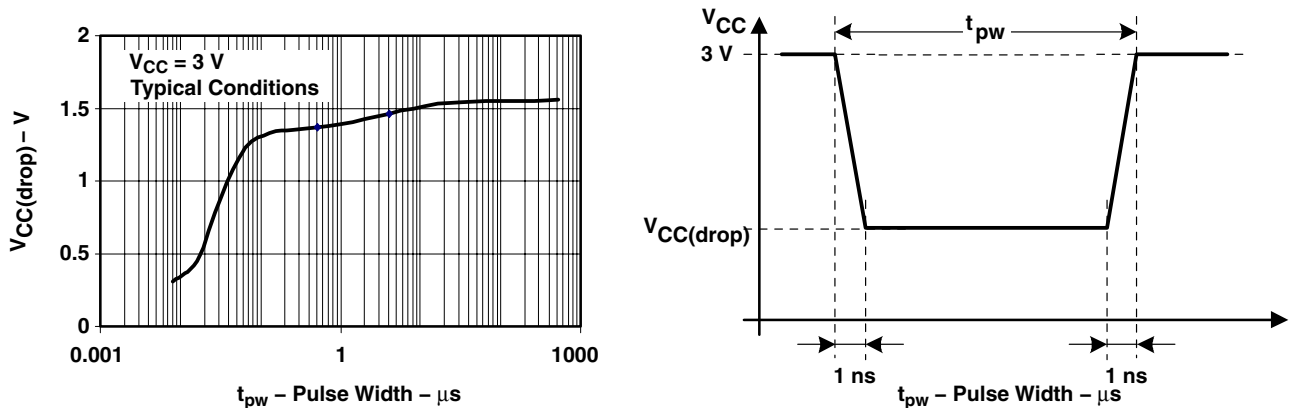


Figure 11.  $V_{CC(drop)}$  Level With a Square Voltage Drop to Generate a POR/Brownout Signal

**typical characteristics (continued)**

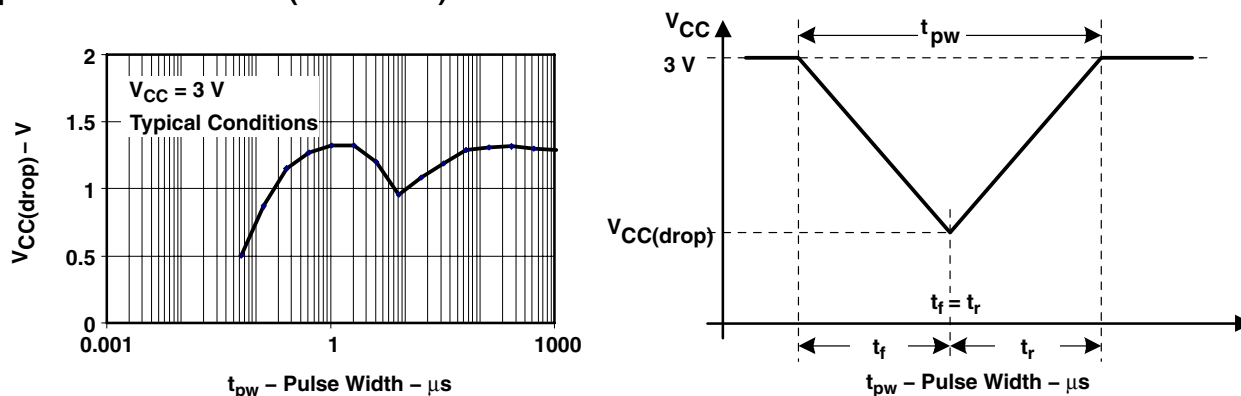


**Figure 12.  $V_{CC(drop)}$  Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal**

**electrical characteristics over recommended operating free-air temperature (unless otherwise noted)**

**supply voltage supervisor/monitor (SVS) (see Note 1)**

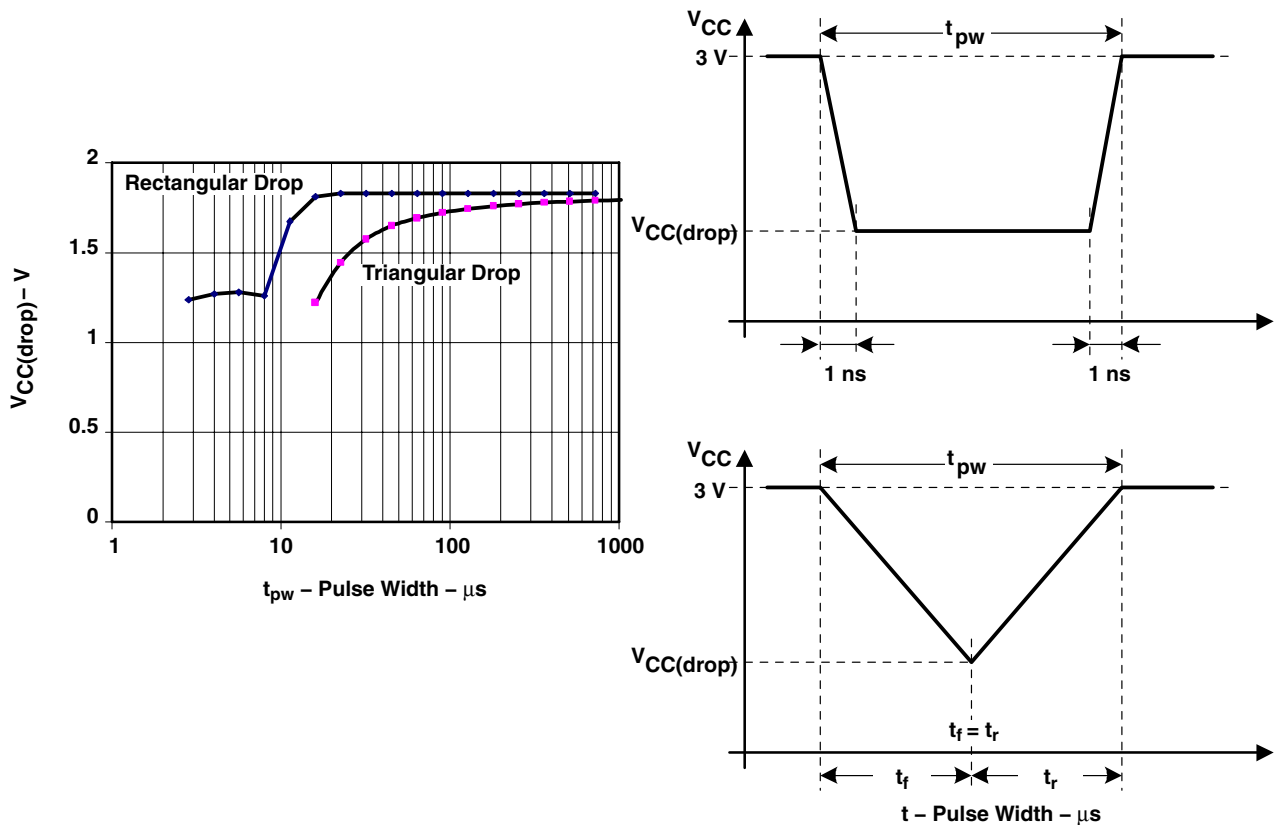
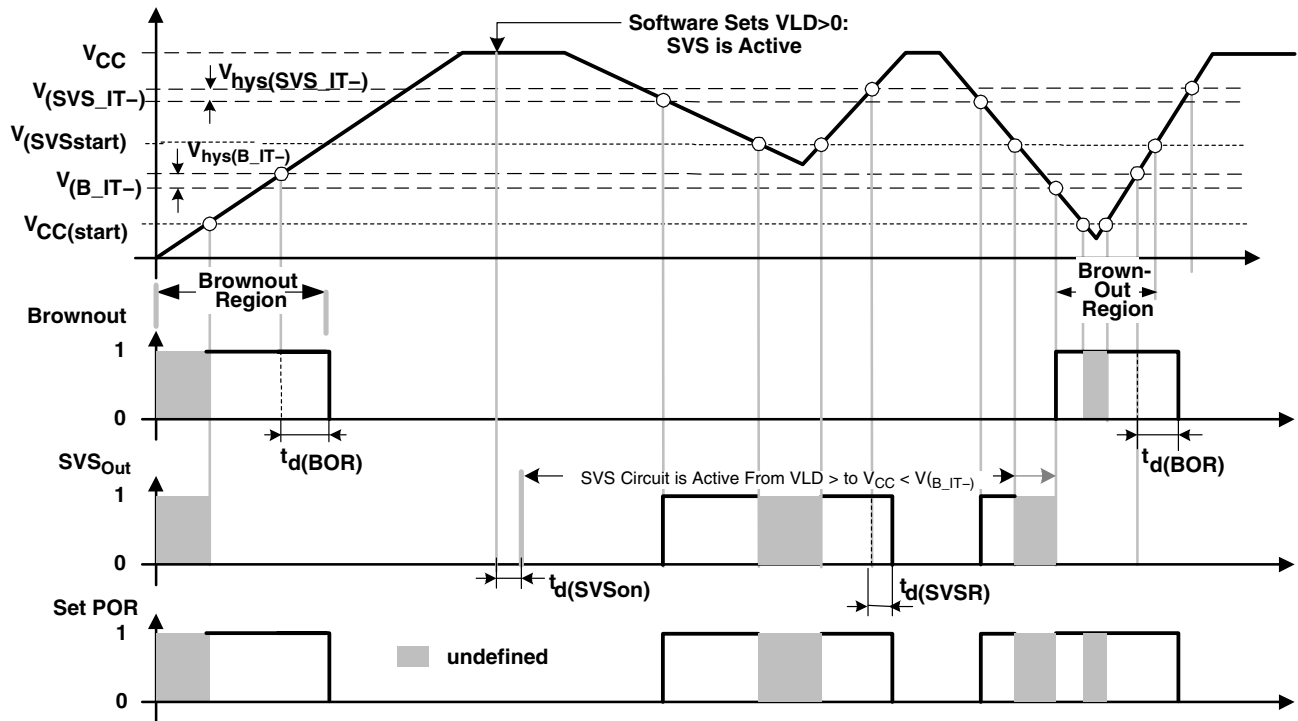
| PARAMETER                             | TEST CONDITIONS                                                             |               | MIN                               | TYP  | MAX                               | UNIT |
|---------------------------------------|-----------------------------------------------------------------------------|---------------|-----------------------------------|------|-----------------------------------|------|
| t <sub>(SVSR)</sub>                   | dV <sub>CC</sub> /dt > 30 V/ms (see Figure 13)                              |               | 5                                 |      | 150                               | μs   |
|                                       | dV <sub>CC</sub> /dt ≤ 30 V/ms                                              |               |                                   |      | 2000                              |      |
| t <sub>d</sub> (SVSon)                | SVS on, switch from VLD = 0 to VLD ≠ 0, V <sub>CC</sub> = 3 V               |               | 20                                |      | 150                               | μs   |
| t <sub>settle</sub>                   | VLD ≠ 0†                                                                    |               |                                   |      | 12                                | μs   |
| V <sub>(SVSstart)</sub>               | VLD ≠ 0, V <sub>CC</sub> /dt ≤ 3 V/s (see Figure 13)                        |               |                                   | 1.55 | 1.7                               | V    |
| V <sub>hys</sub> (SVS_IT–)            | V <sub>CC</sub> /dt ≤ 3 V/s (see Figure 13)                                 | VLD = 1       | 70                                | 120  | 155                               | mV   |
|                                       |                                                                             | VLD = 2 .. 14 | V <sub>(SVS_IT–)</sub><br>x 0.001 |      | V <sub>(SVS_IT–)</sub><br>x 0.016 |      |
|                                       | V <sub>CC</sub> /dt ≤ 3 V/s (see Figure 13), external voltage applied on A7 | VLD = 15      | 4.4                               |      | 20                                | mV   |
| V <sub>(SVS_IT–)</sub>                | V <sub>CC</sub> /dt ≤ 3 V/s (see Figure 13)                                 | VLD = 1       | 1.8                               | 1.9  | 2.05                              | V    |
|                                       |                                                                             | VLD = 2       | 1.94                              | 2.1  | 2.23                              |      |
|                                       |                                                                             | VLD = 3       | 2.05                              | 2.2  | 2.35                              |      |
|                                       |                                                                             | VLD = 4       | 2.14                              | 2.3  | 2.46                              |      |
|                                       |                                                                             | VLD = 5       | 2.24                              | 2.4  | 2.58                              |      |
|                                       |                                                                             | VLD = 6       | 2.33                              | 2.5  | 2.69                              |      |
|                                       |                                                                             | VLD = 7       | 2.46                              | 2.65 | 2.84                              |      |
|                                       |                                                                             | VLD = 8       | 2.58                              | 2.8  | 2.97                              |      |
|                                       |                                                                             | VLD = 9       | 2.69                              | 2.9  | 3.10                              |      |
|                                       |                                                                             | VLD = 10      | 2.83                              | 3.05 | 3.26                              |      |
|                                       |                                                                             | VLD = 11      | 2.94                              | 3.2  | 3.39                              |      |
|                                       |                                                                             | VLD = 12      | 3.11                              | 3.35 | 3.58†                             |      |
|                                       |                                                                             | VLD = 13      | 3.24                              | 3.5  | 3.73†                             |      |
|                                       |                                                                             | VLD = 14      | 3.43                              | 3.7† | 3.96†                             |      |
|                                       | V <sub>CC</sub> /dt ≤ 3 V/s (see Figure 13), external voltage applied on A7 | VLD = 15      | 1.1                               | 1.2  | 1.3                               |      |
| I <sub>CC</sub> (SVS)<br>(see Note 4) | VLD ≠ 0, V <sub>CC</sub> = 2.2 V/3 V                                        |               |                                   | 10   | 15                                | μA   |

<sup>†</sup> The recommended operating voltage range is limited to 3.6 V.

<sup>‡</sup>  $t_{settle}$  is the settling time that the comparator o/p needs to have a stable level after  $VLD \neq 0$  to a different  $VLD$  value somewhere between 2 and 15. The overdrive is assumed to be  $> 50 \text{ mV}$ .

NOTE 4: The current consumption of the SVS module is not included in the  $I_{CC}$  current consumption data.

typical characteristics



# MSP430x461x1, MSP430x461x MIXED SIGNAL MICROCONTROLLER

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

## DCO

| PARAMETER             | TEST CONDITIONS                                                                                                                                | V <sub>CC</sub> | MIN  | TYP  | MAX  | UNIT              |
|-----------------------|------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|------|------|------|-------------------|
| f <sub>(DCOCLK)</sub> | N <sub>(DCO)</sub> =01Eh, FN_8=FN_4=FN_3=FN_2=0, D = 2; DCOPLUS= 0                                                                             | 2.2 V/3 V       |      | 1    |      | MHz               |
| f <sub>(DCO=2)</sub>  | FN_8=FN_4=FN_3=FN_2=0 ; DCOPLUS = 1                                                                                                            | 2.2 V           | 0.3  | 0.65 | 1.25 | MHz               |
|                       |                                                                                                                                                | 3 V             | 0.3  | 0.7  | 1.3  |                   |
| f <sub>(DCO=27)</sub> | FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1                                                                                                             | 2.2 V           | 2.5  | 5.6  | 10.5 | MHz               |
|                       |                                                                                                                                                | 3 V             | 2.7  | 6.1  | 11.3 |                   |
| f <sub>(DCO=2)</sub>  | FN_8=FN_4=FN_3=0, FN_2=1; DCOPLUS = 1                                                                                                          | 2.2 V           | 0.7  | 1.3  | 2.3  | MHz               |
|                       |                                                                                                                                                | 3 V             | 0.8  | 1.5  | 2.5  |                   |
| f <sub>(DCO=27)</sub> | FN_8=FN_4=FN_3=0, FN_2=1; DCOPLUS = 1                                                                                                          | 2.2 V           | 5.7  | 10.8 | 18   | MHz               |
|                       |                                                                                                                                                | 3 V             | 6.5  | 12.1 | 20   |                   |
| f <sub>(DCO=2)</sub>  | FN_8=FN_4=0, FN_3= 1, FN_2=x; DCOPLUS = 1                                                                                                      | 2.2 V           | 1.2  | 2    | 3    | MHz               |
|                       |                                                                                                                                                | 3 V             | 1.3  | 2.2  | 3.5  |                   |
| f <sub>(DCO=27)</sub> | FN_8=FN_4=0, FN_3= 1, FN_2=x; DCOPLUS = 1                                                                                                      | 2.2 V           | 9    | 15.5 | 25   | MHz               |
|                       |                                                                                                                                                | 3 V             | 10.3 | 17.9 | 28.5 |                   |
| f <sub>(DCO=2)</sub>  | FN_8=0, FN_4= 1, FN_3= FN_2=x; DCOPLUS = 1                                                                                                     | 2.2 V           | 1.8  | 2.8  | 4.2  | MHz               |
|                       |                                                                                                                                                | 3 V             | 2.1  | 3.4  | 5.2  |                   |
| f <sub>(DCO=27)</sub> | FN_8=0, FN_4=1, FN_3= FN_2=x; DCOPLUS = 1                                                                                                      | 2.2 V           | 13.5 | 21.5 | 33   | MHz               |
|                       |                                                                                                                                                | 3 V             | 16   | 26.6 | 41   |                   |
| f <sub>(DCO=2)</sub>  | FN_8=1, FN_4=FN_3=FN_2=x; DCOPLUS = 1                                                                                                          | 2.2 V           | 2.8  | 4.2  | 6.2  | MHz               |
|                       |                                                                                                                                                | 3 V             | 4.2  | 6.3  | 9.2  |                   |
| f <sub>(DCO=27)</sub> | FN_8=1, FN_4=FN_3=FN_2=x; DCOPLUS = 1                                                                                                          | 2.2 V           | 21   | 32   | 46   | MHz               |
|                       |                                                                                                                                                | 3 V             | 30   | 46   | 70   |                   |
| S <sub>n</sub>        | Step size between adjacent DCO taps:<br>S <sub>n</sub> = f <sub>DCO(Tap n+1)</sub> / f <sub>DCO(Tap n)</sub> (see Figure 16 for taps 21 to 27) | 1 < TAP ≤ 20    | 1.06 |      | 1.11 |                   |
|                       |                                                                                                                                                | TAP = 27        | 1.07 |      | 1.17 |                   |
| D <sub>t</sub>        | Temperature drift, N <sub>(DCO)</sub> = 01Eh, FN_8=FN_4=FN_3=FN_2=0<br>D = 2; DCOPLUS = 0                                                      | 2.2 V           | -0.2 | -0.3 | -0.4 | %/ <sup>o</sup> C |
|                       |                                                                                                                                                | 3 V             | -0.2 | -0.3 | -0.4 |                   |
| D <sub>V</sub>        | Drift with V <sub>CC</sub> variation, N <sub>(DCO)</sub> = 01Eh, FN_8=FN_4=FN_3=FN_2=0<br>D = 2; DCOPLUS = 0                                   |                 | 0    | 5    | 15   | %/V               |

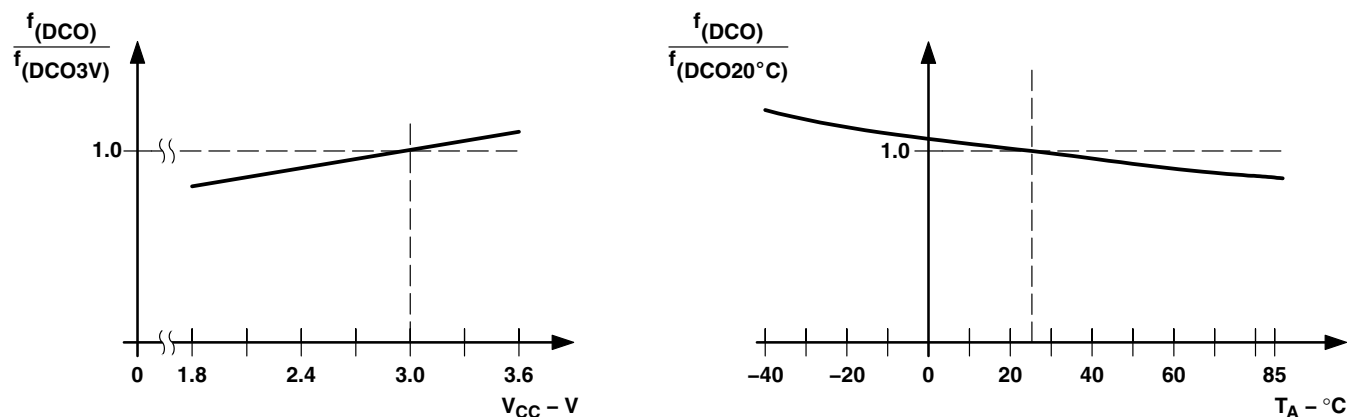


Figure 15. DCO Frequency vs Supply Voltage V<sub>CC</sub> and vs Ambient Temperature

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

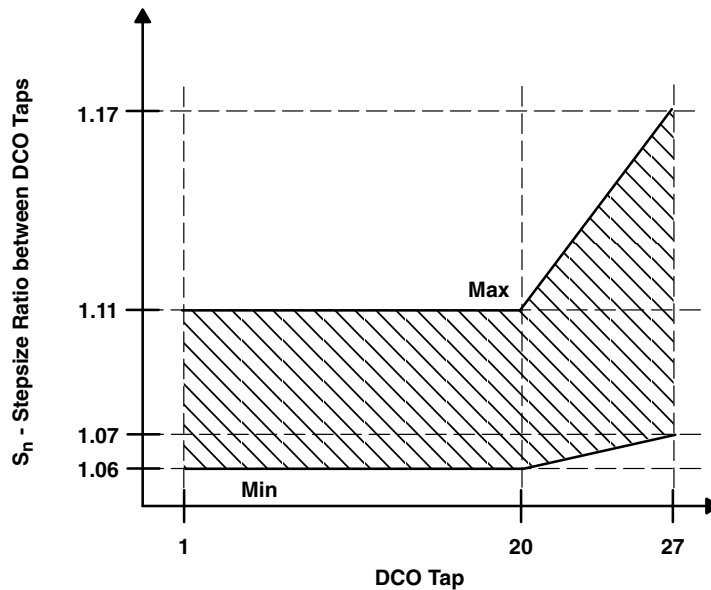


Figure 16. DCO Tap Step Size

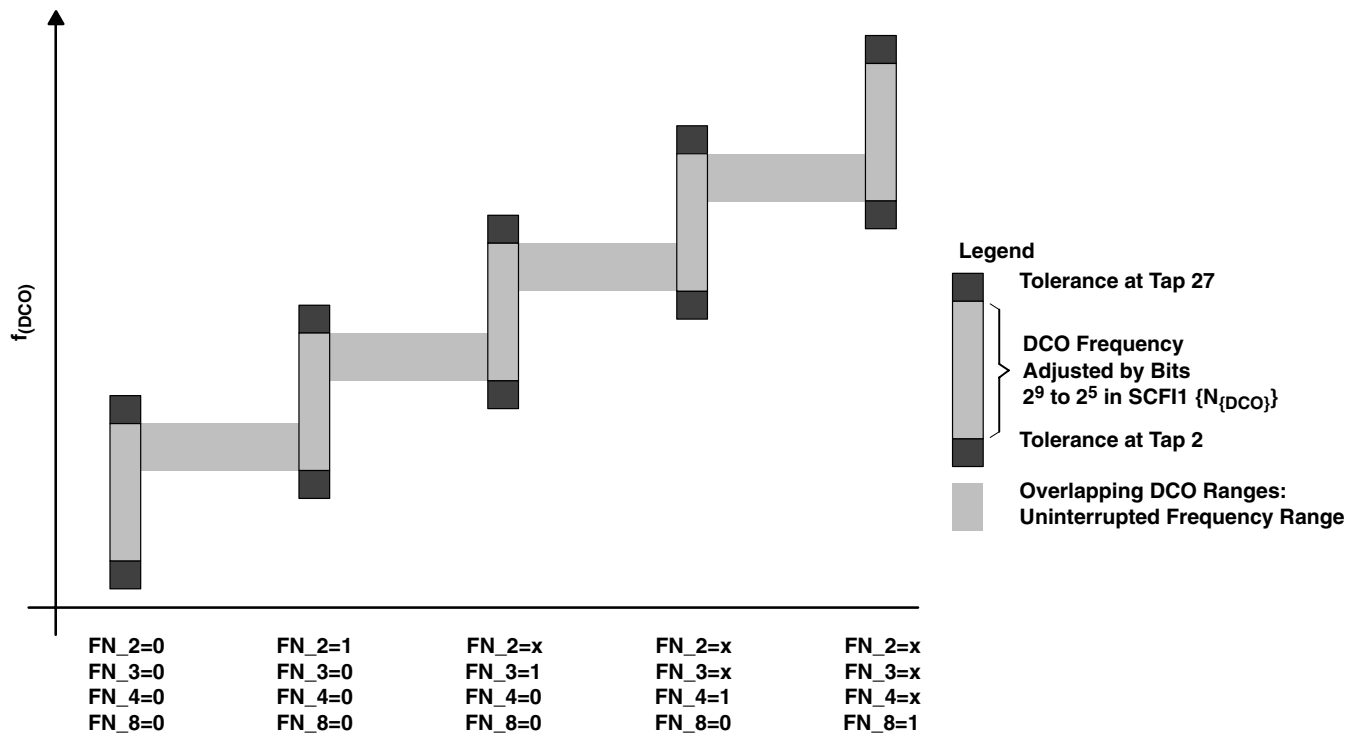


Figure 17. Five Overlapping DCO Ranges Controlled by FN\_x Bits

# MSP430x461x1, MSP430x461x MIXED SIGNAL MICROCONTROLLER

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

crystal oscillator, LFXT1 oscillator (see Notes 1 and 2)

| PARAMETER         |                                            | TEST CONDITIONS | V <sub>CC</sub> | MIN                 | TYP | MAX                 | UNIT |
|-------------------|--------------------------------------------|-----------------|-----------------|---------------------|-----|---------------------|------|
| C <sub>XIN</sub>  | Integrated input capacitance (see Note 4)  | OSCCAPx = 0h    | 2.2 V / 3 V     |                     | 0   |                     | pF   |
|                   |                                            | OSCCAPx = 1h    | 2.2 V / 3 V     |                     | 10  |                     |      |
|                   |                                            | OSCCAPx = 2h    | 2.2 V / 3 V     |                     | 14  |                     |      |
|                   |                                            | OSCCAPx = 3h    | 2.2 V / 3 V     |                     | 18  |                     |      |
| C <sub>XOUT</sub> | Integrated output capacitance (see Note 4) | OSCCAPx = 0h    | 2.2 V / 3 V     |                     | 0   |                     | pF   |
|                   |                                            | OSCCAPx = 1h    | 2.2 V / 3 V     |                     | 10  |                     |      |
|                   |                                            | OSCCAPx = 2h    | 2.2 V / 3 V     |                     | 14  |                     |      |
|                   |                                            | OSCCAPx = 3h    | 2.2 V / 3 V     |                     | 18  |                     |      |
| V <sub>IL</sub>   | Input levels at XIN                        | See Note 3      | 2.2 V/3 V       | V <sub>SS</sub>     |     | 0.2×V <sub>CC</sub> | V    |
| V <sub>IH</sub>   |                                            |                 |                 | 0.8×V <sub>CC</sub> |     | V <sub>CC</sub>     |      |

- NOTES: 1. The parasitic capacitance from the package and board may be estimated to be 2 pF. The effective load capacitor for the crystal is  $(C_{XIN} \times C_{XOUT}) / (C_{XIN} + C_{XOUT})$ . This is independent of XTS\_FLL.
2. To improve EMI on the low-power LFXT1 oscillator, particularly in the LF mode (32 kHz), the following guidelines should be observed.
- Keep the trace between the MSP430 device and the crystal as short as possible.
  - Design a good ground plane around the oscillator pins.
  - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
  - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
  - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
  - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
  - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
3. Applies only when using an external logic-level clock source. XTS\_FLL must be set. Not applicable when using a crystal or resonator.
4. External capacitance is recommended for precision real-time clock applications; OSCCAPx = 0h.

crystal oscillator, XT2 oscillator (see Note 1)

| PARAMETER           |                               | TEST CONDITIONS                          | MIN                   | TYP | MAX                   | UNIT |
|---------------------|-------------------------------|------------------------------------------|-----------------------|-----|-----------------------|------|
| C <sub>XT2IN</sub>  | Integrated input capacitance  | V <sub>CC</sub> = 2.2 V/3 V              |                       | 2   |                       | pF   |
| C <sub>XT2OUT</sub> | Integrated output capacitance | V <sub>CC</sub> = 2.2 V/3 V              |                       | 2   |                       | pF   |
| V <sub>IL</sub>     | Input levels at XT2IN         | V <sub>CC</sub> = 2.2 V/3 V (see Note 2) | V <sub>SS</sub>       |     | 0.2 × V <sub>CC</sub> | V    |
| V <sub>IH</sub>     |                               |                                          | 0.8 × V <sub>CC</sub> |     | V <sub>CC</sub>       | V    |

- NOTES: 1. The oscillator needs capacitors at both terminals, with values specified by the crystal manufacturer.
2. Applies only when using an external logic-level clock source. Not applicable when using a crystal or resonator.

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

**USCI (UART mode)**

| PARAMETER                                                             | TEST CONDITIONS                                                   | V <sub>CC</sub> | MIN | TYP                 | MAX | UNIT |
|-----------------------------------------------------------------------|-------------------------------------------------------------------|-----------------|-----|---------------------|-----|------|
| f <sub>USCI</sub> USCI input clock frequency                          | Internal: SMCLK, ACLK<br>External: UCLK<br>Duty Cycle = 50% ± 10% |                 |     | f <sub>SYSTEM</sub> |     | MHz  |
| f <sub>BITCLK</sub> BITCLK clock frequency (equals Baudrate in MBaud) |                                                                   | 2.2V / 3 V      |     |                     | 1   | MHz  |
| t <sub>τ</sub> UART receive deglitch time (see Note 1)                |                                                                   | 2.2 V           | 50  | 150                 | 600 | ns   |
|                                                                       |                                                                   | 3 V             | 50  | 100                 | 600 |      |

NOTE 1: Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized their width should exceed the maximum specification of the deglitch time.

**USCI (SPI master mode) (see Figure 18 and Figure 19)**

| PARAMETER                                         | TEST CONDITIONS                                    | V <sub>CC</sub> | MIN | TYP                 | MAX | UNIT |
|---------------------------------------------------|----------------------------------------------------|-----------------|-----|---------------------|-----|------|
| f <sub>USCI</sub> USCI input clock frequency      | SMCLK, ACLK<br>Duty Cycle = 50% ± 10%              |                 |     | f <sub>SYSTEM</sub> |     | MHz  |
| t <sub>SU,MI</sub> SOMI input data setup time     |                                                    | 2.2 V           | 110 |                     |     | ns   |
|                                                   |                                                    | 3 V             | 75  |                     |     |      |
| t <sub>HD,MI</sub> SOMI input data hold time      |                                                    | 2.2 V           | 0   |                     |     | ns   |
|                                                   |                                                    | 3 V             | 0   |                     |     |      |
| t <sub>VALID,MO</sub> SIMO output data valid time | UCLK edge to SIMO valid;<br>C <sub>L</sub> = 20 pF | 2.2 V           |     |                     | 30  | ns   |
|                                                   |                                                    | 3 V             |     |                     | 20  |      |

**USCI (SPI slave mode) (see Figure 20 and Figure 21)**

| PARAMETER                                                                | TEST CONDITIONS                                    | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|--------------------------------------------------------------------------|----------------------------------------------------|-----------------|-----|-----|-----|------|
| t <sub>STE,LEAD</sub> STE lead time<br>STE low to clock                  |                                                    | 2.2 V/3 V       |     | 50  |     | ns   |
| t <sub>STE,LAG</sub> STE lag time<br>Last clock to STE high              |                                                    | 2.2 V/3 V       | 10  |     |     | ns   |
| t <sub>STE,ACC</sub> STE access time<br>STE low to SOMI data out         |                                                    | 2.2 V/3 V       |     | 50  |     | ns   |
| t <sub>STE,DIS</sub> STE disable time<br>STE high to SOMI high impedance |                                                    | 2.2 V/3 V       |     | 50  |     | ns   |
| t <sub>SU,SI</sub> SIMO input data setup time                            |                                                    | 2.2 V           | 20  |     |     | ns   |
|                                                                          |                                                    | 3 V             | 15  |     |     |      |
| t <sub>HD,SI</sub> SIMO input data hold time                             |                                                    | 2.2 V           | 10  |     |     | ns   |
|                                                                          |                                                    | 3 V             | 10  |     |     |      |
| t <sub>VALID,SO</sub> SOMI output data valid time                        | UCLK edge to SOMI valid;<br>C <sub>L</sub> = 20 pF | 2.2 V           |     | 75  | 110 | ns   |
|                                                                          |                                                    | 3 V             |     | 50  | 75  |      |

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

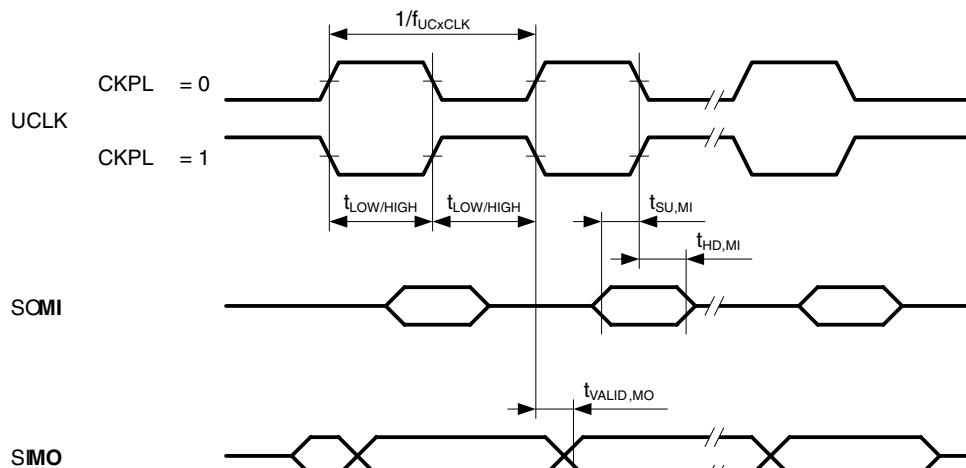


**Figure 18. SPI Master Mode, CKPH = 0**

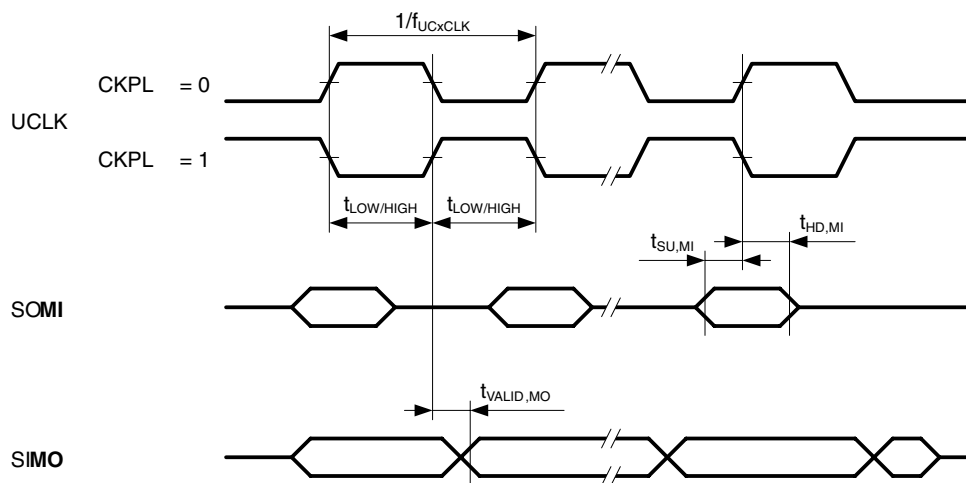


**Figure 19. SPI Master Mode, CKPH = 1**

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

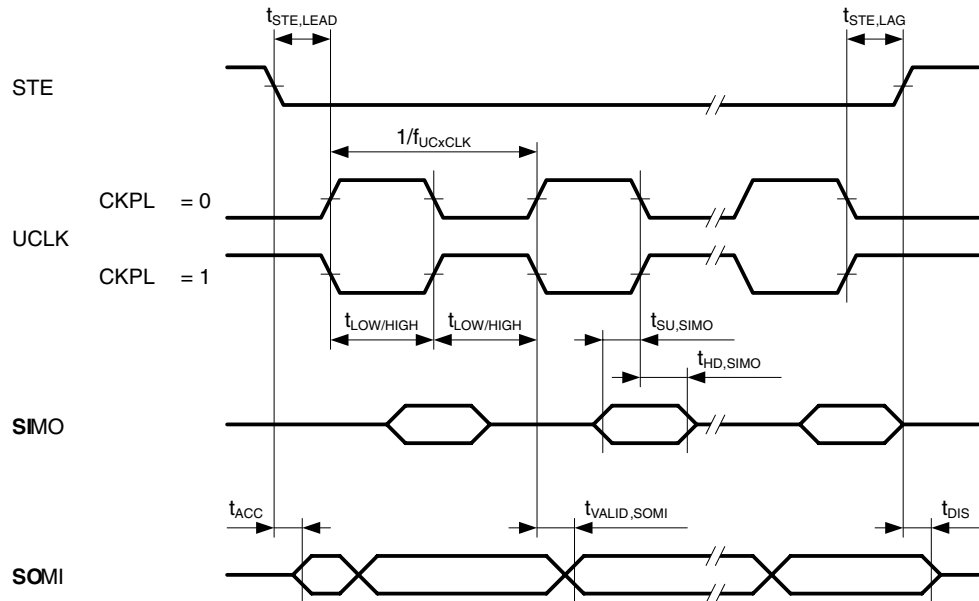


Figure 20. SPI Slave Mode, CKPH = 0

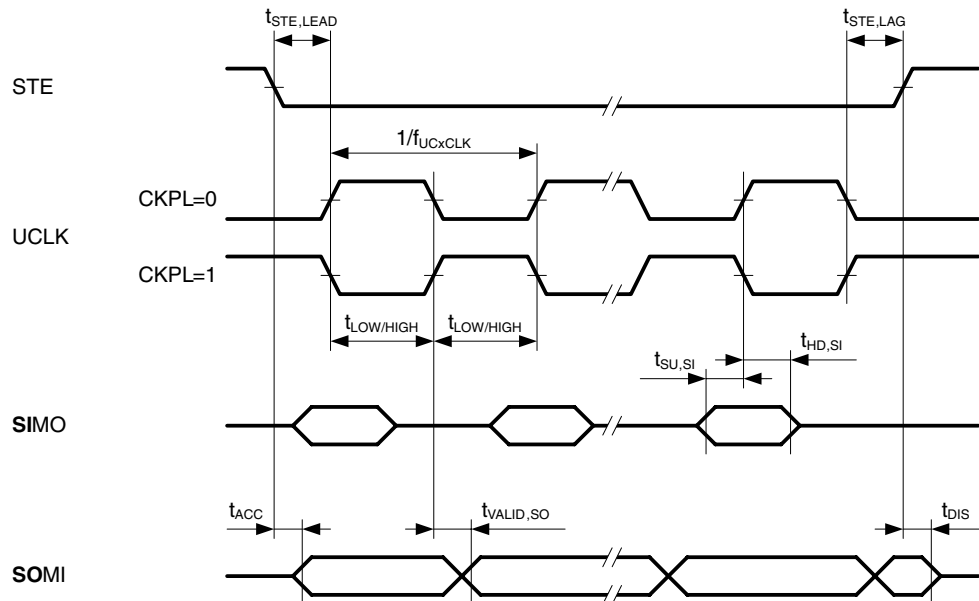


Figure 21. SPI Slave Mode, CKPH = 1

# MSP430x461x1, MSP430x461x MIXED SIGNAL MICROCONTROLLER

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

## USCI (I2C mode) (see Figure 22)

| PARAMETER                                                        | TEST CONDITIONS                                                   | V <sub>CC</sub> | MIN | TYP                 | MAX | UNIT |
|------------------------------------------------------------------|-------------------------------------------------------------------|-----------------|-----|---------------------|-----|------|
| f <sub>USCI</sub> USCI input clock frequency                     | Internal: SMCLK, ACLK<br>External: UCLK<br>Duty Cycle = 50% ± 10% |                 |     | f <sub>SYSTEM</sub> |     | MHz  |
| f <sub>SCL</sub> SCL clock frequency                             |                                                                   | 2.2 V/3 V       | 0   |                     | 400 | kHz  |
| t <sub>HD,STA</sub> Hold time (repeated) START                   | f <sub>SCL</sub> ≤ 100kHz                                         | 2.2 V/3 V       | 4.0 |                     |     | μs   |
|                                                                  | f <sub>SCL</sub> > 100kHz                                         | 2.2 V/3 V       | 0.6 |                     |     |      |
| t <sub>SU,STA</sub> Set-up time for a repeated START             | f <sub>SCL</sub> ≤ 100kHz                                         | 2.2 V/3 V       | 4.7 |                     |     | μs   |
|                                                                  | f <sub>SCL</sub> > 100kHz                                         | 2.2 V/3 V       | 0.6 |                     |     |      |
| t <sub>HD,DAT</sub> Data hold time                               |                                                                   | 2.2 V/3 V       | 0   |                     |     | ns   |
| t <sub>SU,DAT</sub> Data set-up time                             |                                                                   | 2.2 V/3 V       | 250 |                     |     | ns   |
| t <sub>SU,STO</sub> Set-up time for STOP                         |                                                                   | 2.2 V/3 V       | 4.0 |                     |     | μs   |
| t <sub>SP</sub> Pulse width of spikes suppressed by input filter |                                                                   | 2.2 V           | 50  | 150                 | 600 | ns   |
|                                                                  |                                                                   | 3 V             | 50  | 100                 | 600 |      |

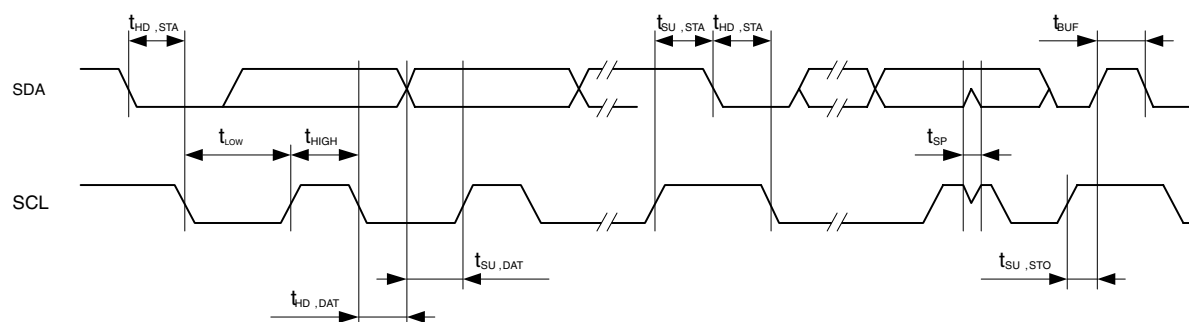


Figure 22. I2C Mode Timing

## USART1 (see Note 1)

| PARAMETER                             | TEST CONDITIONS     | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|---------------------------------------|---------------------|-----------------|-----|-----|-----|------|
| t <sub>(τ)</sub> USART1 deglitch time | SYNC = 0, UART mode | 2.2 V           | 200 | 430 | 800 | ns   |
|                                       | SYNC = 0, UART mode | 3 V             | 150 | 280 | 500 |      |

NOTE 1: The signal applied to the USART1 receive signal/terminal (URXD1) should meet the timing requirements of t<sub>(τ)</sub> to ensure that the URXS flip-flop is set. The URXS flip-flop is set with negative pulses meeting the minimum-timing condition of t<sub>(τ)</sub>. The operating conditions to set the flag must be met independently from this timing constraint. The deglitch circuitry is active only on negative transitions on the URXD1 line.

**electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)**

**12-bit ADC, power supply and input range conditions (see Note 1)**

| PARAMETER                                                                 | TEST CONDITIONS                                                                                                                              | MIN                     | TYP  | MAX        | UNIT     |
|---------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|------|------------|----------|
| $V_{CC}$ Analog supply voltage                                            | $AV_{CC}$ and $DV_{CC}$ are connected together,<br>$AV_{SS}$ and $DV_{SS}$ are connected together,<br>$V_{(AVSS)} = V_{(DVSS)} = 0\text{ V}$ | 2.2                     |      | 3.6        | V        |
| $V_{(P6.x/Ax)}$ Analog input voltage range (see Note 2)                   | All external Ax terminals. Analog inputs selected in ADC12MCTLx register and P6Sel.x=1,<br>$V_{(AVSS)} \leq V_{Ax} \leq V_{(AVCC)}$          | 0                       |      | $V_{AVCC}$ | V        |
| $I_{ADC12}$ Operating supply current into $AV_{CC}$ terminal (see Note 3) | $f_{ADC12CLK} = 5.0\text{ MHz}$ ,<br>$ADC12ON = 1$ , $REFON = 0$ ,<br>$SHT0=0$ , $SHT1=0$ , $ADC12DIV=0$                                     |                         |      |            |          |
|                                                                           | $V_{CC} = 2.2\text{ V}$                                                                                                                      |                         | 0.65 | 1.3        | mA       |
| $I_{REF+}$ Operating supply current into $AV_{CC}$ terminal (see Note 4)  |                                                                                                                                              | $V_{CC} = 3\text{ V}$   | 0.8  | 1.6        |          |
|                                                                           | $f_{ADC12CLK} = 5.0\text{ MHz}$ ,<br>$ADC12ON = 0$ ,<br>$REFON = 1$ , $REF2\_5V = 1$                                                         | $V_{CC} = 3\text{ V}$   | 0.5  | 0.8        | mA       |
|                                                                           | $f_{ADC12CLK} = 5.0\text{ MHz}$ ,<br>$ADC12ON = 0$ ,<br>$REFON = 1$ , $REF2\_5V = 0$                                                         | $V_{CC} = 2.2\text{ V}$ | 0.5  | 0.8        |          |
|                                                                           |                                                                                                                                              | $V_{CC} = 3\text{ V}$   | 0.5  | 0.8        |          |
| $C_I$ Input capacitance                                                   | Only one terminal can be selected at one time, Ax                                                                                            | $V_{CC} = 2.2\text{ V}$ |      | 40         | pF       |
| $R_I$ Input MUX ON resistance                                             | $0V \leq V_{Ax} \leq V_{AVCC}$                                                                                                               | $V_{CC} = 3\text{ V}$   |      | 2000       | $\Omega$ |

- NOTES: 1. The leakage current is defined in the leakage current table with Ax parameter.  
2. The analog input voltage range must be within the selected reference voltage range  $V_{R+}$  to  $V_{R-}$  for valid conversion results.  
3. The internal reference supply current is not included in current consumption parameter  $I_{ADC12}$ .  
4. The internal reference current is supplied via terminal  $AV_{CC}$ . Consumption is independent of the ADC12ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.

**12-bit ADC, external reference (see Note 1)**

| PARAMETER                                                                        | TEST CONDITIONS                               | MIN                                | TYP | MAX        | UNIT          |
|----------------------------------------------------------------------------------|-----------------------------------------------|------------------------------------|-----|------------|---------------|
| $V_{eREF+}$ Positive external reference voltage input                            | $V_{eREF+} > V_{REF-}/V_{eREF-}$ (see Note 2) | 1.4                                |     | $V_{AVCC}$ | V             |
| $V_{REF-}/V_{eREF-}$ Negative external reference voltage input                   | $V_{eREF+} > V_{REF-}/V_{eREF-}$ (see Note 3) | 0                                  |     | 1.2        | V             |
| $(V_{eREF+} - V_{REF-}/V_{eREF-})$ Differential external reference voltage input | $V_{eREF+} > V_{REF-}/V_{eREF-}$ (see Note 4) | 1.4                                |     | $V_{AVCC}$ | V             |
| $I_{VeREF+}$ Input leakage current                                               | $0V \leq V_{eREF+} \leq V_{AVCC}$             | $V_{CC} = 2.2\text{ V}/3\text{ V}$ |     | $\pm 1$    | $\mu\text{A}$ |
| $I_{VREF-}/V_{eREF-}$ Input leakage current                                      | $0V \leq V_{eREF-} \leq V_{AVCC}$             | $V_{CC} = 2.2\text{ V}/3\text{ V}$ |     | $\pm 1$    | $\mu\text{A}$ |

- NOTES: 1. The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance,  $C_I$ , is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.  
2. The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.  
3. The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.  
4. The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

# MSP430x461x1, MSP430x461x MIXED SIGNAL MICROCONTROLLER

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

## 12-bit ADC, built-in reference

| PARAMETER               |                                                                      | TEST CONDITIONS                                                                                                                 | V <sub>CC</sub> | MIN  | TYP | MAX  | UNIT |        |
|-------------------------|----------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------|-----------------|------|-----|------|------|--------|
| V <sub>REF+</sub>       | Positive built-in reference voltage output                           | REF2_5V = 1 for 2.5 V, I <sub>VREF+</sub> max ≤ I <sub>VREF+</sub> ≤ I <sub>VREF+</sub> min                                     | 3 V             | 2.4  | 2.5 | 2.6  | V    |        |
|                         |                                                                      | REF2_5V = 0 for 1.5 V, I <sub>VREF+</sub> max ≤ I <sub>VREF+</sub> ≤ I <sub>VREF+</sub> min                                     | 2.2 V/3 V       | 1.44 | 1.5 | 1.56 |      |        |
| AV <sub>CC(min)</sub>   | AV <sub>CC</sub> minimum voltage, Positive built-in reference active | REF2_5V = 0, I <sub>VREF+</sub> max ≤ I <sub>VREF+</sub> ≤ I <sub>VREF+</sub> min                                               |                 | 2.2  |     |      | V    |        |
|                         |                                                                      | REF2_5V = 1, I <sub>VREF+</sub> min ≥ I <sub>VREF+</sub> ≥ −0.5mA                                                               |                 | 2.8  |     |      |      |        |
|                         |                                                                      | REF2_5V = 1, I <sub>VREF+</sub> min ≥ I <sub>VREF+</sub> ≥ −1mA                                                                 |                 | 2.9  |     |      |      |        |
| I <sub>VREF+</sub>      | Load current out of V <sub>REF+</sub> terminal                       |                                                                                                                                 | 2.2 V           | 0.01 |     |      | −0.5 | mA     |
|                         |                                                                      |                                                                                                                                 | 3 V             | 0.01 |     |      | −1   |        |
| I <sub>L(VREF)+</sub>   | Load-current regulation V <sub>REF+</sub> terminal                   | I <sub>VREF+</sub> = 500 μA +/- 100 μA, Analog input voltage ~0.75 V; REF2_5V = 0                                               | 2.2 V           |      |     |      | ±2   | LSB    |
|                         |                                                                      |                                                                                                                                 | 3 V             |      |     |      | ±2   |        |
|                         |                                                                      | I <sub>VREF+</sub> = 500 μA ± 100 μA, Analog input voltage ~1.25 V, REF2_5V = 1                                                 | 3 V             |      |     |      | ±2   | LSB    |
| I <sub>DL(VREF) +</sub> | Load current regulation V <sub>REF+</sub> terminal                   | I <sub>VREF+</sub> =100 μA → 900 μA, C <sub>VREF+</sub> =5 μF, ax ~0.5 x V <sub>REF+</sub> , Error of conversion result ≤ 1 LSB | 3 V             |      |     |      | 20   | ns     |
| C <sub>VREF+</sub>      | Capacitance at pin V <sub>REF+</sub> (see Note 1)                    | REFON =1, 0 mA ≤ I <sub>VREF+</sub> ≤ I <sub>VREF+</sub> max                                                                    | 2.2 V/3 V       | 5    | 10  |      | μF   |        |
| T <sub>REF+</sub>       | Temperature coefficient of built-in reference                        | I <sub>VREF+</sub> is a constant in the range of 0 mA ≤ I <sub>VREF+</sub> ≤ 1 mA                                               | 2.2 V/3 V       |      |     |      | ±100 | ppm/°C |
| t <sub>REFON</sub>      | Settle time of internal reference voltage (see Figure 23 and Note 2) | I <sub>VREF+</sub> = 0.5 mA, C <sub>VREF+</sub> = 10 μF, V <sub>REF+</sub> = 1.5 V, V <sub>AVCC</sub> = 2.2 V                   |                 |      |     |      | 17   | ms     |

NOTES: 1. The internal buffer operational amplifier and the accuracy specifications require an external capacitor. All INL and DNL tests uses two capacitors between pins V<sub>REF+</sub> and AV<sub>SS</sub> and V<sub>REF-</sub>/V<sub>eREF-</sub> and AV<sub>SS</sub>: 10 μF tantalum and 100 nF ceramic.  
2. The condition is that the error in a conversion started after t<sub>REFON</sub> is less than ±0.5 LSB. The settling time depends on the external capacitive load.

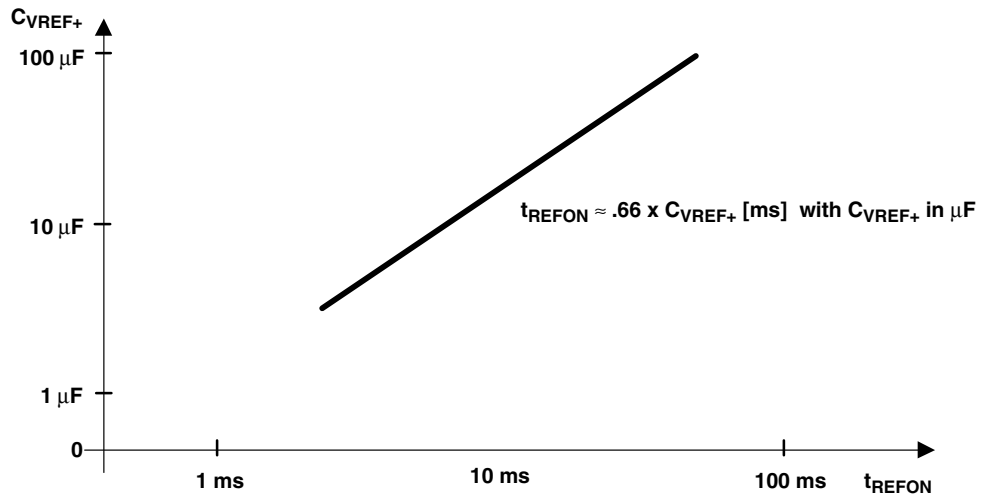


Figure 23. Typical Settling Time of Internal Reference  $t_{REFON}$  vs External Capacitor on  $V_{REF+}$

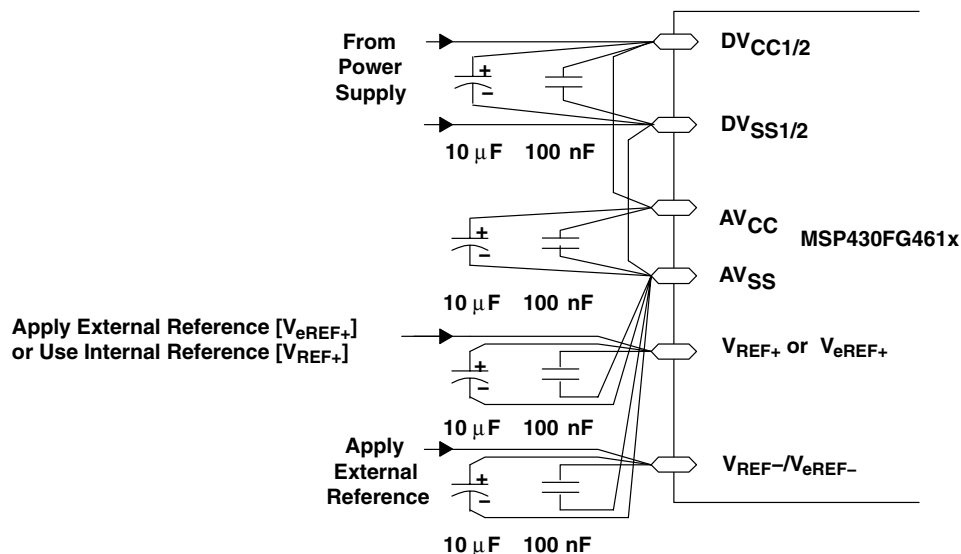


**Figure 24. Supply Voltage and Reference Voltage Design  $V_{REF-}/V_{REF+}$  External Supply**

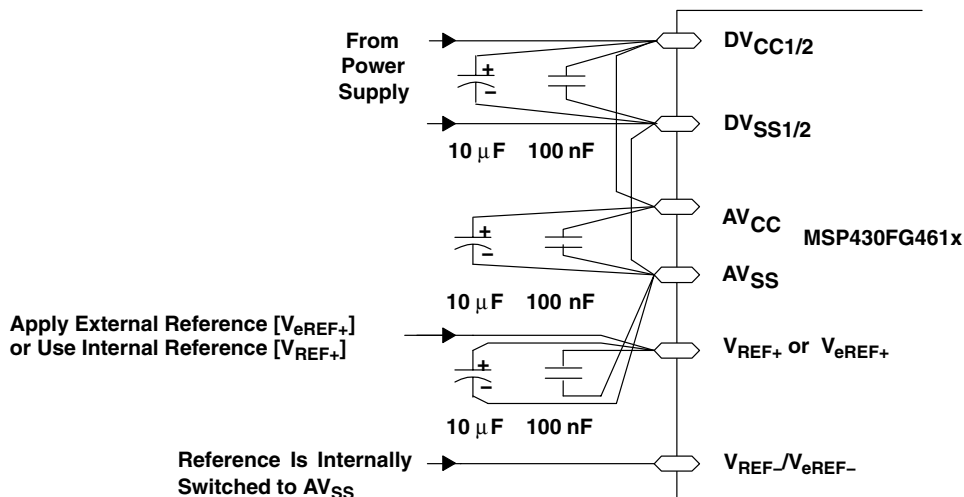


**Figure 25. Supply Voltage and Reference Voltage Design  $V_{REF-}/V_{REF+} = AV_{SS}$ , Internally Connected**

**electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)**

**12-bit ADC, timing parameters**

| PARAMETER             | TEST CONDITIONS                                                                                                                                                        | V <sub>CC</sub> | MIN  | TYP                                     | MAX  | UNIT |
|-----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|------|-----------------------------------------|------|------|
| f <sub>ADC12CLK</sub> | For specified performance of ADC12 linearity parameters                                                                                                                | 2.2V/3 V        | 0.45 | 5                                       | 6.3  | MHz  |
| f <sub>ADC12OSC</sub> | Internal ADC12 oscillator<br>ADC12DIV=0,<br>f <sub>ADC12CLK</sub> =f <sub>ADC12OSC</sub>                                                                               | 2.2 V/ 3 V      | 3.7  | 5                                       | 6.3  | MHz  |
| t <sub>CONVERT</sub>  | Conversion time<br>C <sub>VREF+</sub> ≥ 5 μF, Internal oscillator,<br>f <sub>ADC12OSC</sub> = 3.7 MHz to 6.3 MHz                                                       | 2.2 V/ 3 V      | 2.06 |                                         | 3.51 | μs   |
|                       | External f <sub>ADC12CLK</sub> from ACLK, MCLK, or SMCLK, ADC12SSEL ≠ 0                                                                                                |                 |      | 13×ADC12DIV×<br>1/f <sub>ADC12CLK</sub> |      | μs   |
| t <sub>ADC12ON</sub>  | Turn on settling time of the ADC<br>See Note 1                                                                                                                         |                 |      |                                         | 100  | ns   |
| t <sub>Sample</sub>   | Sampling time<br>R <sub>S</sub> = 400 Ω, R <sub>I</sub> = 1000 Ω,<br>C <sub>I</sub> = 30 pF, τ = [R <sub>S</sub> + R <sub>I</sub> ] × C <sub>I</sub> ,<br>(see Note 2) | 3 V             | 1220 |                                         |      | ns   |
|                       |                                                                                                                                                                        | 2.2 V           | 1400 |                                         |      |      |

- NOTES: 1. The condition is that the error in a conversion started after t<sub>ADC12ON</sub> is less than ±0.5 LSB. The reference and input signal are already settled.
2. Approximately ten Tau (τ) are needed to get an error of less than ±0.5 LSB:  
t<sub>Sample</sub> = ln(2<sup>n+1</sup>) × (R<sub>S</sub> + R<sub>I</sub>) × C<sub>I</sub> + 800 ns where n = ADC resolution = 12, R<sub>S</sub> = external source resistance.

**12-bit ADC, linearity parameters**

| PARAMETER      | TEST CONDITIONS                                                                                                                                                                                                                                                                 | V <sub>CC</sub> | MIN | TYP  | MAX  | UNIT |
|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-----|------|------|------|
| E <sub>I</sub> | Integral linearity error<br>1.4 V ≤ (V <sub>eREF+</sub> - V <sub>REF-/V<sub>eREF-</sub></sub> ) min ≤ 1.6 V                                                                                                                                                                     | 2.2 V/3 V       |     |      | ±2   | LSB  |
|                | 1.6 V < (V <sub>eREF+</sub> - V <sub>REF-/V<sub>eREF-</sub></sub> ) min ≤ [V <sub>AVCC</sub> ]                                                                                                                                                                                  |                 |     |      | ±1.7 |      |
| E <sub>D</sub> | Differential linearity error<br>(V <sub>eREF+</sub> - V <sub>REF-/V<sub>eREF-</sub></sub> ) <sub>min</sub> ≤ (V <sub>eREF+</sub> - V <sub>REF-/V<sub>eREF-</sub></sub> ),<br>C <sub>VREF+</sub> = 10 μF (tantalum) and 100 nF (ceramic)                                         | 2.2 V/3 V       |     |      | ±1   | LSB  |
| E <sub>O</sub> | Offset error<br>(V <sub>eREF+</sub> - V <sub>REF-/V<sub>eREF-</sub></sub> ) <sub>min</sub> ≤ (V <sub>eREF+</sub> - V <sub>REF-/V<sub>eREF-</sub></sub> ),<br>Internal impedance of source R <sub>S</sub> < 100 Ω,<br>C <sub>VREF+</sub> = 10 μF (tantalum) and 100 nF (ceramic) | 2.2 V/3 V       |     | ±2   | ±4   | LSB  |
| E <sub>G</sub> | Gain error<br>(V <sub>eREF+</sub> - V <sub>REF-/V<sub>eREF-</sub></sub> ) <sub>min</sub> ≤ (V <sub>eREF+</sub> - V <sub>REF-/V<sub>eREF-</sub></sub> ),<br>C <sub>VREF+</sub> = 10 μF (tantalum) and 100 nF (ceramic)                                                           | 2.2 V/3 V       |     | ±1.1 | ±2   | LSB  |
| E <sub>T</sub> | Total unadjusted error<br>(V <sub>eREF+</sub> - V <sub>REF-/V<sub>eREF-</sub></sub> ) <sub>min</sub> ≤ (V <sub>eREF+</sub> - V <sub>REF-/V<sub>eREF-</sub></sub> ),<br>C <sub>VREF+</sub> = 10 μF (tantalum) and 100 nF (ceramic)                                               | 2.2 V/3 V       |     | ±2   | ±5   | LSB  |

# MSP430x461x1, MSP430x461x MIXED SIGNAL MICROCONTROLLER

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

## 12-bit ADC, temperature sensor and built-in $V_{MID}$

| PARAMETER            | TEST CONDITIONS                                                   | $V_{CC}$                                                            | MIN           | TYP           | MAX             | UNIT            |
|----------------------|-------------------------------------------------------------------|---------------------------------------------------------------------|---------------|---------------|-----------------|-----------------|
| $I_{SENSOR}$         | Operating supply current into $AV_{CC}$ terminal (see Note 1)     | REFON = 0, INCH = 0Ah,<br>ADC12ON=NA, $T_A = 25^{\circ}C$           | 2.2 V         | 40            | 120             | $\mu A$         |
|                      |                                                                   |                                                                     | 3 V           | 60            | 160             |                 |
| $V_{SENSOR}$         | See Note 2                                                        | ADC12ON = 1, INCH = 0Ah,<br>$T_A = 0^{\circ}C$                      | 2.2 V/<br>3 V | 986           |                 | mV              |
| $TC_{SENSOR}$        |                                                                   | ADC12ON = 1, INCH = 0Ah                                             | 2.2 V/<br>3 V | 3.55 $\pm$ 3% |                 | mV/ $^{\circ}C$ |
| $t_{SENSOR(sample)}$ | Sample time required if<br>channel 10 is selected<br>(see Note 3) | ADC12ON = 1, INCH = 0Ah,<br>Error of conversion result $\leq 1$ LSB | 2.2 V         | 30            |                 | $\mu s$         |
|                      |                                                                   |                                                                     | 3 V           | 30            |                 |                 |
| $I_{VMID}$           | Current into divider at<br>channel 11 (see Note 4)                | ADC12ON = 1, INCH = 0Bh                                             | 2.2 V         |               | NA              | $\mu A$         |
|                      |                                                                   |                                                                     | 3 V           |               | NA              |                 |
| $V_{MID}$            | $AV_{CC}$ divider at channel 11                                   | ADC12ON = 1, INCH = 0Bh,<br>$V_{MID}$ is $\sim 0.5 \times V_{AVCC}$ | 2.2 V         | 1.1           | 1.1 $\pm$ 0.04  | V               |
|                      |                                                                   |                                                                     | 3 V           | 1.5           | 1.50 $\pm$ 0.04 |                 |
| $t_{VMID(sample)}$   | Sample time required if<br>channel 11 is selected<br>(see Note 5) | ADC12ON = 1, INCH = 0Bh,<br>Error of conversion result $\leq 1$ LSB | 2.2 V         | 1400          |                 | ns              |
|                      |                                                                   |                                                                     | 3 V           | 1220          |                 |                 |

- NOTES: 1. The sensor current  $I_{SENSOR}$  is consumed if (ADC12ON = 1 and REFON=1), or (ADC12ON=1 AND INCH=0Ah and sample signal is high). When REFON = 1,  $I_{SENSOR}$  is already included in  $I_{REF+}$ .
2. The temperature sensor offset can be as much as  $\pm 20^{\circ}C$ . A single-point calibration is recommended in order to minimize the offset error of the built-in temperature sensor.
3. The typical equivalent impedance of the sensor is 51 k $\Omega$ . The sample time required includes the sensor-on time  $t_{SENSOR(on)}$ .
4. No additional current is needed. The  $V_{MID}$  is used during sampling.
5. The on-time  $t_{VMID(on)}$  is included in the sampling time  $t_{VMID(sample)}$ ; no additional on time is needed.

**electrical characteristics over recommended operating free-air temperature (unless otherwise noted)**

**flash memory**

| PARAMETER                                                                          | TEST CONDITIONS       | V <sub>CC</sub> | MIN             | TYP             | MAX | UNIT             |
|------------------------------------------------------------------------------------|-----------------------|-----------------|-----------------|-----------------|-----|------------------|
| V <sub>CC(PGM/ERASE)</sub> Program and Erase supply voltage                        |                       |                 | 2.7             |                 | 3.6 | V                |
| f <sub>FTG</sub> Flash Timing Generator frequency                                  |                       |                 | 257             |                 | 476 | kHz              |
| I <sub>PGM</sub> Supply current from DV <sub>CC</sub> during program               |                       | 2.7 V/3.6 V     |                 | 3               | 5   | mA               |
| I <sub>ERASE</sub> Supply current from DV <sub>CC</sub> during erase               | See Note 3            | 2.7 V/3.6 V     |                 | 3               | 7   | mA               |
| I <sub>GMErase</sub> Supply current from DV <sub>CC</sub> during global mass erase | See Note 4            | 2.7 V/3.6 V     |                 | 6               | 14  | mA               |
| t <sub>CPT</sub> Cumulative program time                                           | See Note 1            | 2.7 V/3.6 V     |                 |                 | 10  | ms               |
| t <sub>CMErase</sub> Cumulative mass erase time                                    |                       | 2.7 V/3.6 V     | 20              |                 |     | ms               |
| Program/Erase endurance                                                            |                       |                 | 10 <sup>4</sup> | 10 <sup>5</sup> |     | cycles           |
| t <sub>Retention</sub> Data retention duration                                     | T <sub>J</sub> = 25°C |                 | 100             |                 |     | years            |
| t <sub>Word</sub> Word or byte program time                                        | See Note 2            |                 |                 | 30              |     | t <sub>FTG</sub> |
| t <sub>Block, 0</sub> Block program time for 1 <sup>st</sup> byte or word          |                       |                 |                 | 25              |     |                  |
| t <sub>Block, 1-63</sub> Block program time for each additional byte or word       |                       |                 |                 | 18              |     |                  |
| t <sub>Block, End</sub> Block program end-sequence wait time                       |                       |                 |                 | 6               |     |                  |
| t <sub>Mass Erase</sub> Mass erase time                                            |                       |                 |                 | 10593           |     |                  |
| t <sub>Global Mass Erase</sub> Global mass erase time                              |                       |                 |                 | 10593           |     |                  |
| t <sub>Seq Erase</sub> Segment erase time                                          |                       |                 |                 | 4819            |     |                  |

- NOTES: 6. The cumulative program time must not be exceeded during a block-write operation. This parameter is only relevant if the block write feature is used.
2. These values are hardwired into the Flash Controller's state machine (t<sub>FTG</sub> = 1/f<sub>FTG</sub>).
3. Lower 64-KB or upper 64-KB Flash memory erased.
4. All Flash memory erased.

**JTAG interface**

| PARAMETER                                                               | TEST CONDITIONS | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|-------------------------------------------------------------------------|-----------------|-----------------|-----|-----|-----|------|
| f <sub>TCK</sub> TCK input frequency                                    | See Note 1      | 2.2 V           | 0   |     | 5   | MHz  |
|                                                                         |                 | 3 V             | 0   |     | 10  | MHz  |
| R <sub>Internal</sub> Internal pull-up resistance on TMS, TCK, TDI/TCLK | See Note 2      | 2.2 V/ 3 V      | 25  | 60  | 90  | kΩ   |

- NOTES: 1. f<sub>TCK</sub> may be restricted to meet the timing requirements of the module selected.
2. TMS, TDI/TCLK, and TCK pull-up resistors are implemented in all versions.

**JTAG fuse (see Note 1)**

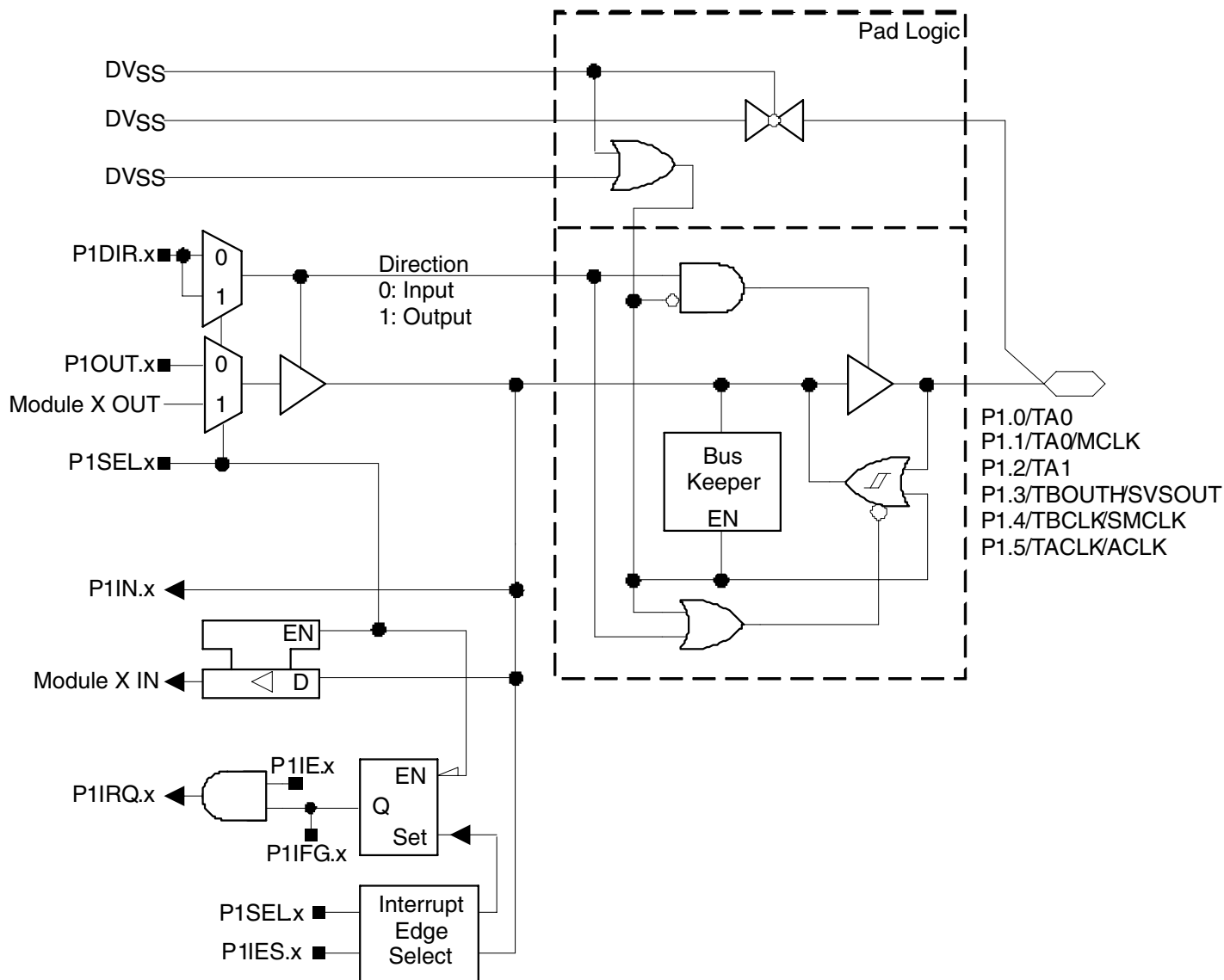
| PARAMETER                                                           | TEST CONDITIONS       | MIN | TYP | MAX | UNIT |
|---------------------------------------------------------------------|-----------------------|-----|-----|-----|------|
| V <sub>CC(FB)</sub> Supply voltage during fuse-blow condition       | T <sub>A</sub> = 25°C | 2.5 |     |     | V    |
| V <sub>FB</sub> Voltage level on TDI/TCLK for fuse-blow: F versions |                       | 6   |     | 7   | V    |
| I <sub>FB</sub> Supply current into TDI/TCLK during fuse blow       |                       |     |     | 100 | mA   |
| t <sub>FB</sub> Time to blow fuse                                   |                       |     |     | 1   | ms   |

NOTE 1: Once the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

## APPLICATION INFORMATION

### input/output schematics

port P1, P1.0 to P1.5, input/output with Schmitt trigger



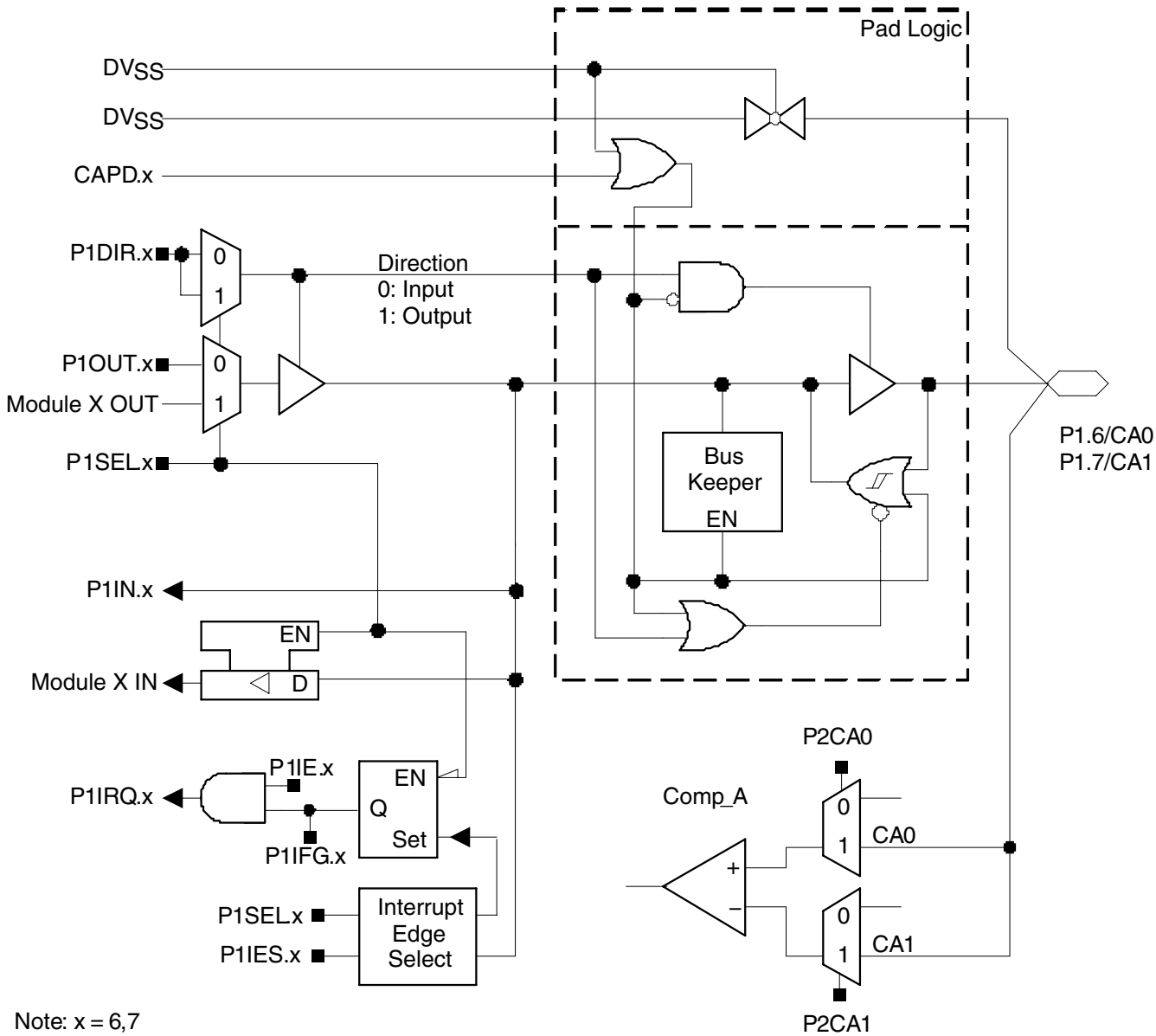
Note: x = 0,1,2,3,4,5

**port P1 (P1.0 to P1.5) pin functions**

| PIN NAME (P1.X)    | X | FUNCTION        | CONTROL BITS / SIGNALS |         |
|--------------------|---|-----------------|------------------------|---------|
|                    |   |                 | P1DIR.x                | P1SEL.x |
| P1.0/TA0           | 0 | P1.0 (I/O)      | I: 0; O: 1             | 0       |
|                    |   | Timer_A3.CCI0A  | 0                      | 1       |
|                    |   | Timer_A3.TA0    | 1                      | 1       |
| P1.1/TA0/MCLK      | 1 | P1.1 (I/O)      | I: 0; O: 1             | 0       |
|                    |   | Timer_A3.CCI0B  | 0                      | 1       |
|                    |   | MCLK            | 1                      | 1       |
| P1.2/TA1           | 2 | P1.2 (I/O)      | I: 0; O: 1             | 0       |
|                    |   | Timer_A3.CCI1A  | 0                      | 1       |
|                    |   | Timer_A3.TA1    | 1                      | 1       |
| P1.3/TBOUTH/SVSOUT | 3 | P1.3 (I/O)      | I: 0; O: 1             | 0       |
|                    |   | Timer_B7.TBOUTH | 0                      | 1       |
|                    |   | SVSOUT          | 1                      | 1       |
| P1.4/TBCLK/SMCLK   | 4 | P1.4 (I/O)      | I: 0; O: 1             | 0       |
|                    |   | Timer_B7.TBCLK  | 0                      | 1       |
|                    |   | SMCLK           | 1                      | 1       |
| P1.5/TACLK/ACLK    | 5 | P1.5 (I/O)      | I: 0; O: 1             | 0       |
|                    |   | Timer_A3.TACLK  | 0                      | 1       |
|                    |   | ACLK            | 1                      | 1       |

MSP430x461x1, MSP430x461x  
MIXED SIGNAL MICROCONTROLLER

port P1, P1.6, P1.7, input/output with Schmitt trigger



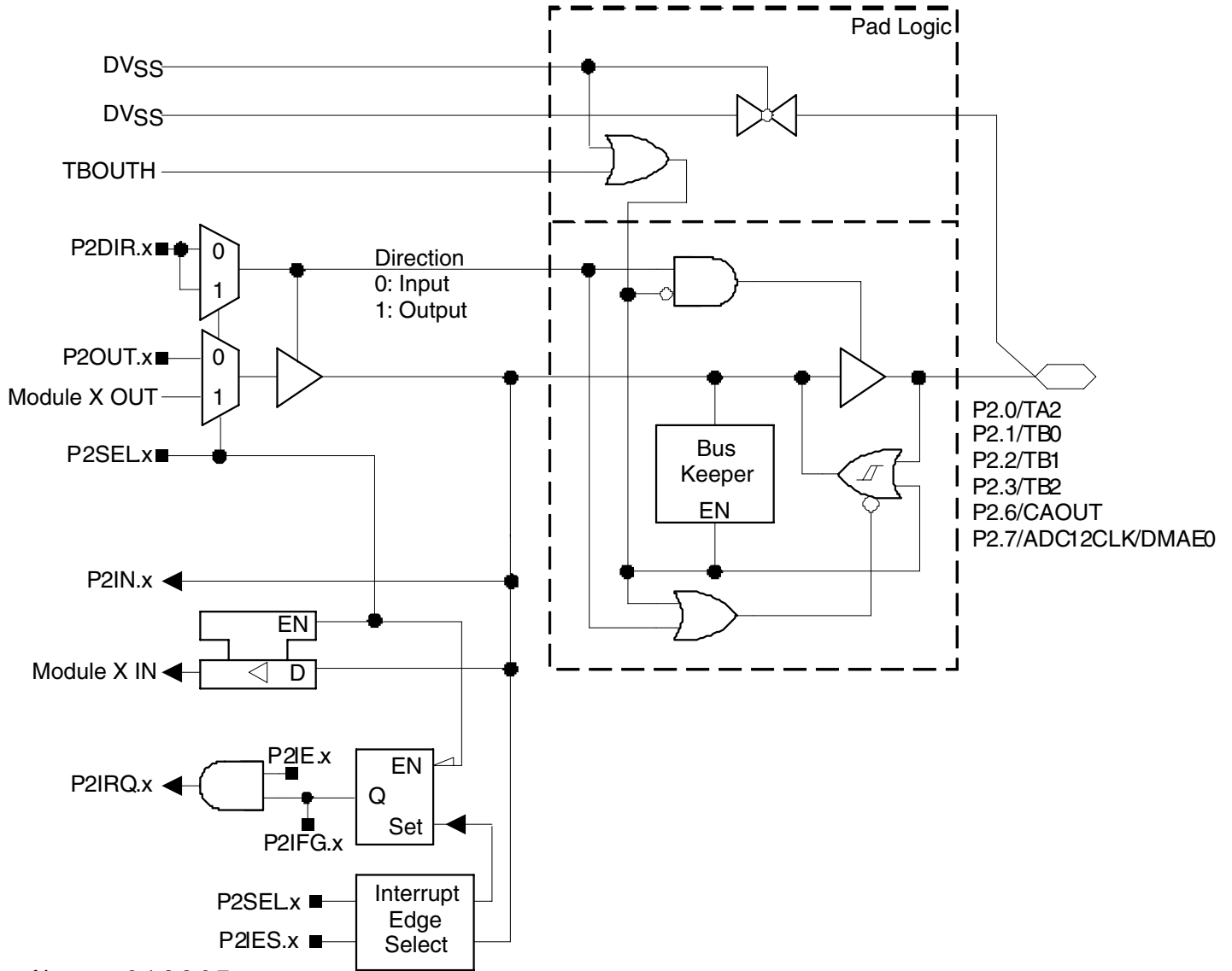
Note: x = 6,7

port P1 (P1.6 and P1.7) pin functions

| PIN NAME (P1.X) | X | FUNCTION   | CONTROL BITS / SIGNALS |            |         |
|-----------------|---|------------|------------------------|------------|---------|
|                 |   |            | CAPD.x                 | P1DIR.x    | P1SEL.x |
| P1.6/CA0        | 6 | P1.6 (I/O) | 0                      | I: 0; O: 1 | 0       |
|                 |   | CA0        | 1                      | X          | X       |
| P1.7/CA1        | 7 | P1.7 (I/O) | 0                      | I: 0; O: 1 | 0       |
|                 |   | CA1        | 1                      | X          | X       |

NOTE 1: X: Don't care.

port P2, P2.0 to P2.3, P2.6 to P2.7, input/output with Schmitt trigger



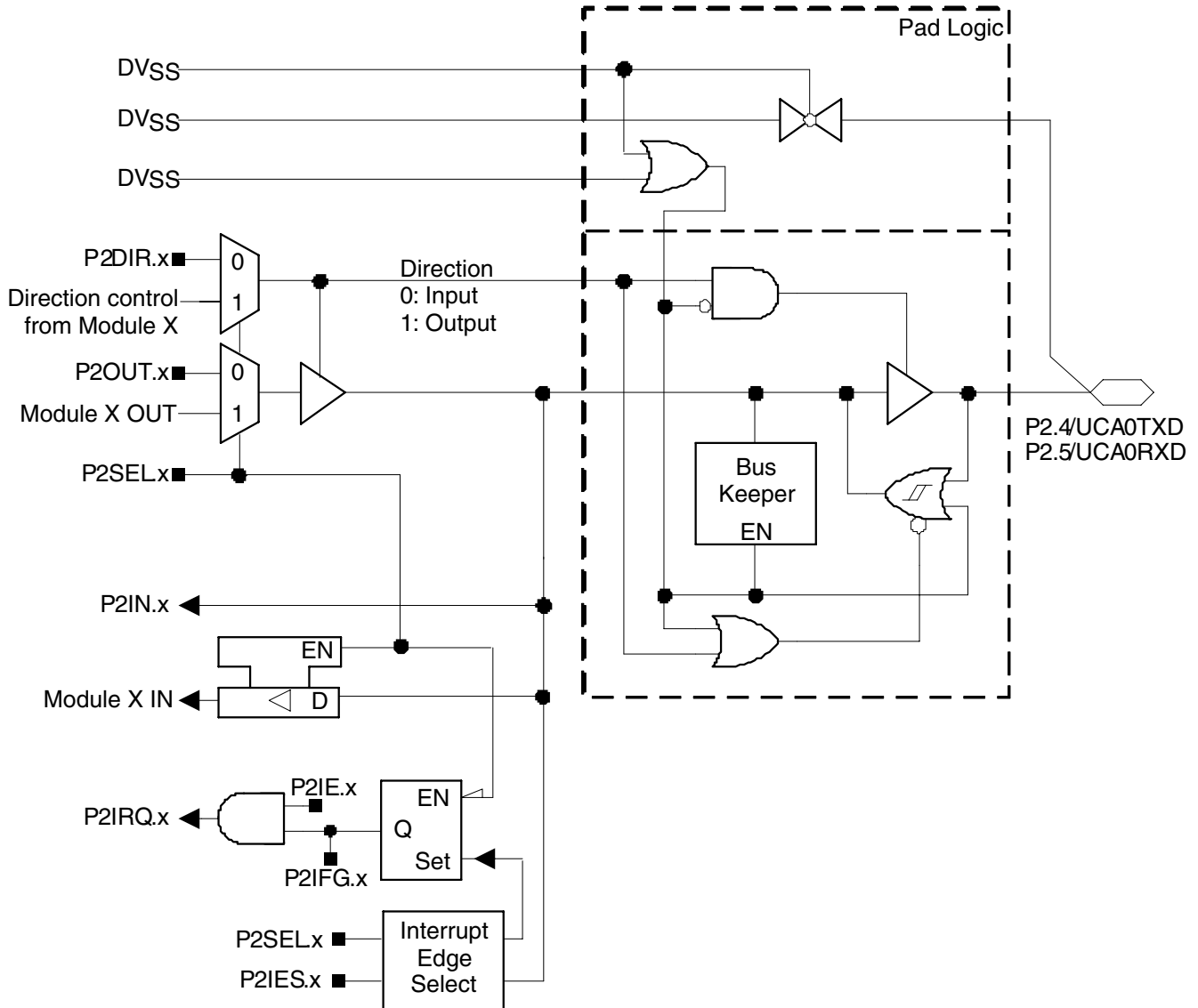
# MSP430x461x1, MSP430x461x MIXED SIGNAL MICROCONTROLLER

## port P2 (P2.0, P2.1, P2.2, P2.3, P2.6 and P2.7) pin functions

| PIN NAME (P2.X)     | X | FUNCTION                          | CONTROL BITS / SIGNALS |         |
|---------------------|---|-----------------------------------|------------------------|---------|
|                     |   |                                   | P2DIR.x                | P2SEL.x |
| P2.0/TA2            | 0 | P2.0 (I/O)                        | I: 0; O: 1             | 0       |
|                     |   | Timer_A3.CCI2A                    | 0                      | 1       |
|                     |   | Timer_A3.TA2                      | 1                      | 1       |
| P2.1/TB0            | 1 | P2.1 (I/O)                        | I: 0; O: 1             | 0       |
|                     |   | Timer_B7.CCI0A and Timer_B7.CCI0B | 0                      | 1       |
|                     |   | Timer_B7.TB0 (see Note 1)         | 1                      | 1       |
| P2.2/TB1            | 2 | P2.2 (I/O)                        | I: 0; O: 1             | 0       |
|                     |   | Timer_B7.CCI1A and Timer_B7.CCI1B | 0                      | 1       |
|                     |   | Timer_B7.TB1 (see Note 1)         | 1                      | 1       |
| P2.3/TB3            | 3 | P2.3 (I/O)                        | I: 0; O: 1             | 0       |
|                     |   | Timer_B7.CCI2A and Timer_B7.CCI2B | 0                      | 1       |
|                     |   | Timer_B7.TB3 (see Note 1)         | 1                      | 1       |
| P2.6/CAOUT          | 6 | P2.6 (I/O)                        | I: 0; O: 1             | 0       |
|                     |   | CAOUT                             | 1                      | 1       |
| P2.7/ADC12CLK/DMAE0 | 7 | P2.7 (I/O)                        | I: 0; O: 1             | 0       |
|                     |   | ADC12CLK (MSP430F461x only)       | 1                      | 1       |
|                     |   | DMAE0                             | 0                      | 1       |

NOTE 1: Setting TBOUTH causes all Timer\_B outputs to be set to high impedance.

port P2, P2.4 to P2.5, input/output with Schmitt trigger



Note: x = 4,5

port P2 (P2.4 and P2.5) pin functions

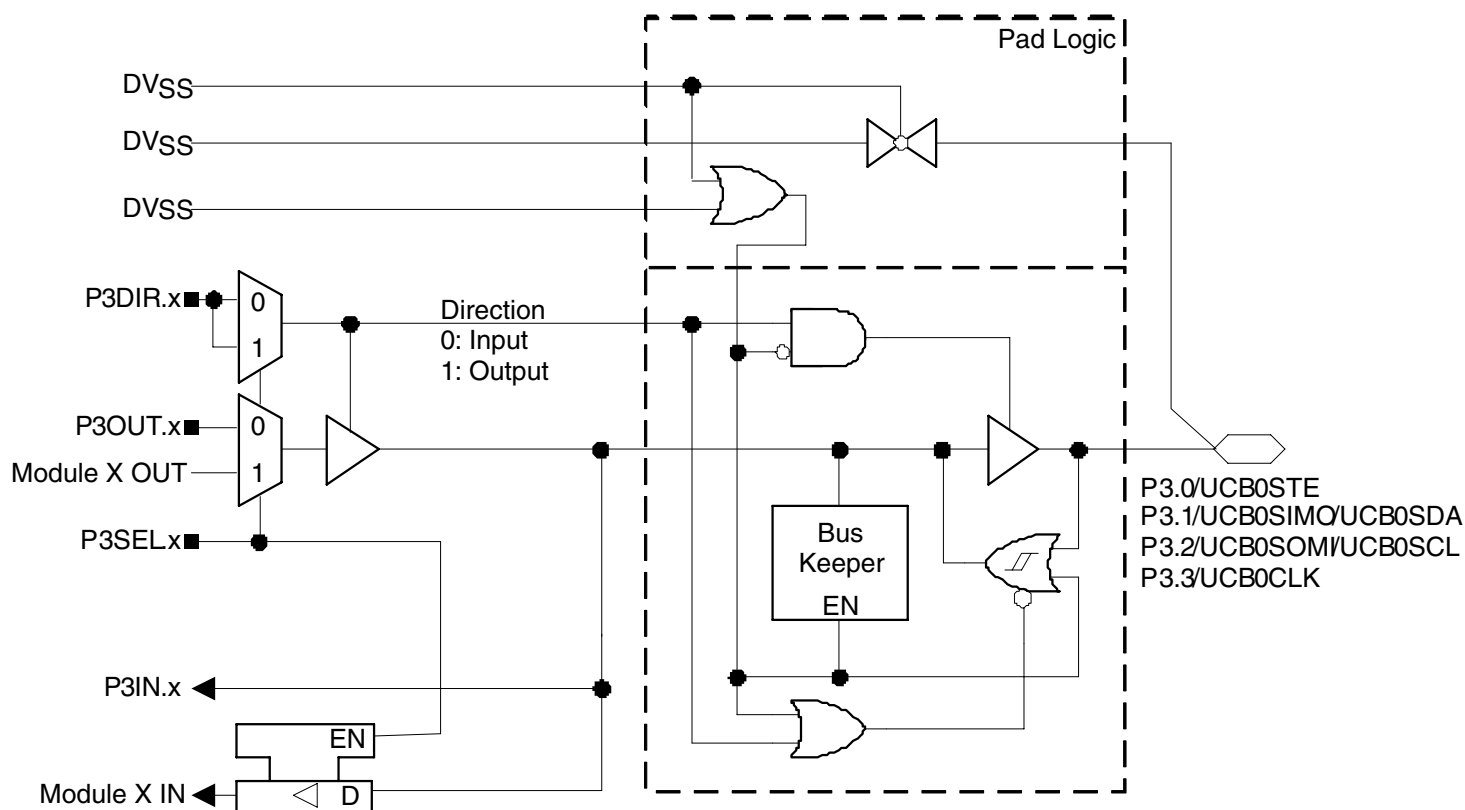
| PIN NAME (P2.X) | X | FUNCTION                        | CONTROL BITS / SIGNALS |         |
|-----------------|---|---------------------------------|------------------------|---------|
|                 |   |                                 | P2DIR.x                | P2SEL.x |
| P2.4/UC A0TXD   | 4 | P2.4 (I/O)                      | I: 0; O: 1             | 0       |
|                 |   | USCI_A0.UCA0TXD (see Note 1, 2) | X                      | 1       |
| P2.5/UC A0RXD   | 5 | P2.5 (I/O)                      | I: 0; O: 1             | 0       |
|                 |   | USCI_A0.UCA0RXD (see Note 1, 2) | X                      | 1       |

NOTES: 1. X: Don't care.

2. When in USCI mode, P2.4 is set to output, P2.5 is set to input.

# MSP430x461x1, MSP430x461x MIXED SIGNAL MICROCONTROLLER

**port P3, P3.0 to P3.3, input/output with Schmitt trigger**



Note:  $x = 0, 1, 2, 3$

### port P3 (P3.0 to P3.3) pin functions

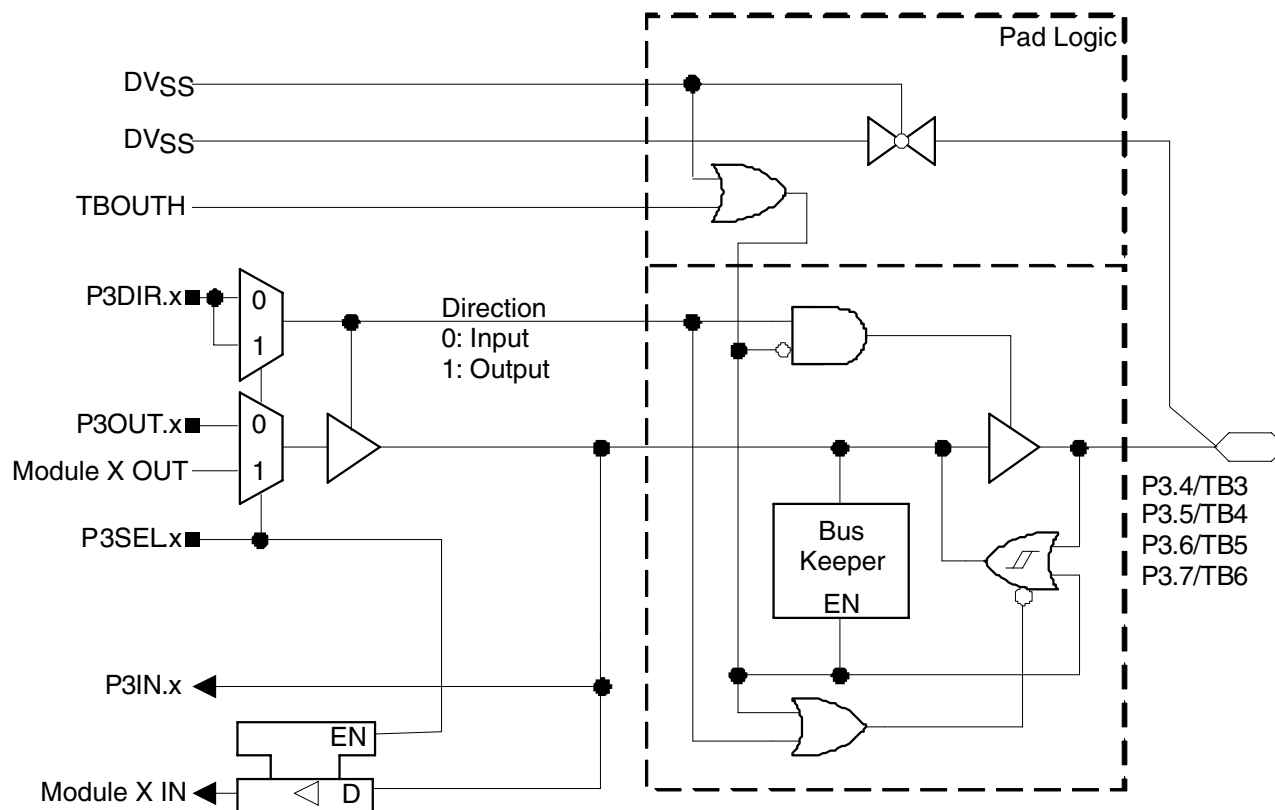
| PIN NAME (P3.X)           | X | FUNCTION                             | CONTROL BITS / SIGNALS |         |
|---------------------------|---|--------------------------------------|------------------------|---------|
|                           |   |                                      | P3DIR.x                | P3SEL.x |
| P3.0/UCB0STE              | 0 | P3.0 (I/O)                           | I: 0; O: 1             | 0       |
|                           |   | UCB0STE (see Notes 1, 2)             | X                      | 1       |
| P3.1/UCB0SIMO/<br>UCB0SDA | 1 | P3.1 (I/O)                           | I: 0; O: 1             | 0       |
|                           |   | UCB0SIMO/UCB0SDA (see Notes 1, 2, 3) | X                      | 1       |
| P3.2/UCB0SOMI/<br>UCB0SCL | 2 | P3.2 (I/O)                           | I: 0; O: 1             | 0       |
|                           |   | UCB0SOMI/UCB0SCL (see Notes 1, 2, 3) | X                      | 1       |
| P3.3/UCB0CLK              | 3 | P3.3 (I/O)                           | I: 0; O: 1             | 0       |
|                           |   | UCB0CLK (see Notes 1, 2)             | X                      | 1       |

NOTES: 1. X: Don't care.

2. The pin direction is controlled by the USCI module.

3. In case the I2C functionality is selected the output drives only the logical 0 to  $V_{SS}$  level.

**port P3, P3.4 to P3.7, input/output with Schmitt trigger**



Note: x = 4,5,6,7

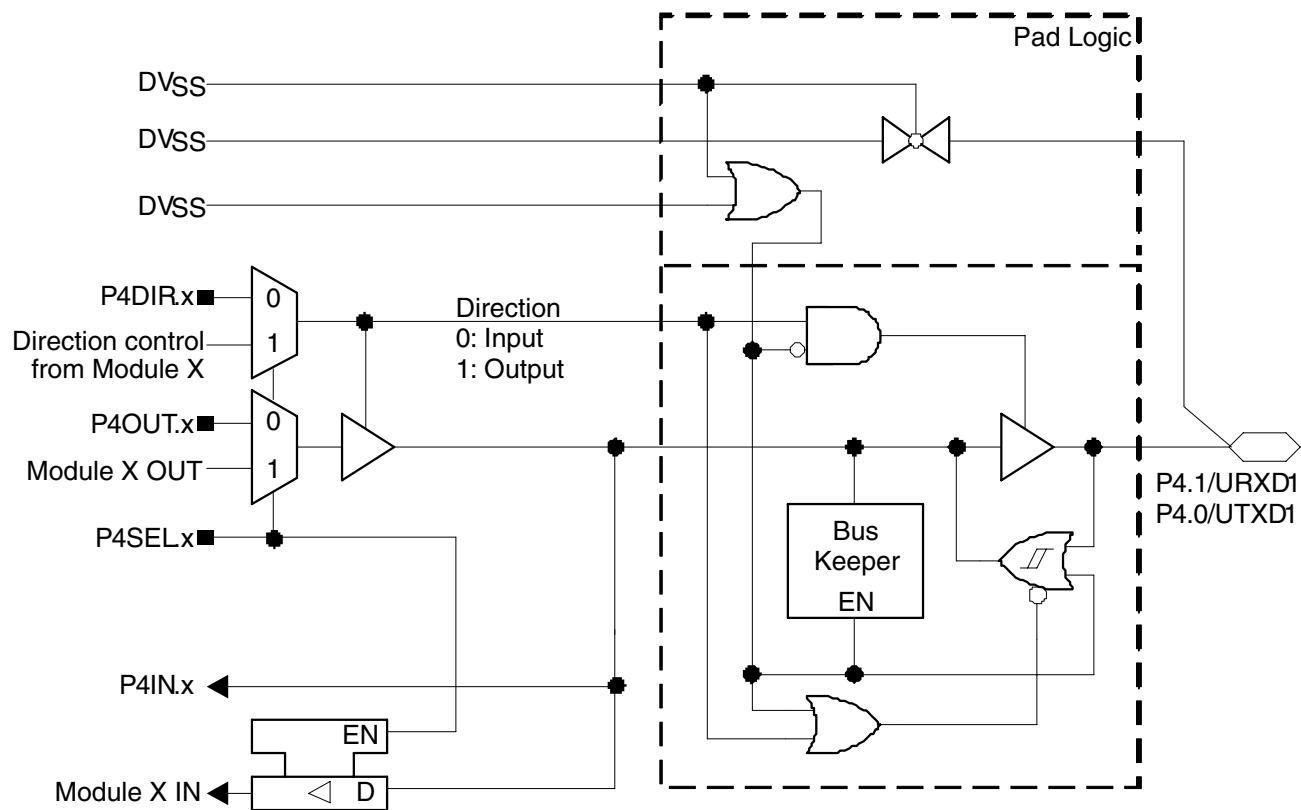
**port P3 (P3.4 to P3.7) pin functions**

| PIN NAME (P3.X) | X | FUNCTION                          | CONTROL BITS / SIGNALS |         |
|-----------------|---|-----------------------------------|------------------------|---------|
|                 |   |                                   | P3DIR.x                | P3SEL.x |
| P3.4/TB3        | 4 | P3.4 (I/O)                        | I: 0; O: 1             | 0       |
|                 |   | Timer_B7.CCI3A and Timer_B7.CCI3B | 0                      | 1       |
|                 |   | Timer_B7.TB3 (see Note 1)         | 1                      | 1       |
| P3.5/TB4        | 5 | P3.5 (I/O)                        | I: 0; O: 1             | 0       |
|                 |   | Timer_B7.CCI4A and Timer_B7.CCI4B | 0                      | 1       |
|                 |   | Timer_B7.TB4 (see Note 1)         | 1                      | 1       |
| P3.6/TB5        | 6 | P3.6 (I/O)                        | I: 0; O: 1             | 0       |
|                 |   | Timer_B7.CCI5A and Timer_B7.CCI5B | 0                      | 1       |
|                 |   | Timer_B7.TB5 (see Note 1)         | 1                      | 1       |
| P3.7/TB6        | 7 | P3.7 (I/O)                        | I: 0; O: 1             | 0       |
|                 |   | Timer_B7.CCI6A and Timer_B7.CCI6B | 0                      | 1       |
|                 |   | Timer_B7.TB6 (see Note 1)         | 1                      | 1       |

NOTE 1: Setting TBOUTH causes all Timer\_B outputs to be set to high impedance.

MSP430x461x1, MSP430x461x  
MIXED SIGNAL MICROCONTROLLER

port P4, P4.0 to P4.1, input/output with Schmitt trigger



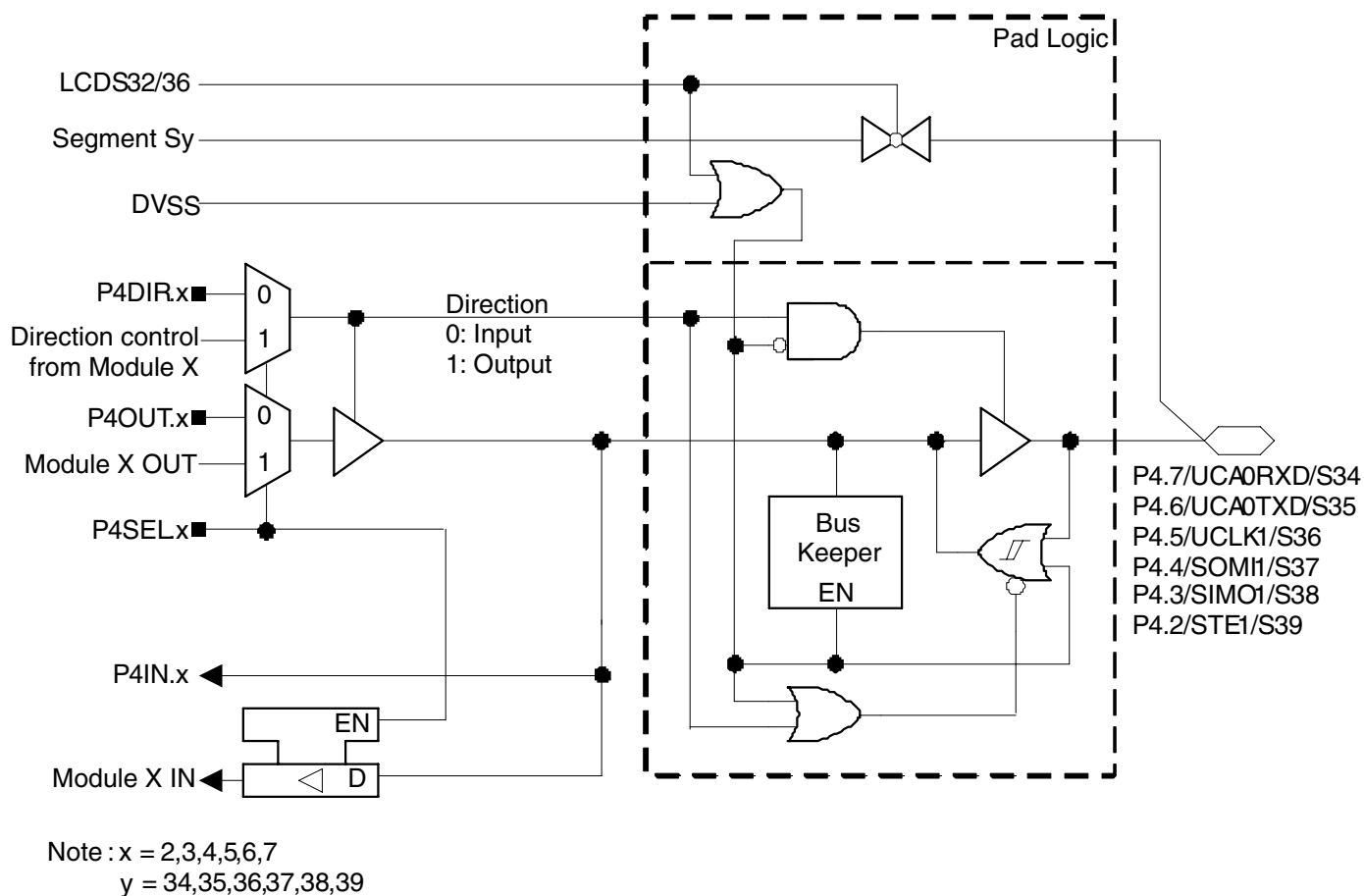
Note: x = 0,1

port P4 (P4.0 to P4.1) pin functions

| PIN NAME (P4.X) | X | FUNCTION                      | CONTROL BITS / SIGNALS |         |
|-----------------|---|-------------------------------|------------------------|---------|
|                 |   |                               | P4DIR.x                | P4SEL.x |
| P4.0/UTXD1      | 0 | P4.0 (I/O)                    | I: 0; O: 1             | 0       |
|                 |   | USART1.UTXD1 (see Notes 1, 2) | X                      | 1       |
| P4.1/URXD1      | 1 | P4.1 (I/O)                    | I: 0; O: 1             | 0       |
|                 |   | USART1.URXD1 (see Notes 1, 2) | X                      | 1       |

NOTES: 1. X: Don't care.  
2. When in USART1 mode, P4.0 is set to output, P4.1 is set to input.

**port P4, P4.2 to P4.7, input/output with Schmitt trigger**



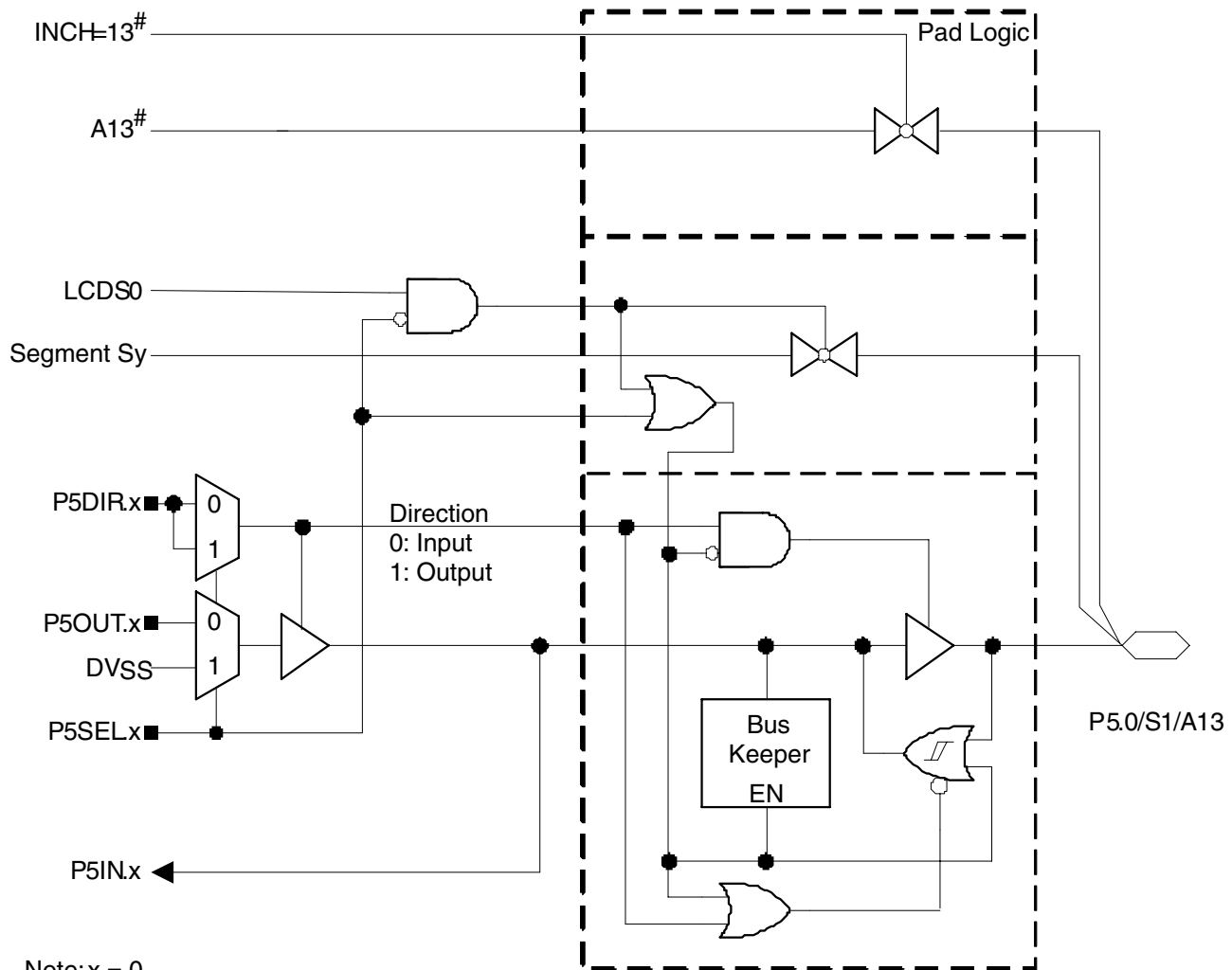
# MSP430x461x1, MSP430x461x MIXED SIGNAL MICROCONTROLLER

## port P4 (P4.2 to P4.5) pin functions

| PIN NAME (P4.X)  | X | FUNCTION                         | CONTROL BITS / SIGNALS |         |        |
|------------------|---|----------------------------------|------------------------|---------|--------|
|                  |   |                                  | P4DIR.x                | P4SEL.x | LCDS36 |
| P4.2/STE1/S39    | 2 | P4.2 (I/O)                       | I: 0; O: 1             | 0       | 0      |
|                  |   | USART1.STE1                      | X                      | 1       | 0      |
|                  |   | S39 (see Note 1)                 | X                      | X       | 1      |
| P4.3/SIMO/S38    | 3 | P4.3 (I/O)                       | I: 0; O: 1             | 0       | 0      |
|                  |   | USART1.SIMO1 (see Notes 1, 2)    | X                      | 1       | 0      |
|                  |   | S38 (see Note 1)                 | X                      | X       | 1      |
| P4.4/SOMI/S37    | 4 | P4.4 (I/O)                       | I: 0; O: 1             | 0       | 0      |
|                  |   | USART1.SOMI1 (see Notes 1, 2)    | X                      | 1       | 0      |
|                  |   | S37 (see Note 1)                 | X                      | X       | 1      |
| P4.5/SOMI/S36    | 5 | P4.5 (I/O)                       | I: 0; O: 1             | 0       | 0      |
|                  |   | USART1.UCLK1 (see Notes 1, 2)    | X                      | 1       | 0      |
|                  |   | S36 (see Note 1)                 | X                      | X       | 1      |
| P4.6/UCA0TXD/S35 | 6 | P4.6 (I/O)                       | I: 0; O: 1             | 0       | 0      |
|                  |   | USCI_A0.UCA0TXD (see Notes 1, 3) | X                      | 1       | 0      |
|                  |   | S35 (see Note 1)                 | X                      | X       | 1      |
| P4.7/UCA0RXD/S34 | 7 | P4.7 (I/O)                       | I: 0; O: 1             | 0       | 0      |
|                  |   | USCI_A0.UCA0RXD (see Notes 1, 3) | X                      | 1       | 0      |
|                  |   | S34 (see Note 1)                 | X                      | X       | 1      |

NOTES: 1. X: Don't care.  
2. The pin direction is controlled by the USART1 module.  
3. When in USCI mode, P4.6 is set to output, P4.7 is set to input.

**port P5, P5.0, input/output with Schmitt trigger**



Note: x = 0  
y = 1  
# = Signal from or to ADC12  
(MSP430x461x only)

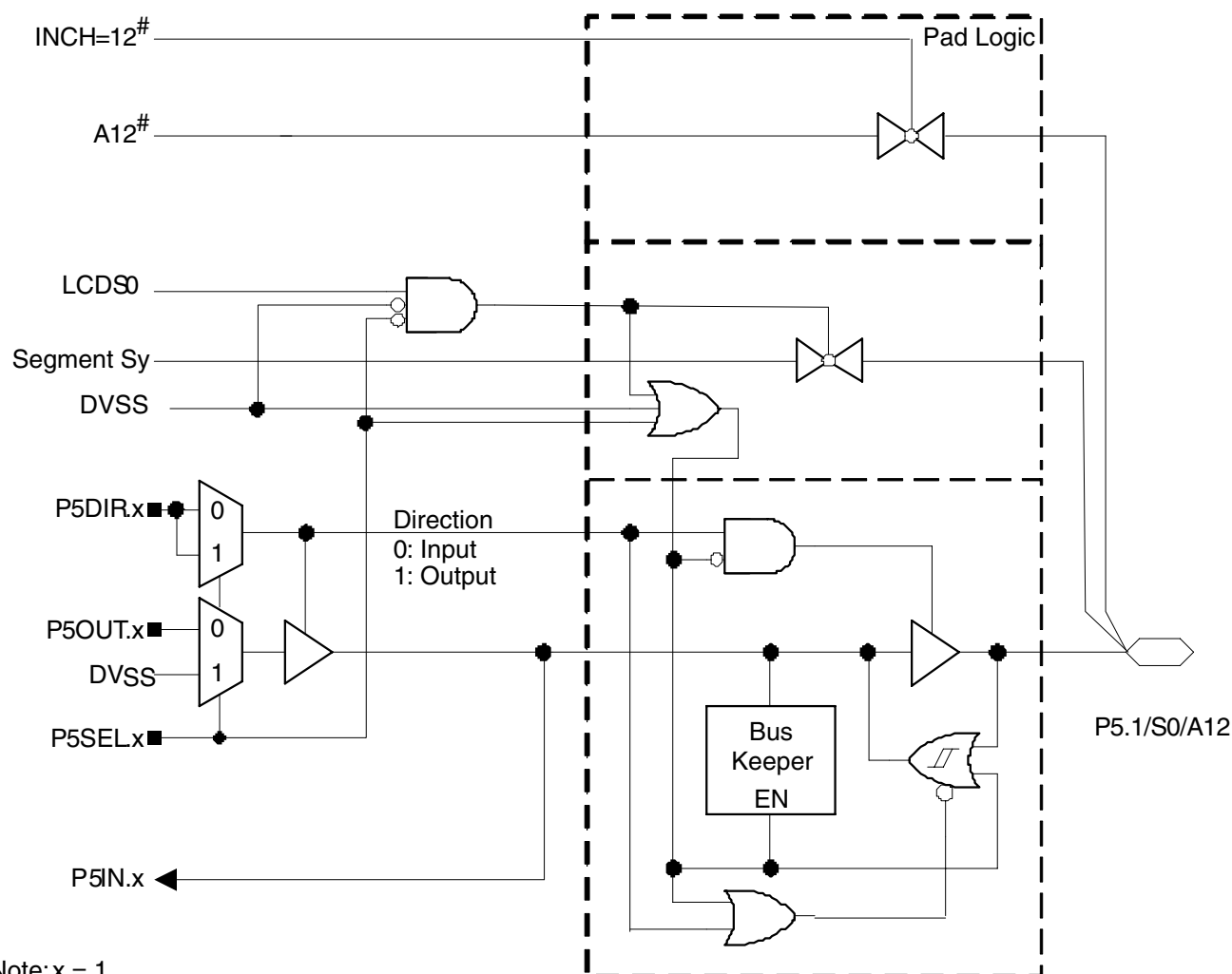
**port P5 (P5.0) pin functions**

| PIN NAME (P5.X) | X | FUNCTION                               | CONTROL BITS / SIGNALS |         |       |        |
|-----------------|---|----------------------------------------|------------------------|---------|-------|--------|
|                 |   |                                        | P5DIR.x                | P5SEL.x | INCHx | LCD S0 |
| P5.0/S1/A13     | 0 | P5.0 (I/O) (see Note 1)                | I: 0; O: 1             | 0       | X     | 0      |
|                 |   | A13 (MSP430x461x only, see Notes 1, 3) | X                      | 1       | 13    | X      |
|                 |   | S1 enabled (see Note 1)                | X                      | 0       | X     | 1      |
|                 |   | S1 disabled (see Note 1)               | X                      | 1       | X     | 1      |

NOTES: 1. X: Don't care.  
2. N/A: Not available or not applicable.  
3. Setting the P5SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

# MSP430x461x1, MSP430x461x MIXED SIGNAL MICROCONTROLLER

**port P5, P5.1, input/output with Schmitt trigger**



Note:  $x = 1$   
 $y = 0$

# = Signal from or to ADC12  
(MSP430x461x only)

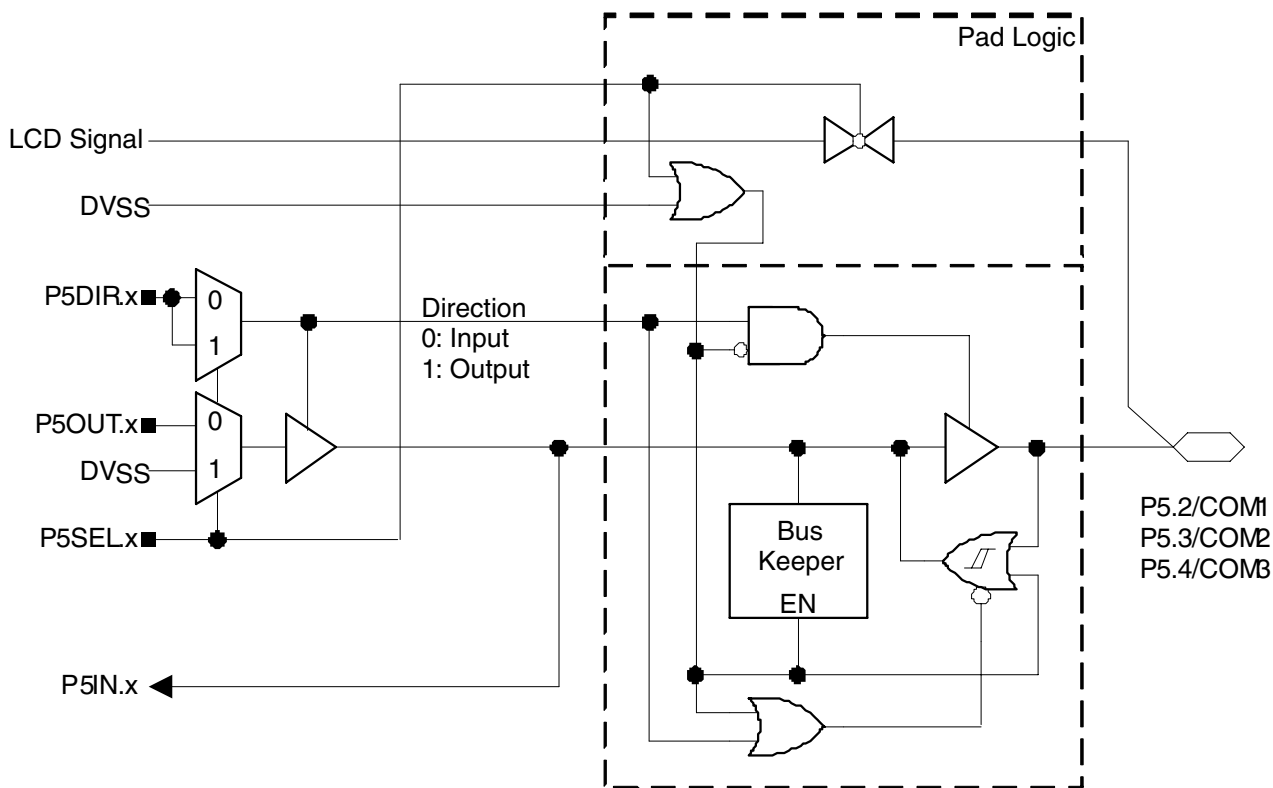
### port P5 (P5.1) pin functions

| PIN NAME (P5.X) | X | FUNCTION                               | CONTROL BITS / SIGNALS |         |       |       |
|-----------------|---|----------------------------------------|------------------------|---------|-------|-------|
|                 |   |                                        | P5DIR.x                | P5SEL.x | INCHx | LCDS0 |
| P5.1/S0/A12     | 1 | P5.1 (I/O) (see Note 1)                | I: 0; O: 1             | 0       | X     | 0     |
|                 |   | A12 (MSP430x461x only, see Notes 1, 2) | X                      | 1       | 12    | 0     |
|                 |   | S0 enabled (see Note 1)                | X                      | 0       | X     | 1     |
|                 |   | S0 disabled<br>(see Note 1)            | X                      | 1       | X     | 1     |

NOTES: 1. X: Don't care.

2. Setting the P5SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

**port P5, P5.2 to P5.4, input/output with Schmitt trigger**



Note: x = 2,3,4

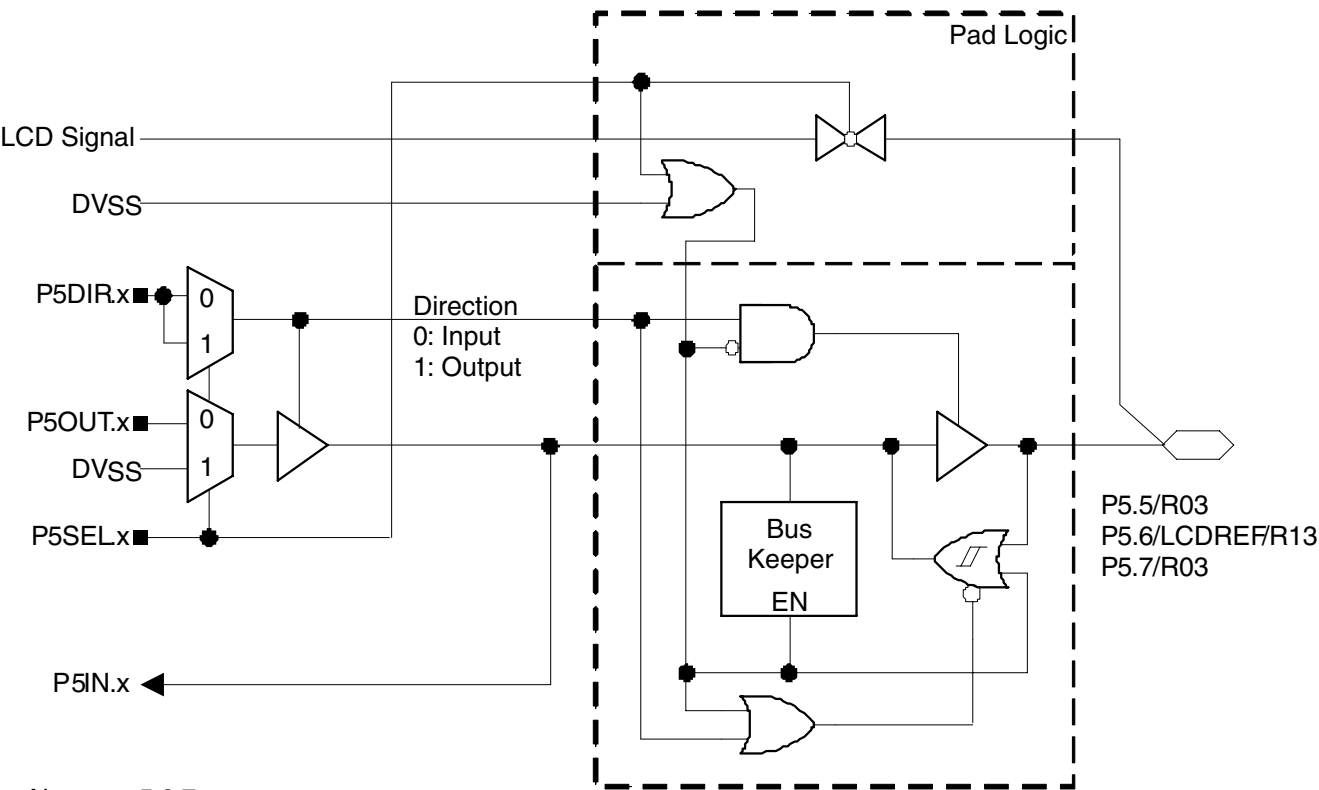
**port P5 (P5.2 to P5.4) pin functions**

| PIN NAME (P5.X) | X | FUNCTION          | CONTROL BITS / SIGNALS |         |
|-----------------|---|-------------------|------------------------|---------|
|                 |   |                   | P5DIR.x                | P5SEL.x |
| P5.2/COM1       | 2 | P5.2 (I/O)        | I: 0; O: 1             | 0       |
|                 |   | COM1 (see Note 1) | X                      | 1       |
| P5.3/COM2       | 3 | P5.3 (I/O)        | I: 0; O: 1             | 0       |
|                 |   | COM2 (see Note 1) | X                      | 1       |
| P5.4/COM3       | 4 | P5.4 (I/O)        | I: 0; O: 1             | 0       |
|                 |   | COM3 (see Note 1) | X                      | 1       |

NOTE 1: X: Don't care.

MSP430x461x1, MSP430x461x  
MIXED SIGNAL MICROCONTROLLER

port P5, P5.5 to P5.7, input/output with Schmitt trigger

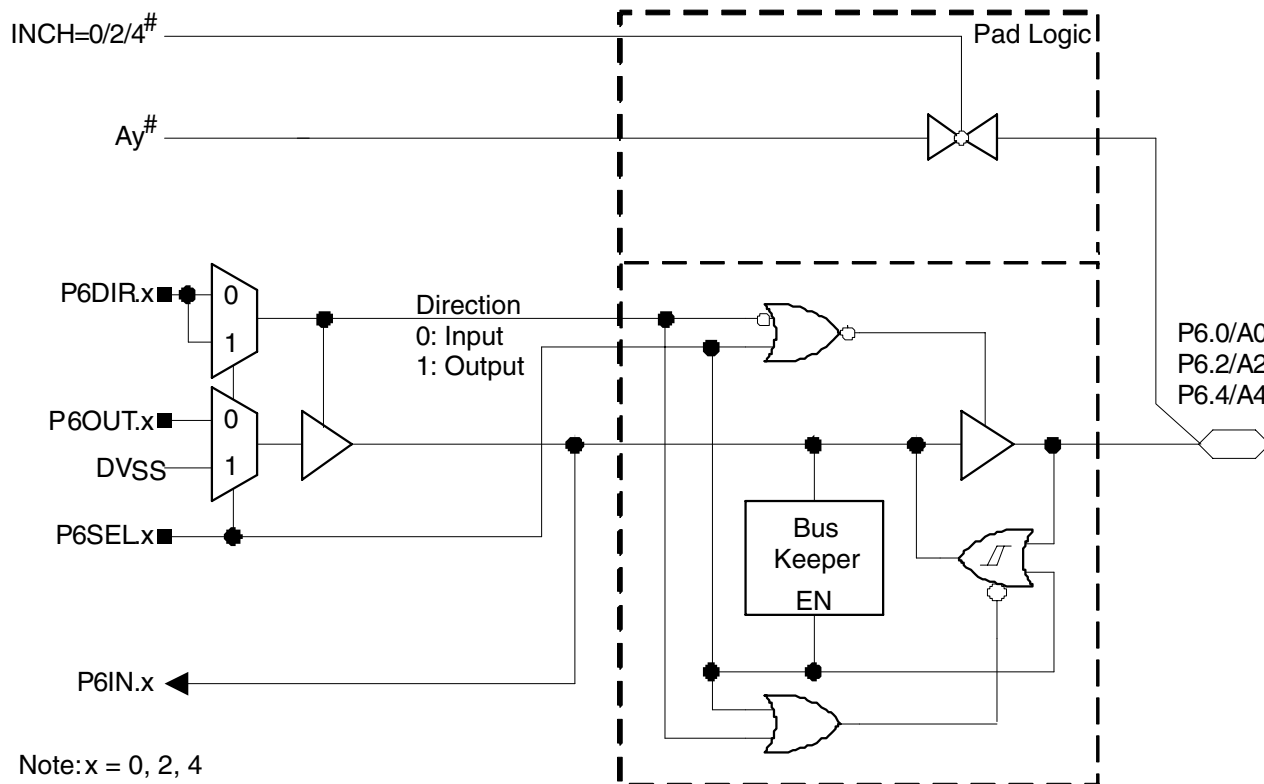


port P5 (P5.5 to P5.7) pin functions

| PIN NAME (P5.X) | X | FUNCTION                       | CONTROL BITS / SIGNALS |         |
|-----------------|---|--------------------------------|------------------------|---------|
|                 |   |                                | P5DIR.x                | P5SEL.x |
| P5.5/R03        | 5 | P5.5 (I/O)                     | I: 0; O: 1             | 0       |
|                 |   | R03 (see Note 1)               | X                      | 1       |
| P5.6/LCDREF/R13 | 6 | P5.6 (I/O)                     | I: 0; O: 1             | 0       |
|                 |   | R13 or LCDREF (see Notes 1, 2) | X                      | 1       |
| P5.7/R03        | 7 | P5.7 (I/O)                     | I: 0; O: 1             | 0       |
|                 |   | R03 (see Note 1)               | X                      | 1       |

NOTES: 1. X: Don't care.  
2. External reference for the LCD\_A charge pump is applied when VLCDREFx = 01. Otherwise R13 is selected.

**port P6, P6.0, P6.2, and P6.4, input/output with Schmitt trigger**



Note: x = 0, 2, 4

y = 0, 1

# = Signal from or to ADC12  
 (MSP430x461x only)

**port P6 (P6.0, P6.2, and P6.4) pin functions**

| PIN NAME (P6.X) | X | FUNCTION                              | CONTROL BITS / SIGNALS |         |       |
|-----------------|---|---------------------------------------|------------------------|---------|-------|
|                 |   |                                       | P6DIR.x                | P6SEL.x | INCHx |
| P6.0/A0         | 0 | P6.0 (I/O) (see Note 1)               | I: 0; O: 1             | 0       | X     |
|                 |   | A0 (MSP430x461x only, see Notes 1, 3) | X                      | 1       | 0     |
| P6.2/A2         | 2 | P6.2 (I/O) (see Note 1)               | I: 0; O: 1             | 0       | X     |
|                 |   | A2 (MSP430x461x only, see Notes 1, 3) | X                      | 1       | 2     |
| P6.4/A4         | 4 | P6.4 (I/O) (see Note 1)               | I: 0; O: 1             | 0       | X     |
|                 |   | A4 (MSP430x461x only, see Notes 1, 3) | X                      | 1       | 4     |

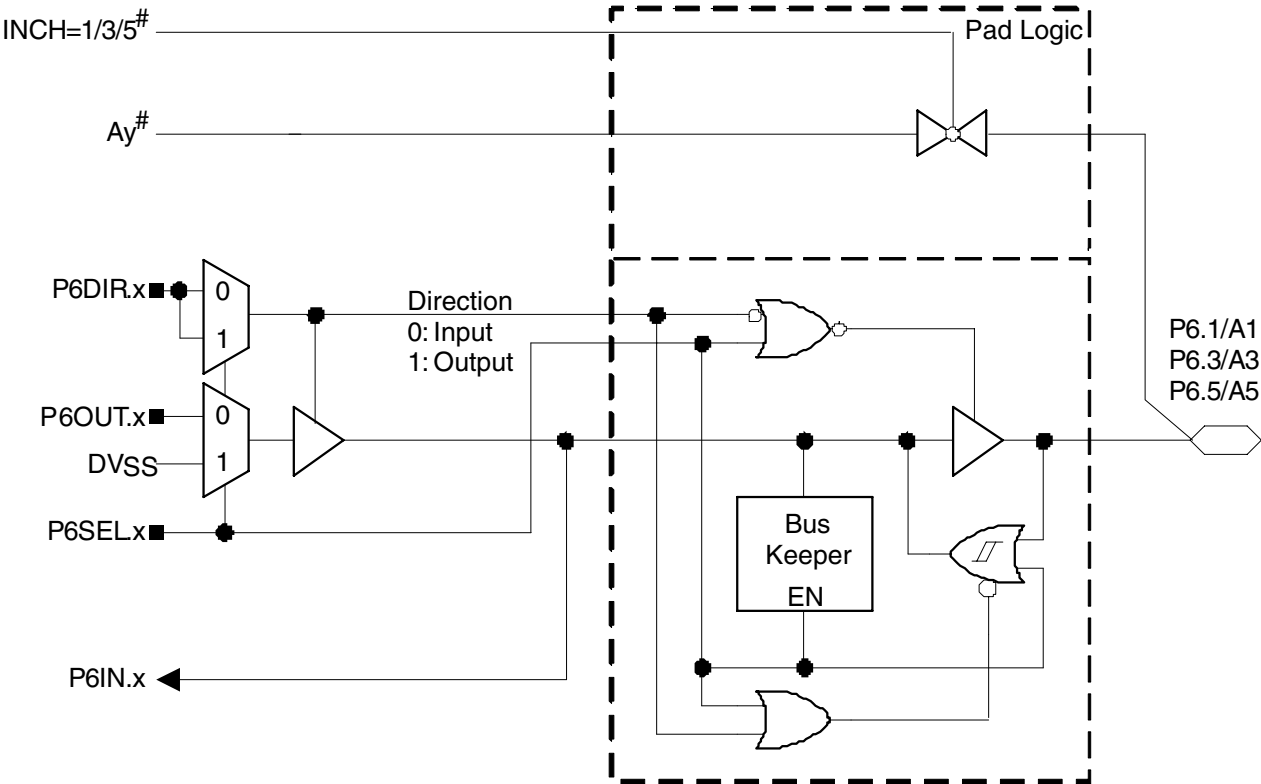
NOTES: 1. X: Don't care.

2. N/A: Not available or not applicable.

3. Setting the P6SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

MSP430x461x1, MSP430x461x  
MIXED SIGNAL MICROCONTROLLER

port P6, P6.1, P6.3, and P6.5 input/output with Schmitt trigger



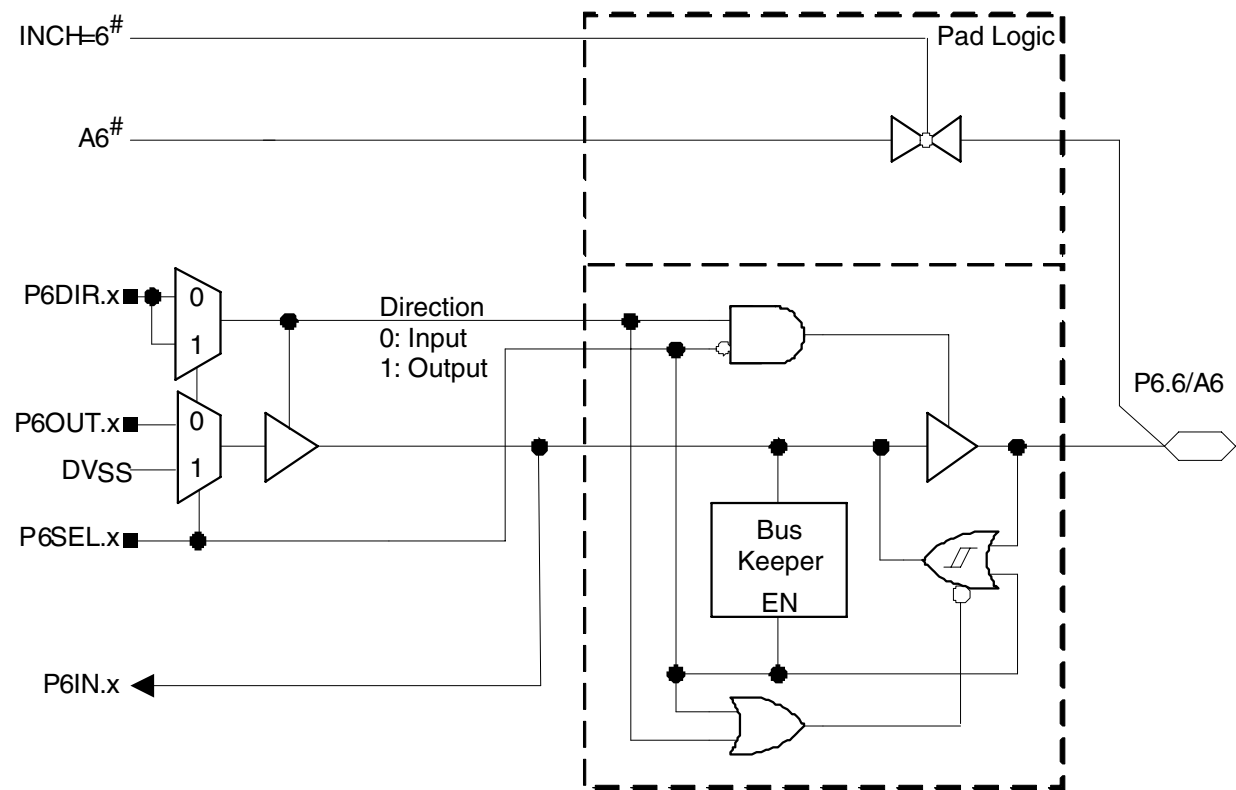
Note: x = 1, 3, 5  
y = 0, 1, 2  
# = Signal from or to ADC12  
(MSP430x461x only)

port P6 (P6.1, P6.3, and P6.5) pin functions

| PIN NAME (P6.X) | X | FUNCTION                              | CONTROL BITS / SIGNALS |         |       |
|-----------------|---|---------------------------------------|------------------------|---------|-------|
|                 |   |                                       | P6DIR.x                | P6SEL.x | INCHx |
| P6.1/A1         | 1 | P6.1 (I/O) (see Note 1)               | I: 0; O: 1             | 0       | X     |
|                 |   | A1 (MSP430x461x only, see Notes 1, 3) | X                      | 1       | 1     |
| P6.3/A3         | 3 | P6.3 (I/O) (see Note 1)               | I: 0; O: 1             | 0       | X     |
|                 |   | A3 (MSP430x461x only, see Notes 1, 3) | X                      | 1       | 3     |
| P6.5/A5         | 5 | P6.5 (I/O) (see Note 1)               | I: 0; O: 1             | 0       | X     |
|                 |   | A5 (MSP430x461x only, see Notes 1, 3) | X                      | 1       | 5     |

NOTES: 1. X: Don't care.  
2. N/A: Not available or not applicable.  
3. Setting the P6SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

port P6, P6.6, input/output with Schmitt trigger



Note: x = 6  
# = Signal from or to ADC12  
(MSP430x461 only)

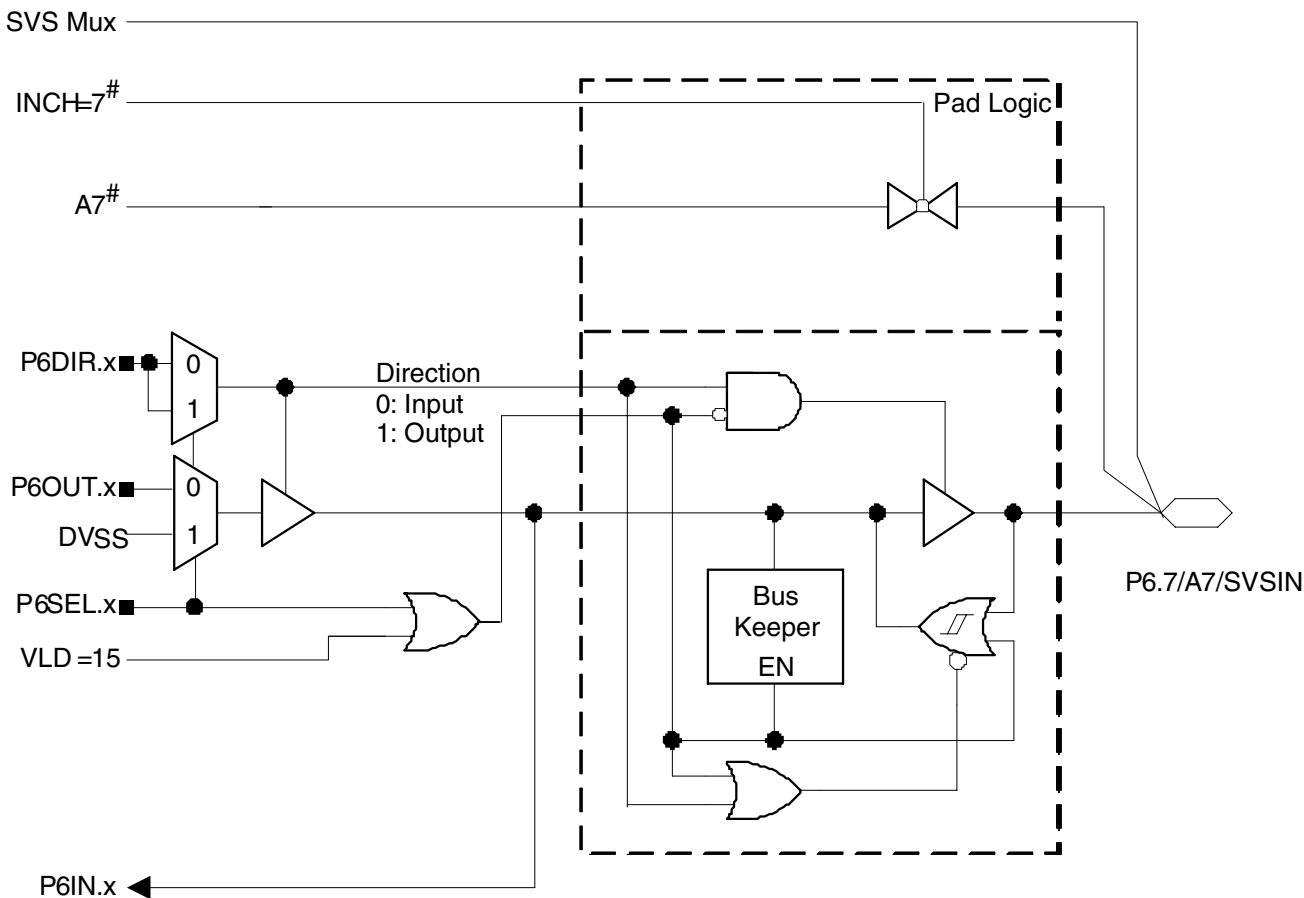
port P6 (P6.6) pin functions

| PIN NAME (P6.X) | X | FUNCTION                              | CONTROL BITS / SIGNALS |         |       |
|-----------------|---|---------------------------------------|------------------------|---------|-------|
|                 |   |                                       | P6DIR.x                | P6SEL.x | INCHx |
| P6.6/A6         | 6 | P6.6 (I/O) (see Note 1)               | I: 0; O: 1             | 0       | X     |
|                 |   | A6 (MSP430x461x only, see Notes 1, 2) | X                      | 1       | 6     |

NOTES: 1. X: Don't care.  
2. Setting the P6SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

MSP430x461x1, MSP430x461x  
MIXED SIGNAL MICROCONTROLLER

port P6, P6.7, input/output with Schmitt trigger



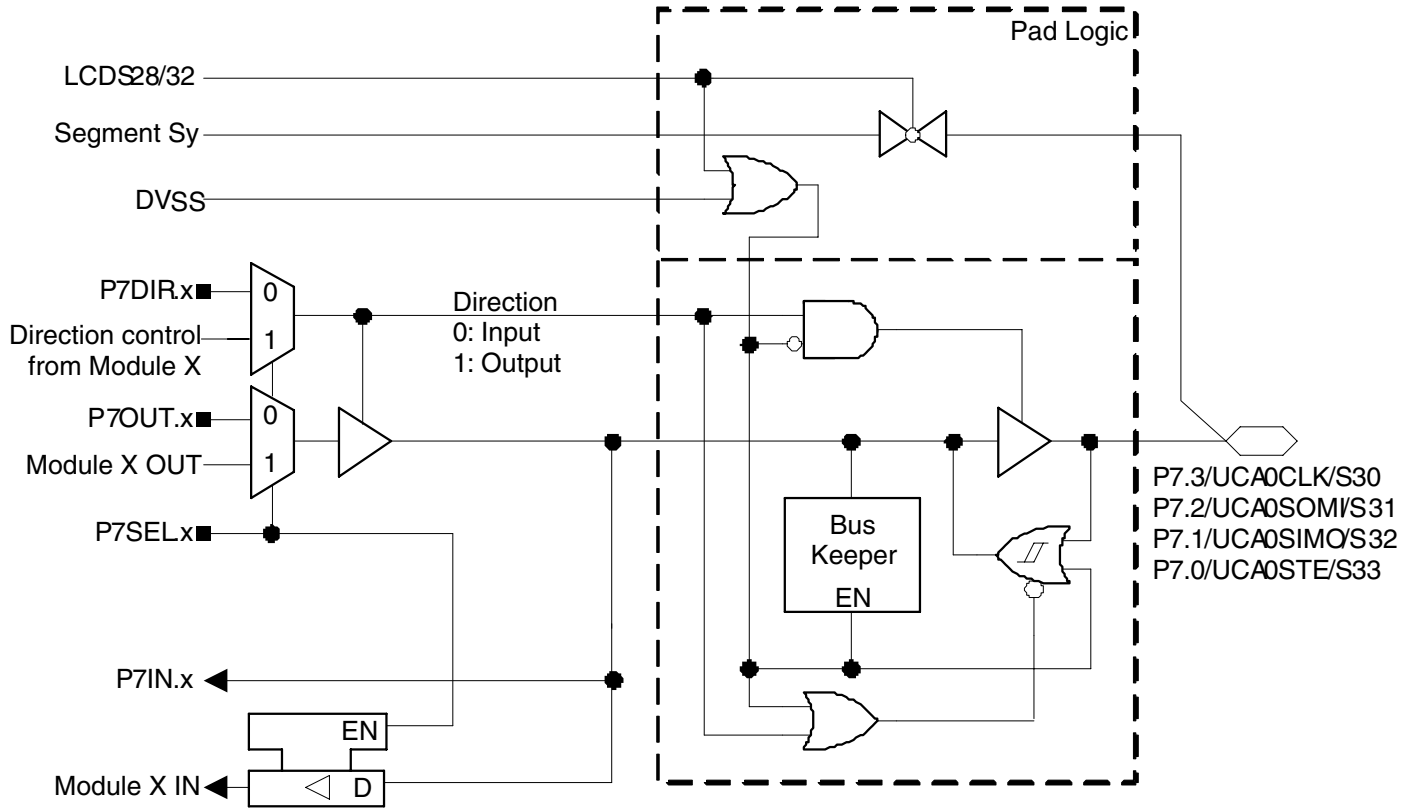
Note: x = 7  
# = Signal from or to ADC12  
(MSP430x461x only)

port P6 (P6.7) pin functions

| PIN NAME (P6.X) | X | FUNCTION                              | CONTROL BITS / SIGNALS |         |       |
|-----------------|---|---------------------------------------|------------------------|---------|-------|
|                 |   |                                       | P6DIR.x                | P6SEL.x | INCHx |
| P6.7/A7/SVSIN   | 7 | P6.7 (I/O) (see Note 1)               | I: 0; O: 1             | 0       | X     |
|                 |   | A7 (MSP430x461x only, see Notes 1, 2) | X                      | 1       | 7     |
|                 |   | SVSIN (see Notes 1,3)                 | 0                      | 1       | 0     |

NOTES: 1. X: Don't care.  
2. Setting the P6SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.  
3. Setting VLDx = 15 will also cause the external SVSIN to be used. In this case, the P6SEL.x bit is a do not care.

**port P7, P7.0 to P7.3, input/output with Schmitt trigger**



Note: x = 0, 1, 2, 3  
 y = 30, 31, 32, 33

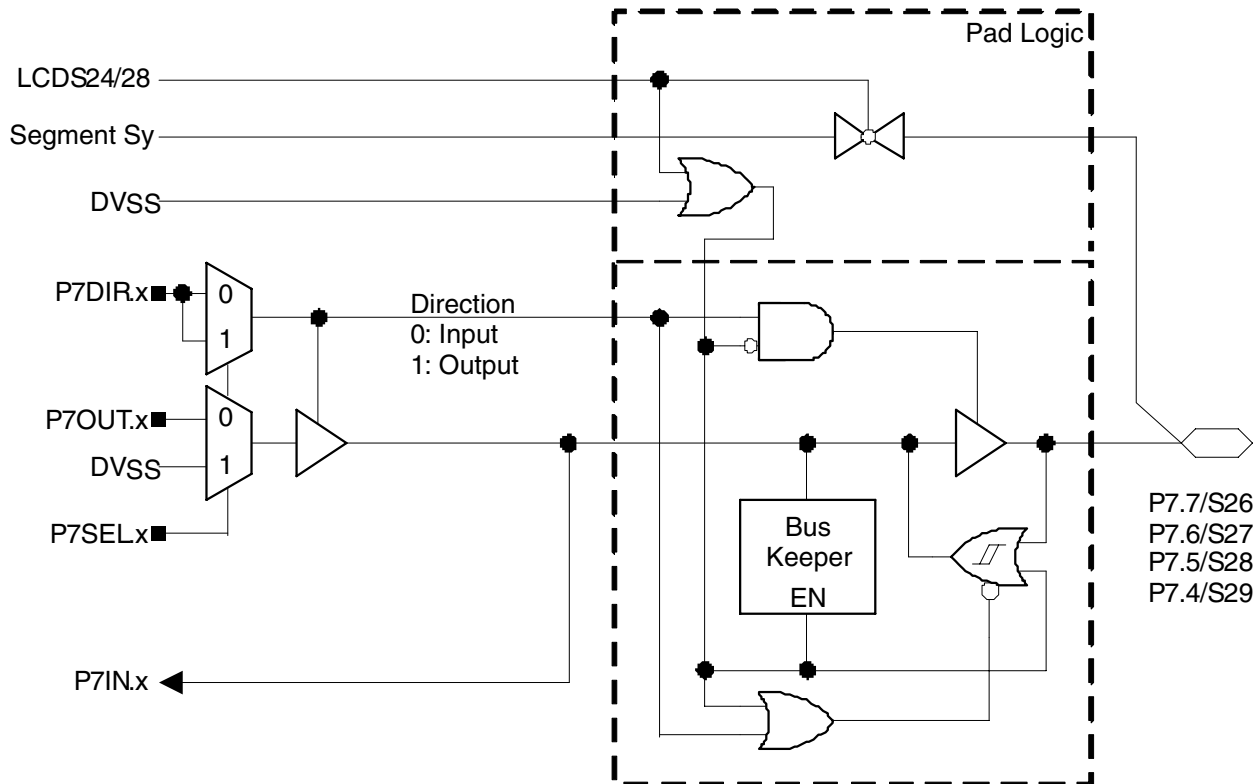
# MSP430x461x1, MSP430x461x MIXED SIGNAL MICROCONTROLLER

## port P7 (P7.0 to P7.1) pin functions

| PIN NAME (P7.X)   | X | FUNCTION                          | CONTROL BITS / SIGNALS |         |        |
|-------------------|---|-----------------------------------|------------------------|---------|--------|
|                   |   |                                   | P7DIR.x                | P7SEL.x | LCDS32 |
| P7.0/UCA0STE/S33  | 0 | P7.0 (I/O)                        | I: 0; O: 1             | 0       | 0      |
|                   |   | USCI_A0.UCA0STE (see Notes 1, 2)  | X                      | 1       | 0      |
|                   |   | S33 (see Note 1)                  | X                      | X       | 1      |
| P7.1/UCA0SIMO/S32 | 1 | P7.1 (I/O)                        | I: 0; O: 1             | 0       | 0      |
|                   |   | USCI_A0.UCA0SIMO (see Notes 1, 2) | X                      | 1       | 0      |
|                   |   | S32 (see Note 1)                  | X                      | X       | 1      |
| P7.2/UCA0SOMI/S31 | 2 | P7.2 (I/O)                        | I: 0; O: 1             | 0       | 0      |
|                   |   | USCI_A0.UCA0SOMI (see Notes 1, 3) | X                      | 1       | 0      |
|                   |   | S31 (see Note 1)                  | X                      | X       | 1      |
| P7.3/UCA0CLK/S30  | 3 | P7.3 (I/O)                        | I: 0; O: 1             | 0       | 0      |
|                   |   | USCI_A0.UCA0CLK (see Notes 1, 3)  | X                      | 1       | 0      |
|                   |   | S30 (see Note 1)                  | X                      | X       | 1      |

NOTES: 1. X: Don't care.  
2. The pin direction is controlled by the USCI module.  
3. The pin direction is controlled by the USCI module.

port P7, P7.4 to P7.7, input/output with Schmitt trigger



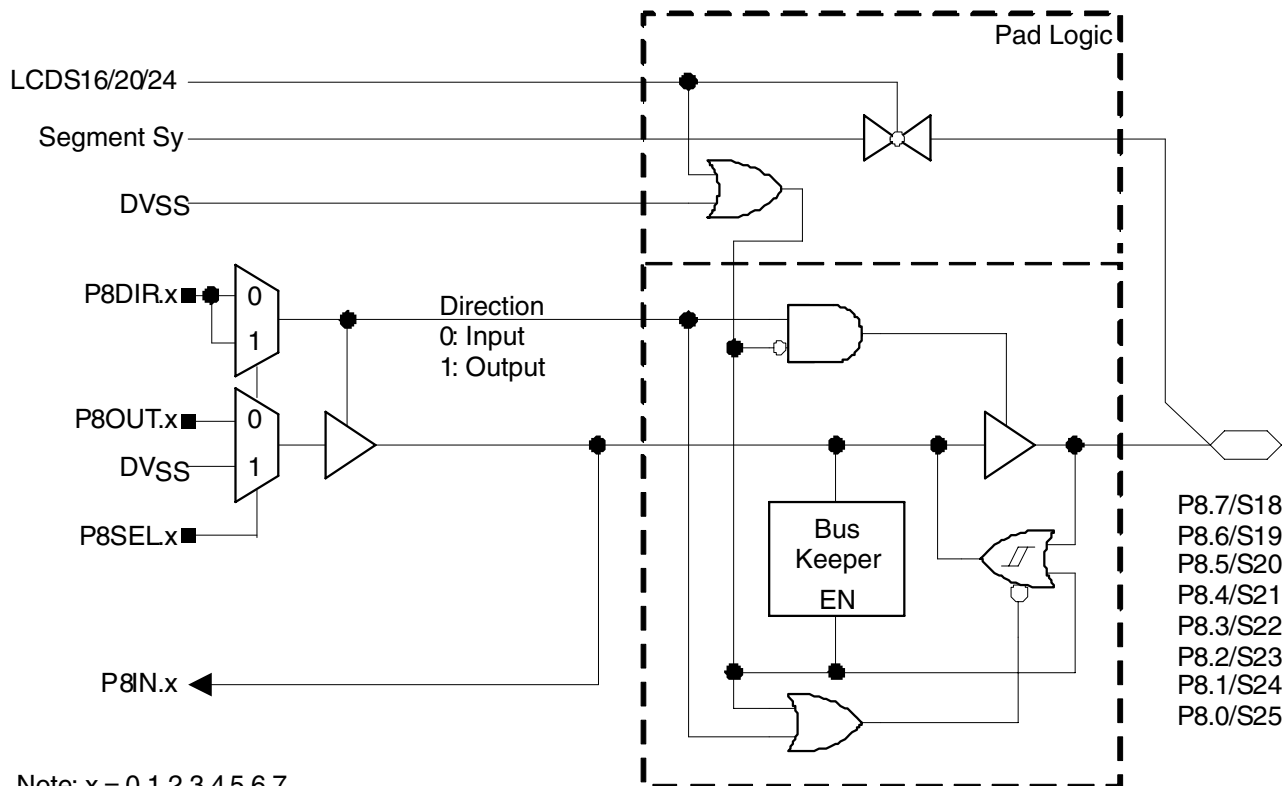
Note: x = 4, 5, 6, 7  
y = 26, 27, 28, 29

port P7 (P7.4 to P7.5) pin functions

| PIN NAME (P7.X) | X | FUNCTION         | CONTROL BITS / SIGNALS |         |        |
|-----------------|---|------------------|------------------------|---------|--------|
|                 |   |                  | P7DIR.x                | P7SEL.x | LCDS28 |
| P7.4/S29        | 4 | P7.4 (I/O)       | I: 0; O: 1             | 0       | 0      |
|                 |   | S29 (see Note 1) | X                      | X       | 1      |
| P7.5/S28        | 5 | P7.5 (I/O)       | I: 0; O: 1             | 0       | 0      |
|                 |   | S28 (see Note 1) | X                      | X       | 1      |
| P7.6/S27        | 6 | P7.6 (I/O)       | I: 0; O: 1             | 0       | 0      |
|                 |   | S27 (see Note 1) | X                      | X       | 1      |
| P7.7/S26        | 7 | P7.7 (I/O)       | I: 0; O: 1             | 0       | 0      |
|                 |   | S26 (see Note 1) | X                      | X       | 1      |

NOTE 1: X: Don't care.

port P8, P8.0 to P8.7, input/output with Schmitt trigger



Note: x = 0,1,2,3,4,5,6,7  
y = 25,24,23,22,21,20,19,18

**port P8 (P8.0 to P8.1) pin functions**

| PIN NAME (P8.X) | X | FUNCTION         | CONTROL BITS / SIGNALS |         |        |
|-----------------|---|------------------|------------------------|---------|--------|
|                 |   |                  | P8DIR.x                | P8SEL.x | LCDS16 |
| P8.0/S18        | 0 | P8.0 (I/O)       | I: 0; O: 1             | 0       | 0      |
|                 |   | S18 (see Note 1) | X                      | X       | 1      |
| P8.1/S19        | 0 | P8.0 (I/O)       | I: 0; O: 1             | 0       | 0      |
|                 |   | S19 (see Note 1) | X                      | X       | 1      |
| P8.2/S20        | 2 | P8.2 (I/O)       | I: 0; O: 1             | 0       | 0      |
|                 |   | S20 (see Note 1) | X                      | X       | 1      |
| P8.3/S21        | 3 | P8.3 (I/O)       | I: 0; O: 1             | 0       | 0      |
|                 |   | S21 (see Note 1) | X                      | X       | 1      |
| P8.4/S22        | 4 | P8.4 (I/O)       | I: 0; O: 1             | 0       | 0      |
|                 |   | S22 (see Note 1) | X                      | X       | 1      |
| P8.5/S23        | 5 | P8.5 (I/O)       | I: 0; O: 1             | 0       | 0      |
|                 |   | S23 (see Note 1) | X                      | X       | 1      |

NOTE 1: X: Don't care.

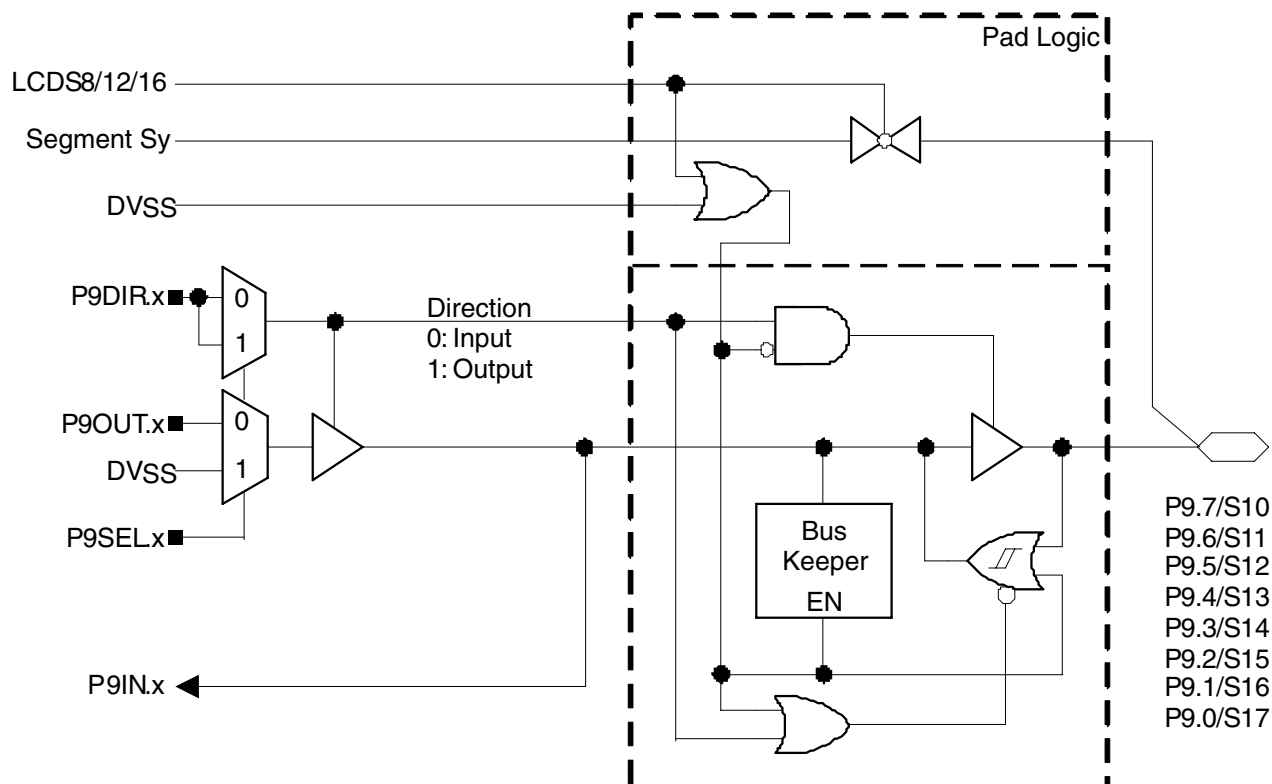
**port P8 (P8.6 to P8.7) pin functions**

| PIN NAME (P8.X) | X | FUNCTION         | CONTROL BITS / SIGNALS |         |        |
|-----------------|---|------------------|------------------------|---------|--------|
|                 |   |                  | P8DIR.x                | P8SEL.x | LCDS24 |
| P8.6/S24        | 6 | P8.6 (I/O)       | I: 0; O: 1             | 0       | 0      |
|                 |   | S24 (see Note 1) | X                      | X       | 1      |
| P8.7/S25        | 7 | P8.7 (I/O)       | I: 0; O: 1             | 0       | 0      |
|                 |   | S25 (see Note 1) | X                      | X       | 1      |

NOTE 1: X: Don't care.

# MSP430x461x1, MSP430x461x MIXED SIGNAL MICROCONTROLLER

port P9, P9.0 to P9.7, input/output with Schmitt trigger



Note: x = 0,1,2,3,4,5,6,7  
y = 17,16,15,14,13,12,11,10

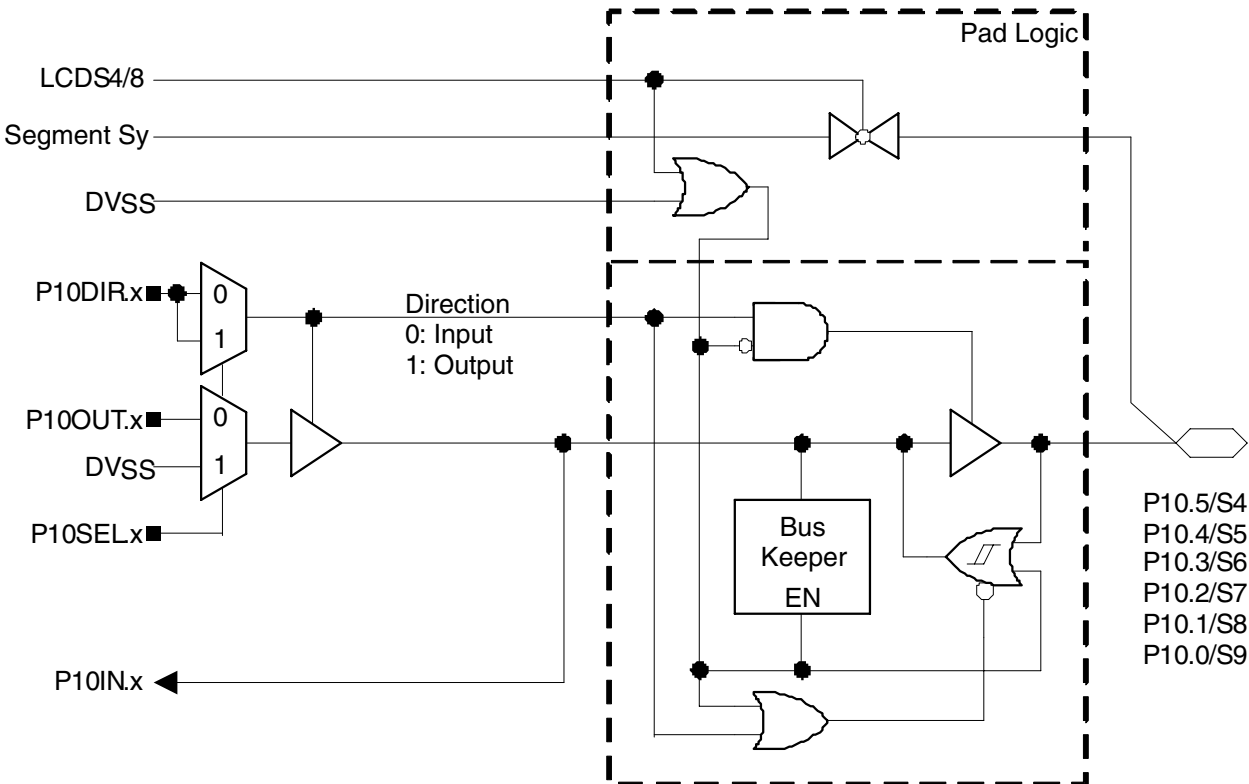
**port P9 (P9.0 to P9.1) pin functions**

| PIN NAME (P9.X) | X | FUNCTION         | CONTROL BITS / SIGNALS |         |        |
|-----------------|---|------------------|------------------------|---------|--------|
|                 |   |                  | P9DIR.x                | P9SEL.x | LCDS16 |
| P9.0/S17        | 0 | P9.0 (I/O)       | I: 0; O: 1             | 0       | 0      |
|                 |   | S17 (see Note 1) | X                      | X       | 1      |
| P9.1/S16        | 1 | P9.1 (I/O)       | I: 0; O: 1             | 0       | 0      |
|                 |   | S16 (see Note 1) | X                      | X       | 1      |
| P9.2/S20        | 2 | P9.2 (I/O)       | I: 0; O: 1             | 0       | 0      |
|                 |   | S15 (see Note 1) | X                      | X       | 1      |
| P9.3/S21        | 3 | P9.3 (I/O)       | I: 0; O: 1             | 0       | 0      |
|                 |   | S14 (see Note 1) | X                      | X       | 1      |
| P9.4/S22        | 4 | P9.4 (I/O)       | I: 0; O: 1             | 0       | 0      |
|                 |   | S13 (see Note 1) | X                      | X       | 1      |
| P9.5/S23        | 5 | P9.5 (I/O)       | I: 0; O: 1             | 0       | 0      |
|                 |   | S12 (see Note 1) | X                      | X       | 1      |
| P9.6/S24        | 6 | P9.6 (I/O)       | I: 0; O: 1             | 0       | 0      |
|                 |   | S11 (see Note 1) | X                      | X       | 1      |
| P9.7/S25        | 7 | P9.7 (I/O)       | I: 0; O: 1             | 0       | 0      |
|                 |   | S10 (see Note 1) | X                      | X       | 1      |

NOTE 1: X: Don't care.

MSP430x461x1, MSP430x461x  
MIXED SIGNAL MICROCONTROLLER

port P10, P10.0 to P10.5, input/output with Schmitt trigger



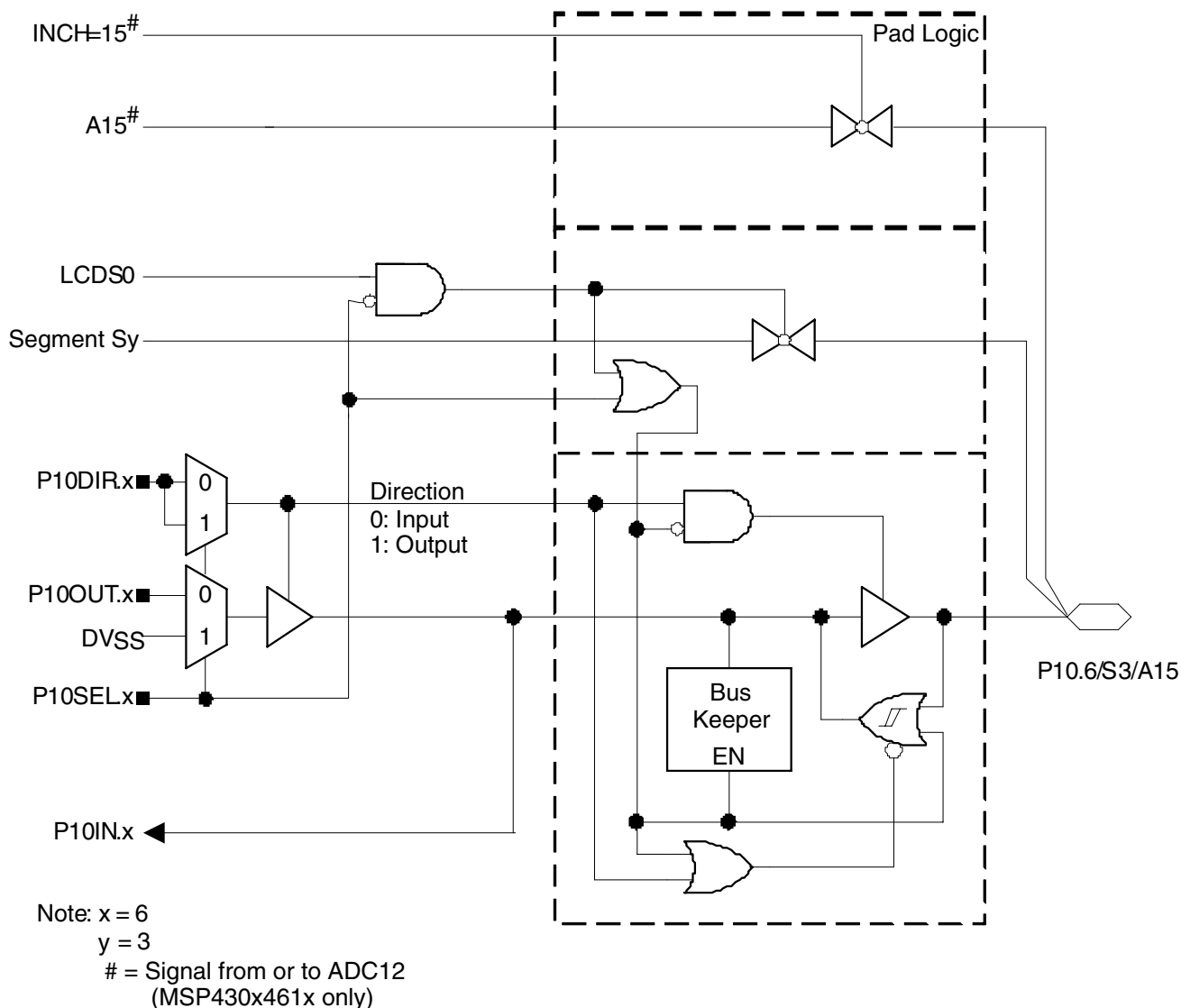
Note: x = 0,1,2,3,4,5  
y = 9,8,7,6,5,4

port P10 (P10.0 to P10.1) pin functions

| PIN NAME (P10.X) | X | FUNCTION        | CONTROL BITS / SIGNALS |          |       |
|------------------|---|-----------------|------------------------|----------|-------|
|                  |   |                 | P10DIR.x               | P10SEL.x | LCDs8 |
| P10.0/S8         | 0 | P10.0 (I/O)     | I: 0; O: 1             | 0        | 0     |
|                  |   | S8 (see Note 1) | X                      | X        | 1     |
| P10.1/S7         | 1 | P10.1 (I/O)     | I: 0; O: 1             | 0        | 0     |
|                  |   | S7 (see Note 1) | X                      | X        | 1     |
| P10.2/S7         | 2 | P10.2 (I/O)     | I: 0; O: 1             | 0        | 0     |
|                  |   | S7 (see Note 1) | X                      | X        | 1     |
| P10.3/S6         | 3 | P10.3 (I/O)     | I: 0; O: 1             | 0        | 0     |
|                  |   | S6 (see Note 1) | X                      | X        | 1     |
| P10.4/S5         | 4 | P10.4 (I/O)     | I: 0; O: 1             | 0        | 0     |
|                  |   | S5 (see Note 1) | X                      | X        | 1     |
| P10.5/S4         | 5 | P10.5 (I/O)     | I: 0; O: 1             | 0        | 0     |
|                  |   | S4 (see Note 1) | X                      | X        | 1     |

NOTE 1: X: Don't care.

port P10, P10.6, input/output with Schmitt trigger



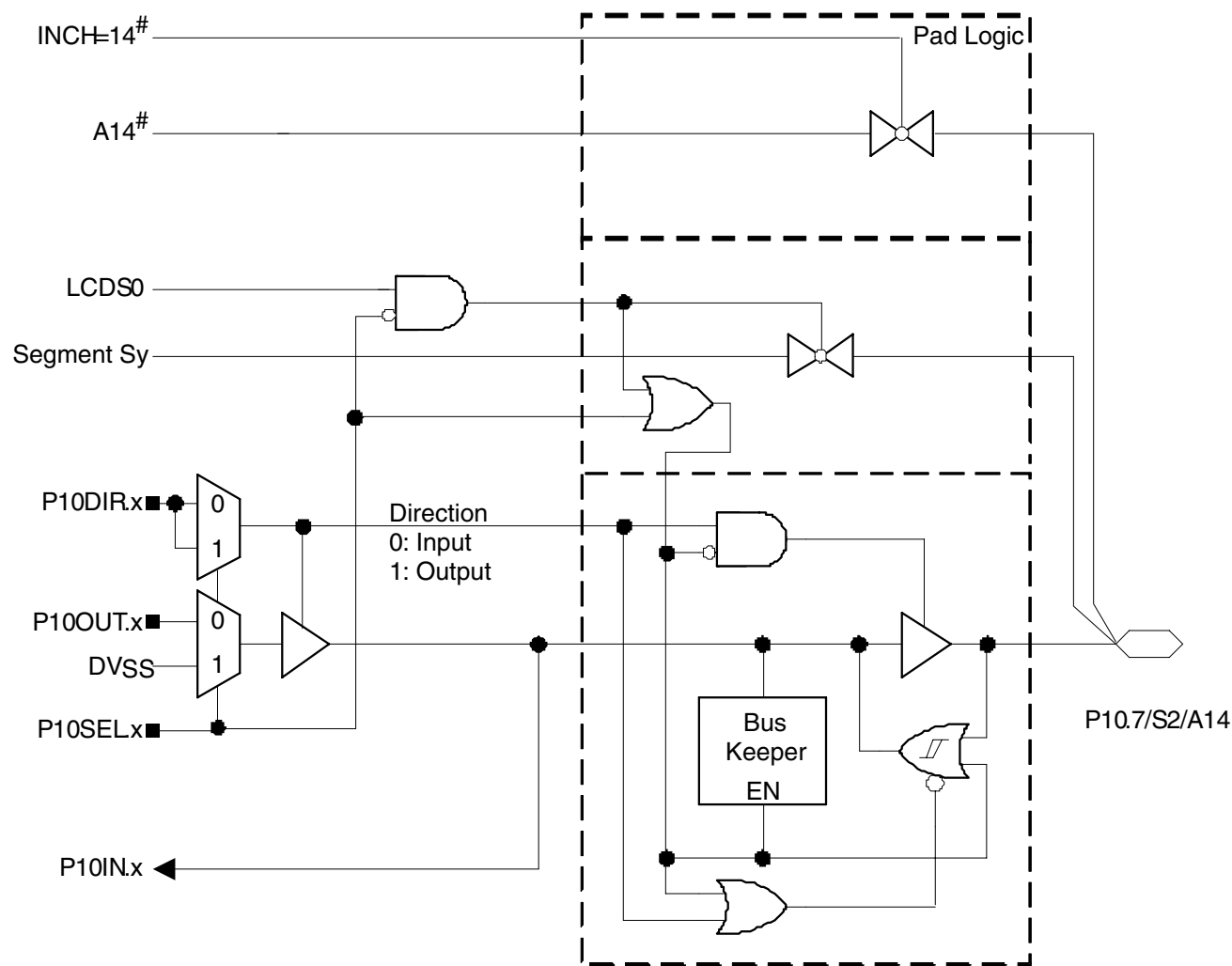
port P10 (P10.6) pin functions

| PIN NAME (P10.X) | X | FUNCTION                               | CONTROL BITS / SIGNALS |          |       |       |
|------------------|---|----------------------------------------|------------------------|----------|-------|-------|
|                  |   |                                        | P10DIR.x               | P10SEL.x | INCHx | LCDS0 |
| P10.6/S3/A15     | 6 | P5.0 (I/O) (see Note 1)                | I: 0; O: 1             | 0        | X     | 0     |
|                  |   | A15 (MSP430x461x only, see Notes 1, 3) | X                      | 1        | 15    | 0     |
|                  |   | S3 enabled (see Note 1)                | X                      | 0        | X     | 1     |
|                  |   | S3 disabled (see Note 1)               | X                      | 1        | X     | 1     |

- NOTES: 1. X: Don't care.  
2. N/A: Not available or not applicable.  
3. Setting the P10SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

MSP430x461x1, MSP430x461x  
MIXED SIGNAL MICROCONTROLLER

port P10, P10.7, input/output with Schmitt trigger



Note: x = 7

y = 2

# = Signal from or to ADC12  
(MSP430x461x only)

port P10 (P10.7) pin functions

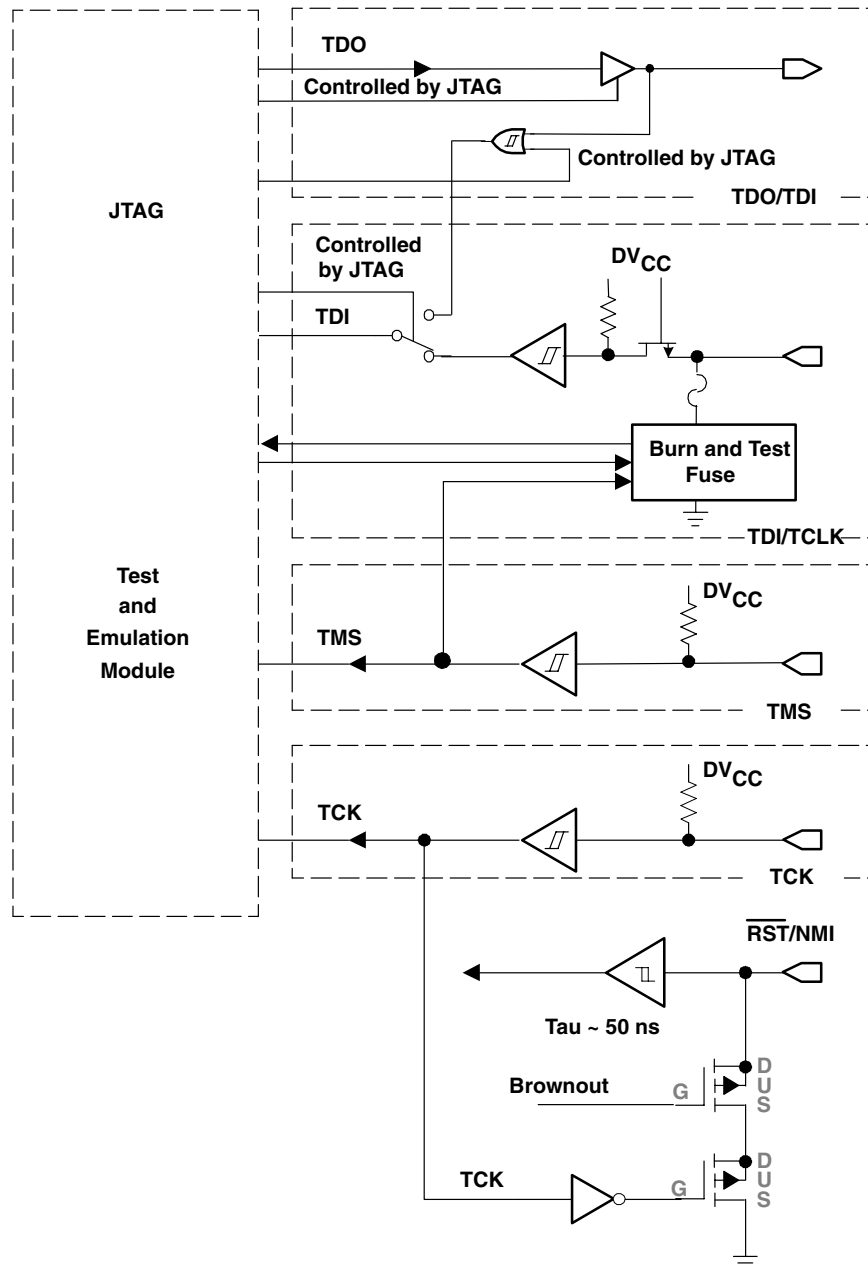
| PIN NAME (P10.X) | X | FUNCTION                               | CONTROL BITS / SIGNALS |          |       |       |
|------------------|---|----------------------------------------|------------------------|----------|-------|-------|
|                  |   |                                        | P10DIR.x               | P10SEL.x | INCHx | LCDS0 |
| P10.7/S2/A14     | 7 | P10.7 (I/O) (see Note 1)               | I: 0; O: 1             | 0        | X     | 0     |
|                  |   | A14 (MSP430x461x only, see Notes 1, 3) | X                      | 1        | 14    | 0     |
|                  |   | S2 enabled (see Note 1)                | X                      | 0        | X     | 1     |
|                  |   | S2 disabled (see Note 1)               | X                      | 1        | X     | 1     |

NOTES: 1. X: Don't care.

2. N/A: Not available or not applicable.

3. Setting the P10SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

JTAG pins TMS, TCK, TDI/TCLK, TDO/TDI, input/output with Schmitt-trigger or output



## **JTAG fuse check mode**

MSP430 devices that have the fuse on the TDI/TCLK terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current ( $I_{(TF)}$ ) of 1 mA at 3 V can flow from the TDI/TCLK pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current only flows when the fuse check mode is active and the TMS pin is in a low state (see Figure 26). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition). The JTAG pins are terminated internally and therefore do not require external termination.

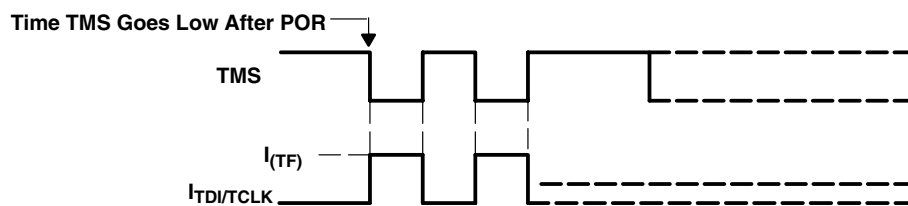


**Figure 26. Fuse Check Mode Current**

---

**Data Sheet Revision History**

| <b>Literature<br/>Number</b> | <b>Summary</b>                     |
|------------------------------|------------------------------------|
| SLAS675                      | Production Data data sheet release |

NOTE: Page and figure numbers refer to the respective document revision.

# **Corrections to MSP430F461x, MSP430F461x1 Data Sheet (SLAS675)**

Document Being Updated: *MSP430F461x, MSP430F461x1 Mixed Signal Microcontroller*

Literature Number Being Updated: SLAS675

## **Page Change or Add**

- 68 The table includes *LCDS36* in the "CONTROL BITS / SIGNALS" column. This is correct for P4.2/STE1/S39, P4.3/SIMO/S38, P4.4/SOMI/S37, and P4.5/SOMI/S36.  
For P4.6/UCA0TXD/S35 and P4.7/UCA0RXD/S34, the correct control bit is **LCDS32**.
- 78 The table includes *LCDS32* in the "CONTROL BITS / SIGNALS" column. This is correct for P7.0/UCA0STE/S33 and P7.1/UCA0SIMO/S32.  
For P7.2/UCA0SOMI/S31 and P7.3/UCA0CLK/S30, the correct control bit is **LCDS28**.
- 79 The table includes *LCDS28* in the "CONTROL BITS / SIGNALS" column. This is correct for P7.4/S29 and P7.5/S28.  
For P7.6/S27 and P7.7/S26, the correct control bit is **LCDS24**.
- 81 The "port P8 (P8.0 to P8.1) pin functions" table includes *LCDS16* in the "CONTROL BITS / SIGNALS" column. This is correct for P8.0/S18 and P8.1/S19.  
For P8.2/S20, P8.3/S21, P8.4/S22, and P8.5/S23, the correct control bit is **LCDS20**.
- 83 In the "PIN NAME (P9.X)" column, the segment signal names on P9.2 through P9.7 are incorrect—they should be:  
**P9.2/S15**  
**P9.3/S14**  
**P9.4/S13**  
**P9.5/S12**  
**P9.6/S11**  
**P9.7/S10**  
The table includes *LCDS16* in the "CONTROL BITS / SIGNALS" column. This is correct for P9.0/S17 and P9.1/S16.  
For P9.2/S15, P9.3/S14, P9.4/S13, and P9.5/S12, the correct control bit is **LCDS12**.  
For P9.6/S11 and P9.7/S10, the correct control bit is **LCDS8**.
- 84 In the "PIN NAME (P10.X)" and "FUNCTION" columns, the segment signal names on P10.0 and P10.1 are incorrect—they should be changed to:  
**P10.0/S9**  
**P10.1/S8**  
The table includes *LCDS8* in the "CONTROL BITS / SIGNALS" column. This is correct for P10.0/S9 and P10.1/S8.  
For P10.2/S7, P10.3/S6, P10.4/S5, and P10.5/S4, the correct control bit is **LCDS4**.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP430F46161IPZ  | ACTIVE        | LQFP         | PZ                 | 100  | 90             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-3-260C-168 HR  | -40 to 85    | M430F46161              | <a href="#">Samples</a> |
| MSP430F46161IPZR | ACTIVE        | LQFP         | PZ                 | 100  | 1000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-3-260C-168 HR  | -40 to 85    | M430F46161              | <a href="#">Samples</a> |
| MSP430F4616IPZ   | ACTIVE        | LQFP         | PZ                 | 100  | 90             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-3-260C-168 HR  | -40 to 85    | M430F4616               | <a href="#">Samples</a> |
| MSP430F4616IPZR  | ACTIVE        | LQFP         | PZ                 | 100  | 1000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-3-260C-168 HR  | -40 to 85    | M430F4616               | <a href="#">Samples</a> |
| MSP430F46171IPZ  | ACTIVE        | LQFP         | PZ                 | 100  | 90             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-3-260C-168 HR  | -40 to 85    | M430F46171              | <a href="#">Samples</a> |
| MSP430F46171IPZR | ACTIVE        | LQFP         | PZ                 | 100  | 1000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-3-260C-168 HR  | -40 to 85    | M430F46171              | <a href="#">Samples</a> |
| MSP430F4617IPZ   | ACTIVE        | LQFP         | PZ                 | 100  | 90             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-3-260C-168 HR  | -40 to 85    | M430F4617               | <a href="#">Samples</a> |
| MSP430F4617IPZR  | ACTIVE        | LQFP         | PZ                 | 100  | 1000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-3-260C-168 HR  | -40 to 85    | M430F4617               | <a href="#">Samples</a> |
| MSP430F46181IPZ  | ACTIVE        | LQFP         | PZ                 | 100  | 90             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-3-260C-168 HR  | -40 to 85    | M430F46181              | <a href="#">Samples</a> |
| MSP430F46181IPZR | ACTIVE        | LQFP         | PZ                 | 100  | 1000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-3-260C-168 HR  | -40 to 85    | M430F46181              | <a href="#">Samples</a> |
| MSP430F4618IPZ   | ACTIVE        | LQFP         | PZ                 | 100  | 90             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-3-260C-168 HR  | -40 to 85    | M430F4618               | <a href="#">Samples</a> |
| MSP430F4618IPZR  | ACTIVE        | LQFP         | PZ                 | 100  | 1000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-3-260C-168 HR  | -40 to 85    | M430F4618               | <a href="#">Samples</a> |
| MSP430F46191IPZ  | ACTIVE        | LQFP         | PZ                 | 100  | 90             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-3-260C-168 HR  | -40 to 85    | M430F46191              | <a href="#">Samples</a> |
| MSP430F46191IPZR | ACTIVE        | LQFP         | PZ                 | 100  | 1000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-3-260C-168 HR  | -40 to 85    | M430F46191              | <a href="#">Samples</a> |
| MSP430F4619IPZ   | ACTIVE        | LQFP         | PZ                 | 100  | 90             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-3-260C-168 HR  | -40 to 85    | M430F4619               | <a href="#">Samples</a> |
| MSP430F4619IPZR  | ACTIVE        | LQFP         | PZ                 | 100  | 1000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-3-260C-168 HR  | -40 to 85    | M430F4619               | <a href="#">Samples</a> |

<sup>(1)</sup> The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

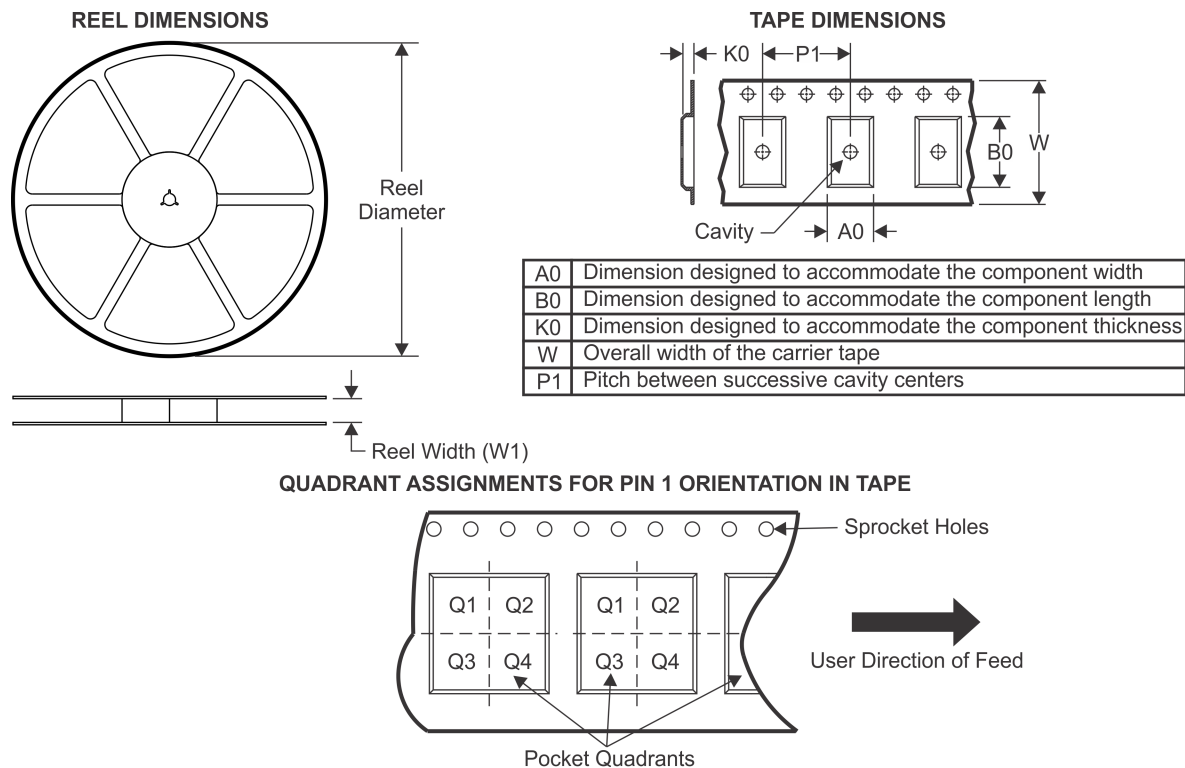
<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

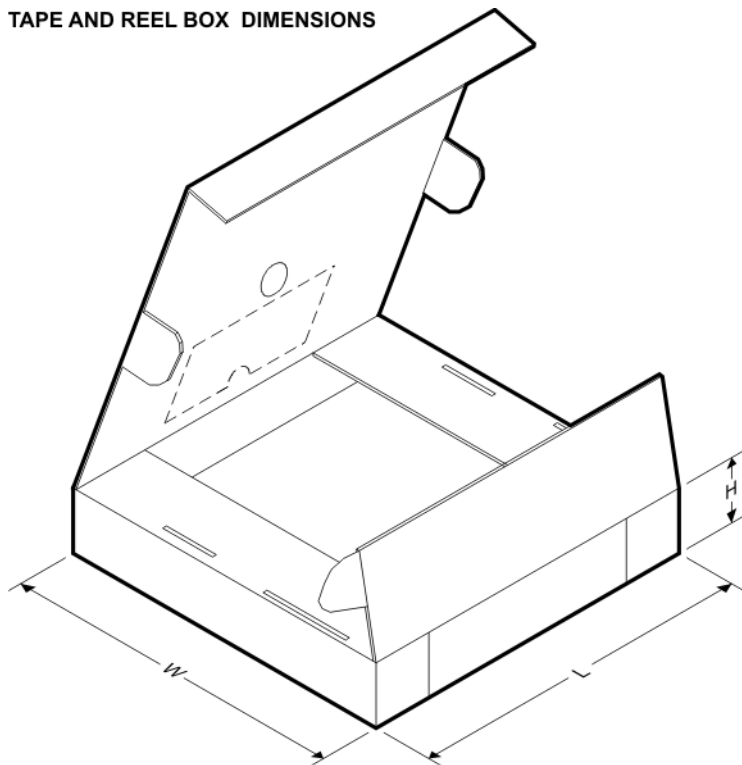
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430F46161IPZR | LQFP         | PZ              | 100  | 1000 | 330.0              | 24.4               | 17.0    | 17.0    | 2.1     | 20.0    | 24.0   | Q2            |
| MSP430F4616IPZR  | LQFP         | PZ              | 100  | 1000 | 330.0              | 24.4               | 17.0    | 17.0    | 2.1     | 20.0    | 24.0   | Q2            |
| MSP430F46171IPZR | LQFP         | PZ              | 100  | 1000 | 330.0              | 24.4               | 17.0    | 17.0    | 2.1     | 20.0    | 24.0   | Q2            |
| MSP430F4617IPZR  | LQFP         | PZ              | 100  | 1000 | 330.0              | 24.4               | 17.0    | 17.0    | 2.1     | 20.0    | 24.0   | Q2            |
| MSP430F46181IPZR | LQFP         | PZ              | 100  | 1000 | 330.0              | 24.4               | 17.0    | 17.0    | 2.1     | 20.0    | 24.0   | Q2            |
| MSP430F4618IPZR  | LQFP         | PZ              | 100  | 1000 | 330.0              | 24.4               | 17.0    | 17.0    | 2.1     | 20.0    | 24.0   | Q2            |
| MSP430F46191IPZR | LQFP         | PZ              | 100  | 1000 | 330.0              | 24.4               | 17.0    | 17.0    | 2.1     | 20.0    | 24.0   | Q2            |
| MSP430F4619IPZR  | LQFP         | PZ              | 100  | 1000 | 330.0              | 24.4               | 17.0    | 17.0    | 2.1     | 20.0    | 24.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS

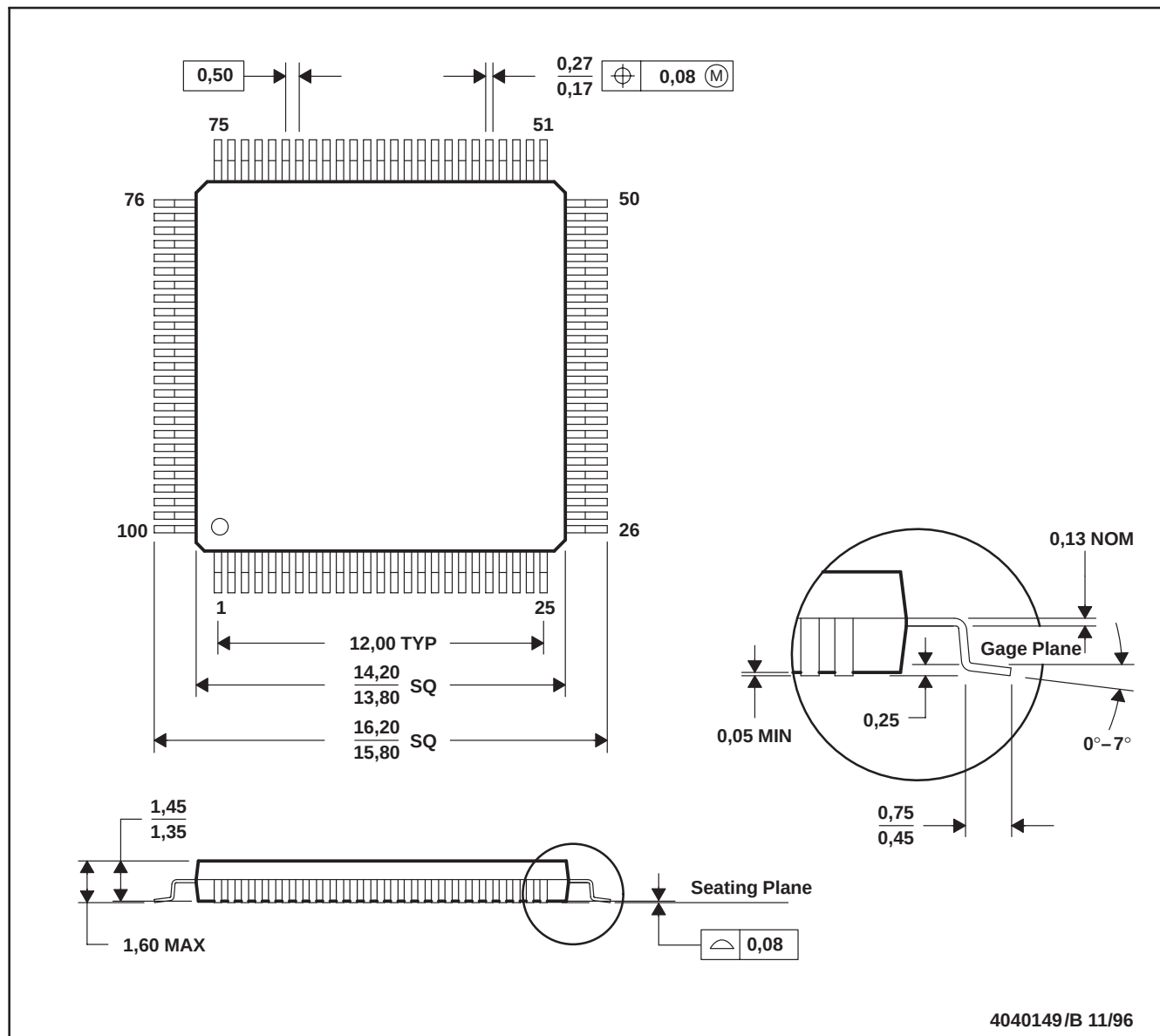


\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSP430F46161IPZR | LQFP         | PZ              | 100  | 1000 | 367.0       | 367.0      | 45.0        |
| MSP430F4616IPZR  | LQFP         | PZ              | 100  | 1000 | 367.0       | 367.0      | 45.0        |
| MSP430F46171IPZR | LQFP         | PZ              | 100  | 1000 | 367.0       | 367.0      | 45.0        |
| MSP430F4617IPZR  | LQFP         | PZ              | 100  | 1000 | 367.0       | 367.0      | 45.0        |
| MSP430F46181IPZR | LQFP         | PZ              | 100  | 1000 | 367.0       | 367.0      | 45.0        |
| MSP430F4618IPZR  | LQFP         | PZ              | 100  | 1000 | 367.0       | 367.0      | 45.0        |
| MSP430F46191IPZR | LQFP         | PZ              | 100  | 1000 | 367.0       | 367.0      | 45.0        |
| MSP430F4619IPZR  | LQFP         | PZ              | 100  | 1000 | 367.0       | 367.0      | 45.0        |

## PZ (S-PQFP-G100)

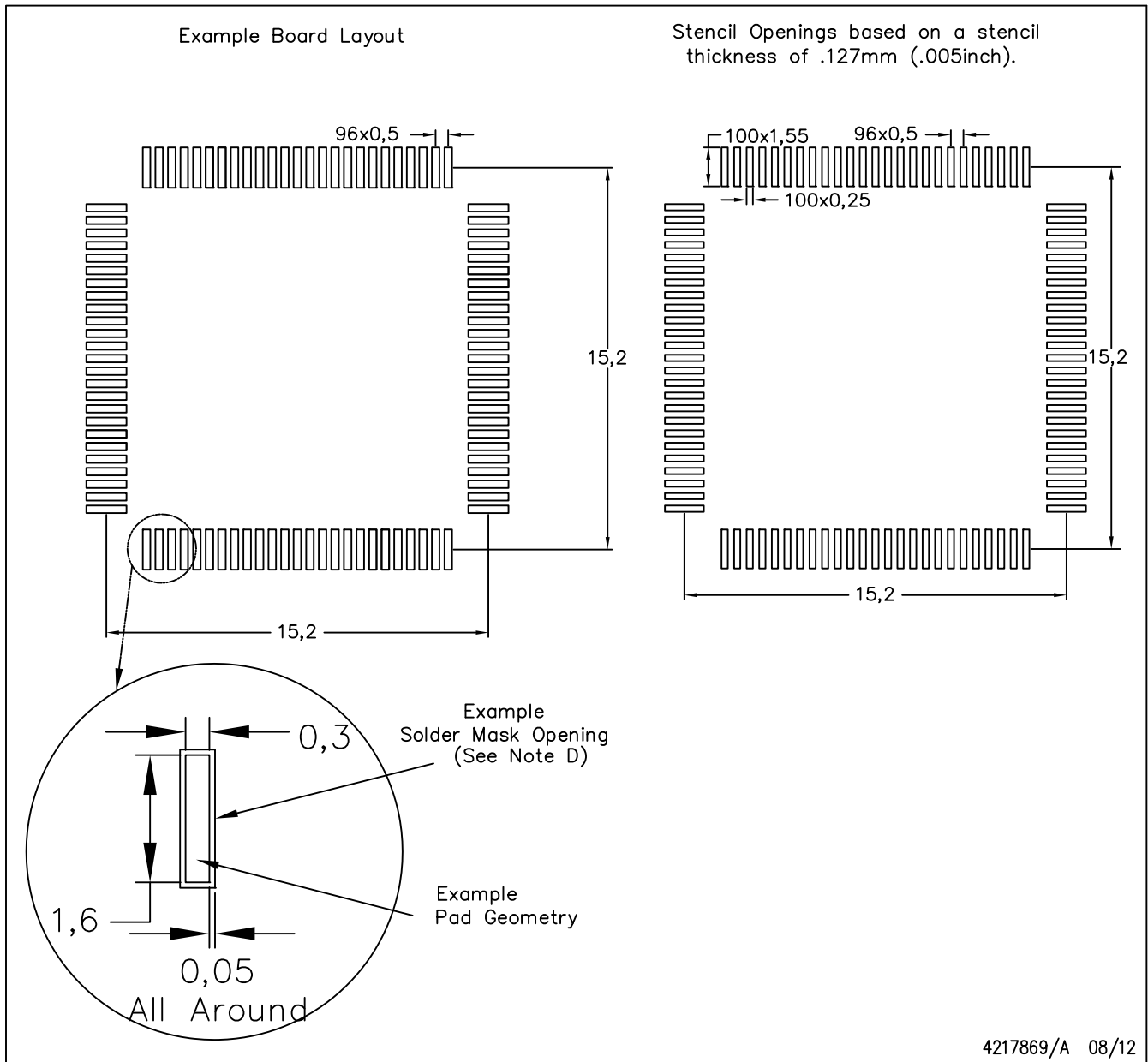
## PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-026

PZ (S-PQFP-G100)

PLASTIC QUAD FLAT PACK



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2020, Texas Instruments Incorporated