A product Line of
Diodes Incorporated

PI3PCIE3412A

3.3V, PCI Express® 3.0 2-Lane, 2:1 Mux/DeMux Switch, with Single Enable

Features

- 4 Differential Channel, 2:1 Mux/DeMux
- PCI Express® 3.0 Performance, 8.0Gbps
- Bi-directional Operation
- Low Bit-to-Bit Skew, 10ps max
- Low channel-to-channel skew, 20ps max
- Low Crosstalk: -35dB@4 GHz
- High Off Isolation: -22dB@4 GHz (8.0Gbps)
- Low insertion loss: -1.3dB@4 GHz (8.0Gbps)
- Return loss: -21dB@4 GHz
- ESD:1.5KV HBM
- Support for DP1.2 - HBR2, HBR, RBR
- Supply Voltage 3.3V
- Industrial Temperature Range: -40°C to 85°C
- Packaging (Pb-free & Green):
  - 42-contact, TQFN (ZH42), 3.5 x 9mm
  - 40-contact, TQFN (ZL40), 3 x 6mm

Description

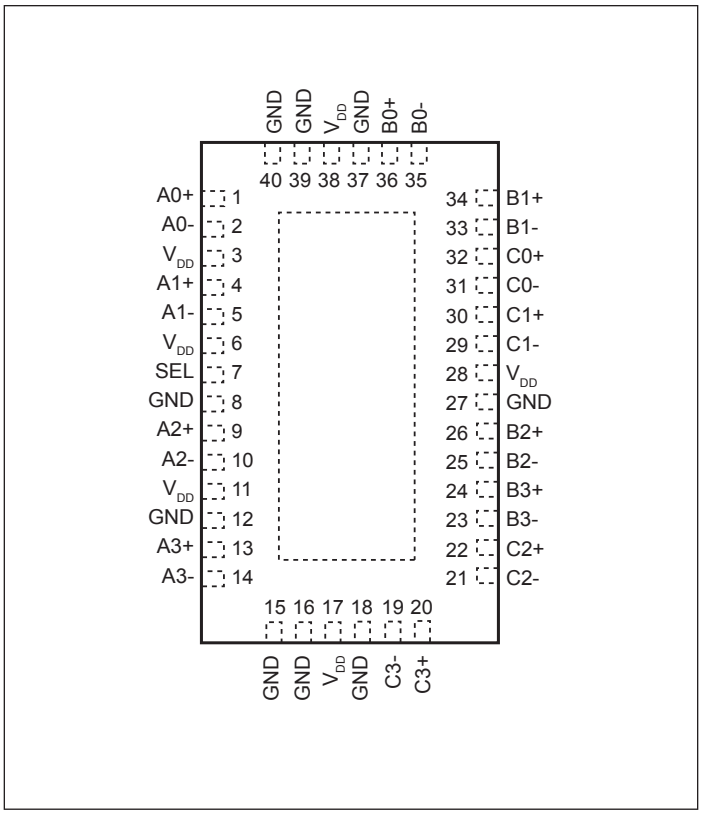
The PI3PCIE3412A is an 8 to 4 differential channel multiplexer/demultiplexer switch. This solution can switch 2 full PCI Express® 3.0, lanes to one of two locations. Using a unique design technique, Diodes Incorporated has been able to minimize the impedance of the switch such that the attenuation observed through the switch is minimal. The unique design technique also offers a layout targeted for PCI Express signals, which minimizes the channel to channel skew as well as channel to channel crosstalk as required by the PCI Express specification.

The PI3PCIE3412A can also be used for application up to 12Gbps.

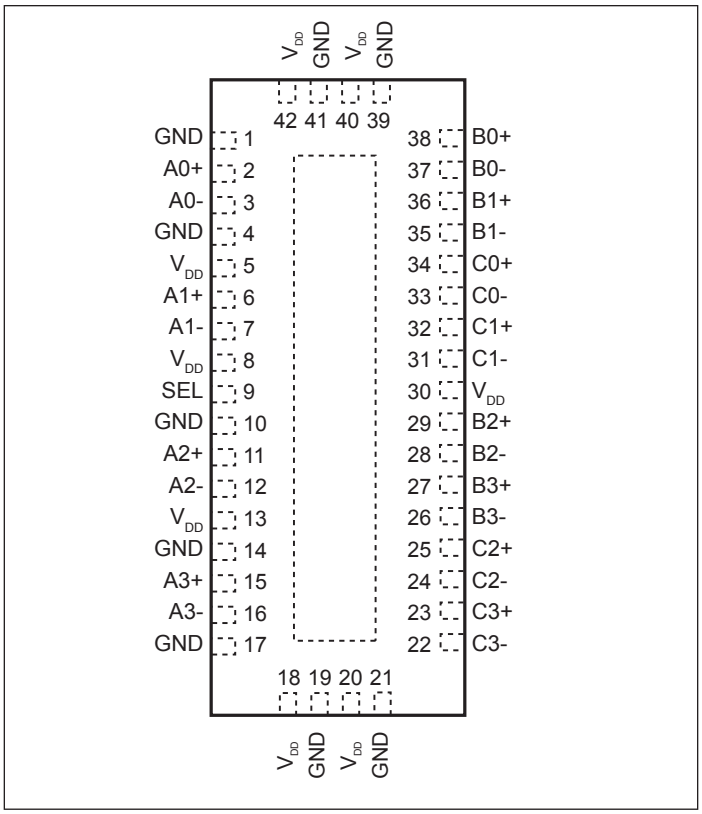
Application

Routing of PCI Express 3.0, DP1.2, USB3.0, SAS2.0, SATA3.0, XAUI, RXAUI signals with low signal attenuation.

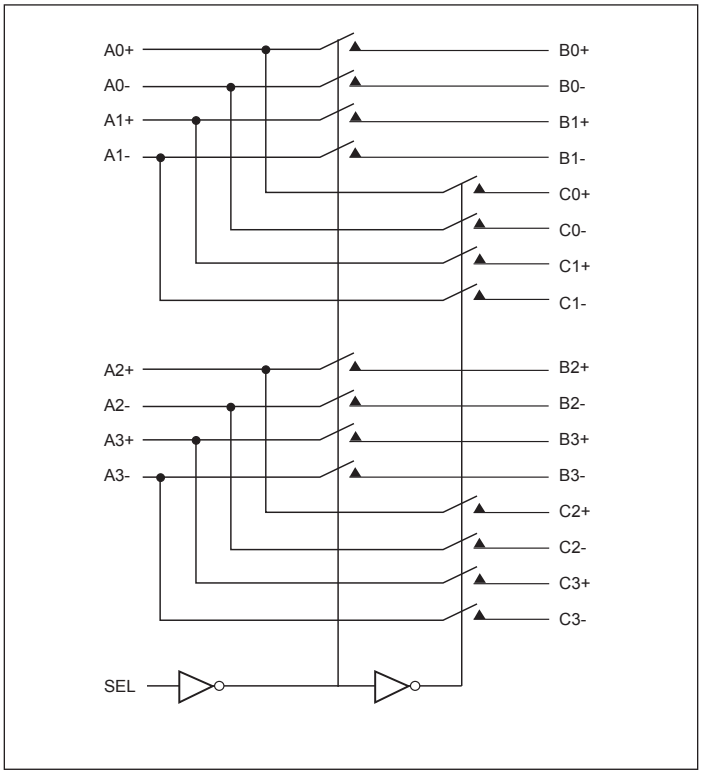
Pin Configuration 40-Contact TQFN



Pin Configuration 42-Contact TQFN



Block Diagram



Truth Table

Function	SEL
A_N to B_N	L
A_N to C_N	H

Pin Description

Pin #		Pin Name	I/O	Description
42-TQFN	40-TQFN			
2 3	1 2	A0+ A0–	I/O	Signal I/O, Channel 0, Port A
6 7	4 5	A1+ A1–	I/O	Signal I/O, Channel 1, Port A
11 12	9 10	A2+ A2–	I/O	Signal I/O, Channel 2, Port A
15 16	13 14	A3+ A3–	I/O	Signal I/O, Channel 3, Port A
38 37	36 35	B0+ B0–	I/O	Signal I/O, Channel 0, Port B
36 35	34 33	B1+ B1–	I/O	Signal I/O, Channel 1, Port B
29 28	26 25	B2+ B2–	I/O	Signal I/O, Channel 2, Port B
27 26	24 23	B3+ B3–	I/O	Signal I/O, Channel 3, Port B
34 33	32 31	C0+ C0–	I/O	Signal I/O, Channel 0, Port C
32 31	30 29	C1+ C1–	I/O	Signal I/O, Channel 1, Port C
25 24	22 21	C2+ C2–	I/O	Signal I/O, Channel 2, Port C
23 22	20 19	C3+ C3–	I/O	Signal I/O, Channel 3, Port C
9	7	SEL	I	Operation mode Select (when SEL=0: A→B, when SEL=1: A→C
5, 8, 13,18, 20, 30, 40, 42	3, 6, 11, 17, 28, 38	V_{DD}	Pwr	3.3V ±10% Positive Supply Voltage
1, 4, 10, 14, 17, 19, 21, 39, 41, Center Pad	8, 12, 15, 16, 18, 27, 37, 39, 40	GND	Pwr	Power ground

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +3.7V
Channel DC Input Voltage	–0.5V to 1.5V
DC Output Current	120mA
Power Dissipation	0.5W
SEL DC Input Voltage	–0.5V to 3.7V
Junction Temperature	125°C

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	3.3V Power Supply		3.0	3.3	3.6	V
I_{DD}	Total current from V_{DD} 3.3V supply	SEL = 0V or V_{DD}		0.15	1	mA
$V_{I/O}$-DIF	Differential Voltage (differential pins)				1.6	V_{ppd}
$V_{I/O-CM}$	Common Mode Voltage (differiential pins)		0		0.8	V
T_A	Operating temperature range		-40		85	°C

DC Electrical Characteristics for Switching over Operating Range

Parameters	Description	Test Conditions(1)	Min.	Typ.(1)	Max.	Units
V_{IH} - SEL	Input HIGH Voltage, SEL Input		2		3.6	V
V_{IL} - SEL	Input LOW Voltage, SEL Input		0		0.8	
V_{IK}	Clamp Diode Voltage	V_{DD} = Max., I_{IN} = –18mA		–0.7	–1.2	
IIH	Input HIGH Current, SEL	V_{DD} = Max., V_{IN} = V_{DD}			±5	µA
I_{IL}	Input LOW Current, SEL	V_{DD} = Max., V_{IN} = 0V			±5	
I_{IN} - SEL	Input Leakage Current, SEL Input	V_{IN} = V_{IH} - SEL Max or V_{IL} - SEL Min	–10		+10	µA
IIH	Input HIGH Current, A_X, B_X, C_X	V_{DD} = Max., V_{IN} = 1.5V	–10		+10	µA
I_{IL}	Input LOW Current, A_X, B_X, C_X	V_{DD} = Max., V_{IN} = 0V	–10		+10	
I_{OZH}	HighZ HIGH Current, B_X, C_X	V_{DD} = Max., V_{IN} = 1.5V	–10		+10	µA
I_{OZL}	HighZ LOW Current, B_X, C_X	V_{DD} = Max., V_{IN} = 0V	–10		+10	µA
$C_{I/O-ON}$	ON state I/O capacitance			1.5		pF
R_{ON}	ON state resistance	V_{DD} = 3.3V, IO = 8mA, V_{IN} = 0.8V		5		Ω

Note:
1. Typical values are at V_{DD} = 3.3V, T_A = 25°C ambient and maximum loading.

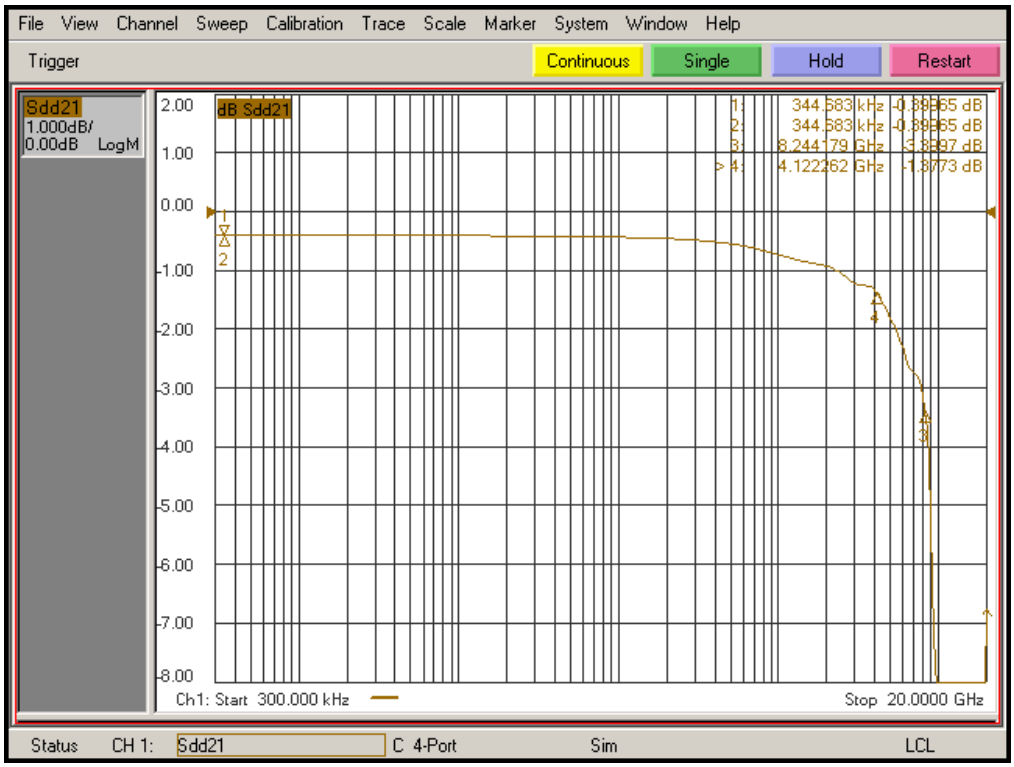
Switching Characteristics

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PZH}, t_{PZL}	Line Enable Time - SEL to A_N, B_N, C_N		2	20	25	ns
t_{PHZ}, t_{PLZ}	Line Disable Time - SEL to A_N, B_N, C_N		0.5	5	25	
t_{b-b}	Bit-to-bit skew within the same differential pair			5	10	ps
t_{ch-ch}	Channel-to-channel skew				20	ps

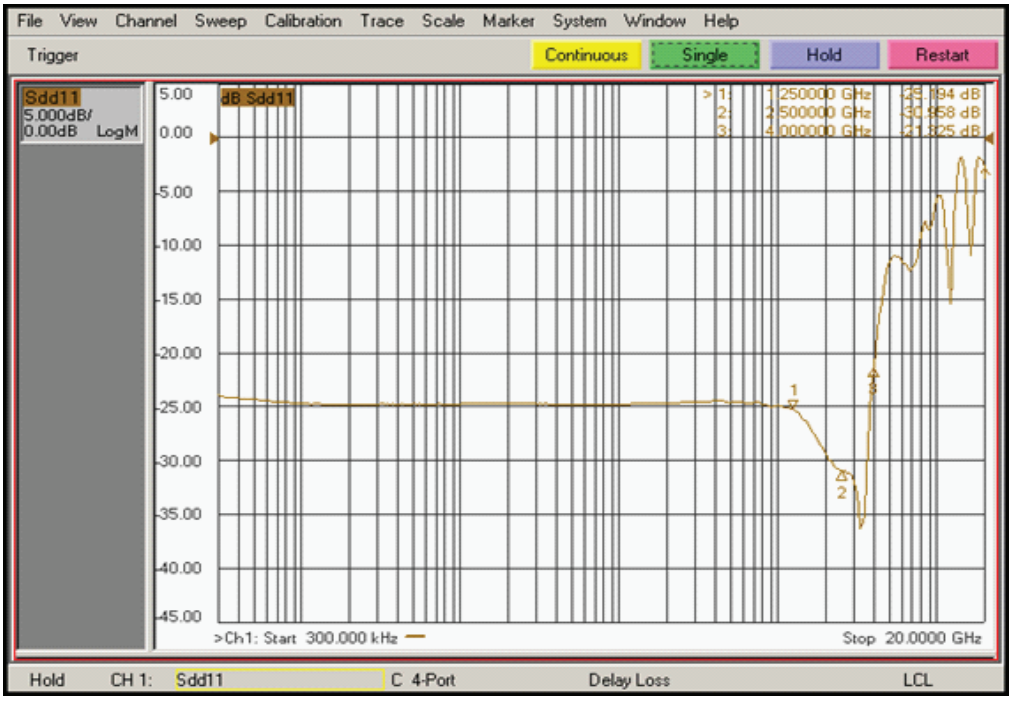
Dynamic Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Typ.(1)	Max.	Units
DDIL	Differential Insertion Loss (V_{IN} = -10dBm, DC = 0V)	f= 50MHz - 1.25GHz		-0.8	-1	dB
		f=1.25GHz - 2.5GHz		-1.0	-1.2	
		f=2.5GHz - 4GHz		-1.3	-1.6	
		f=5GHz		-1.8	-2.2	
$DDIL_{OFF}$	Differential Off Isolation	f= 50MHz - 1.25GHz	-26.3	-32.9		dB
		f=1.25GHz - 2.5GHz	-21.4	-26.7		
		f=2.5GHz - 4GHz	-17.6	-22		
		f=5GHz	-16	-20		
DDRL	Differential Return Loss	f= 50MHz - 1.25GHz	-20	-25		dB
		f=1.25GHz - 2.5GHz	-18.4	-23		
		f=2.5GHz - 4GHz	-16.8	-21		
		f=5GHz	-9.6	-12		
DDNEXT	Near End Crosstalk	f= 50MHz - 1.25GHz	-34.1	-42.6		dB
		f=1.25GHz - 2.5GHz	-30.5	-38.1		
		f=2.5GHz - 4GHz	-28.1	-35.1		
		f=5GHz	-27.2	-34		
V_{IF}	Max Signal Frequency Range	Insertion loss 1.5dB, V_{IN}=0.623Vpp, DC=0V		4.0		GHz
		Insertion loss 1.5dB, V_{IN}=0.623Vpp, DC=0.9V		4.0		
		Insertion loss 3dB, V_{IN}=0.623Vpp, DC=0V		8.0		
		Insertion loss 3dB, V_{IN}=0.623Vpp, DC=0.9V		8.0		
BW	-3dB Bandwidth			8.2		GHz

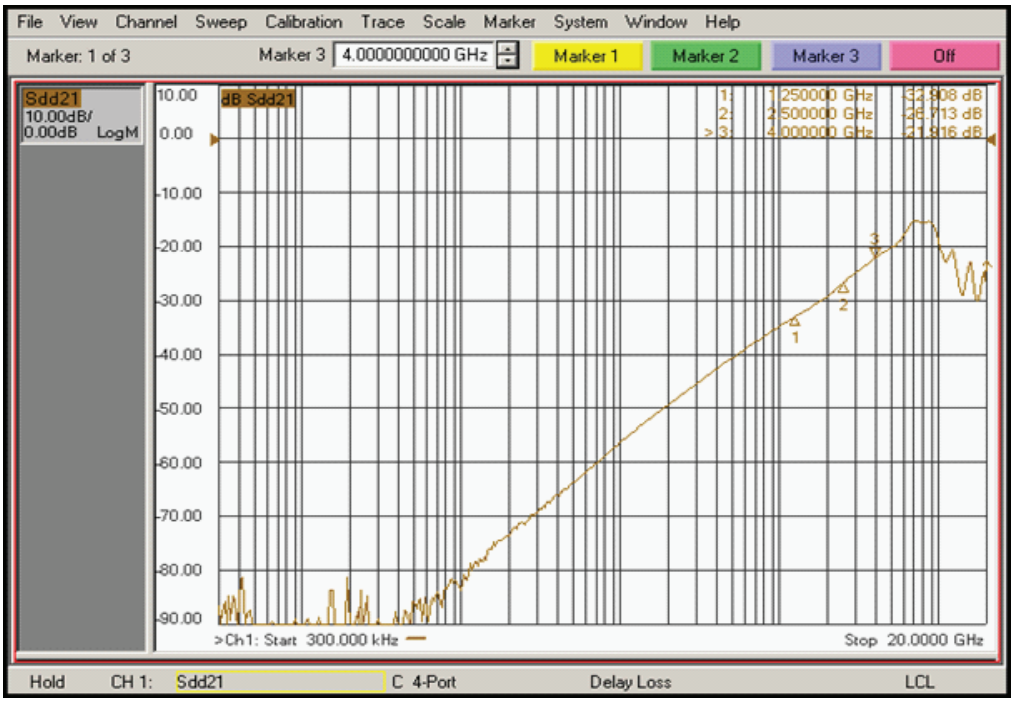
Notes:
1. Guaranteed by design. Typical values are at V_{DD} = 3.3V , T_A = 25°C ambient and maximum loading.



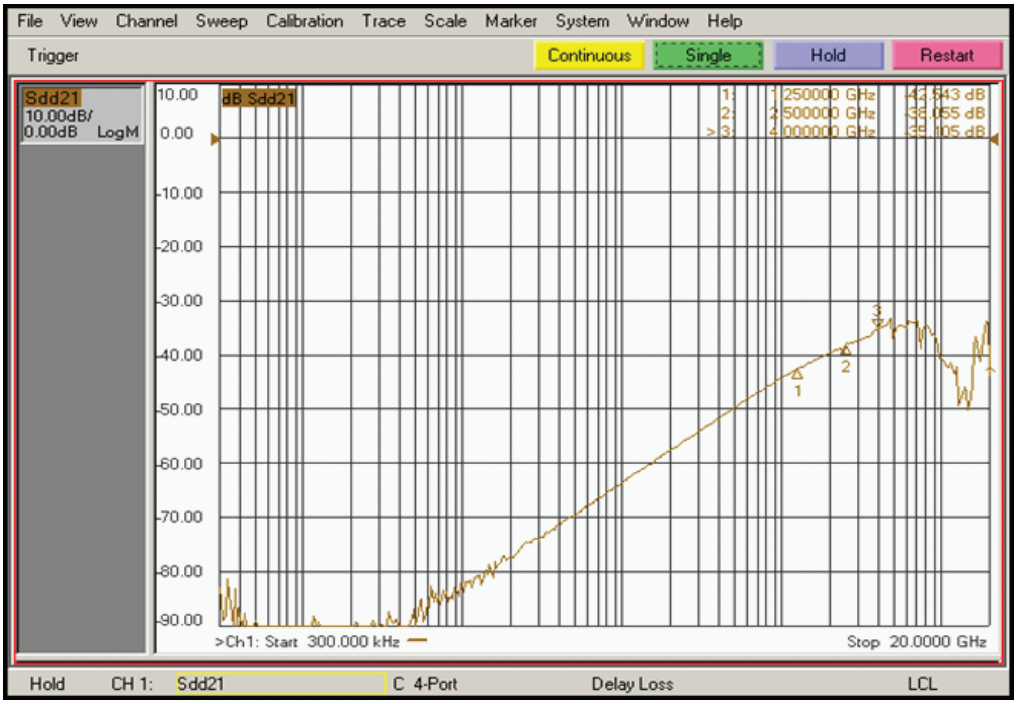
Differential Insertion Loss



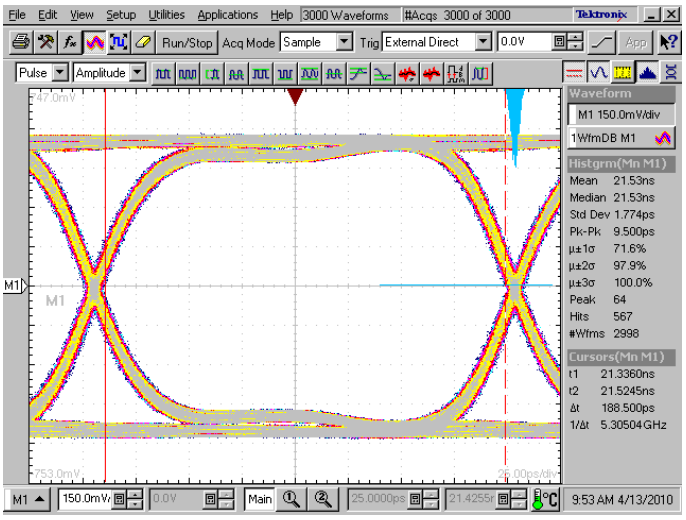
Differential Return Loss



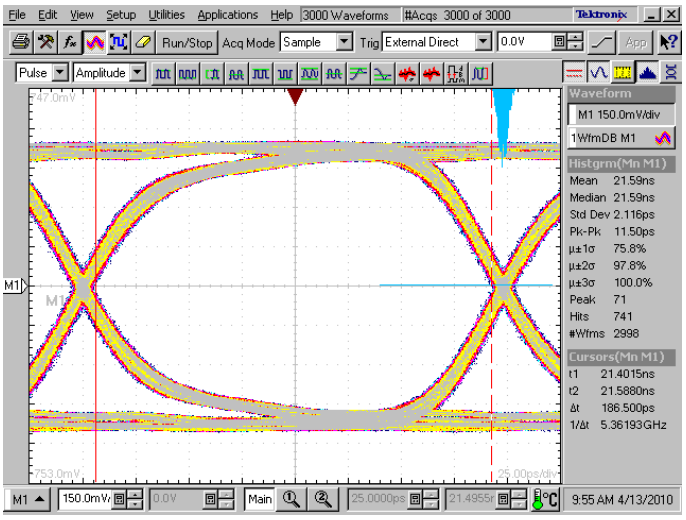
Differential Off Isolation



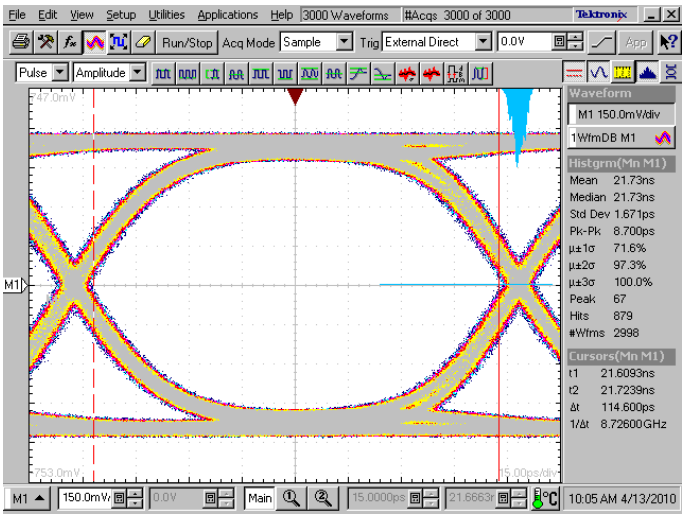
Differential Crosstalk



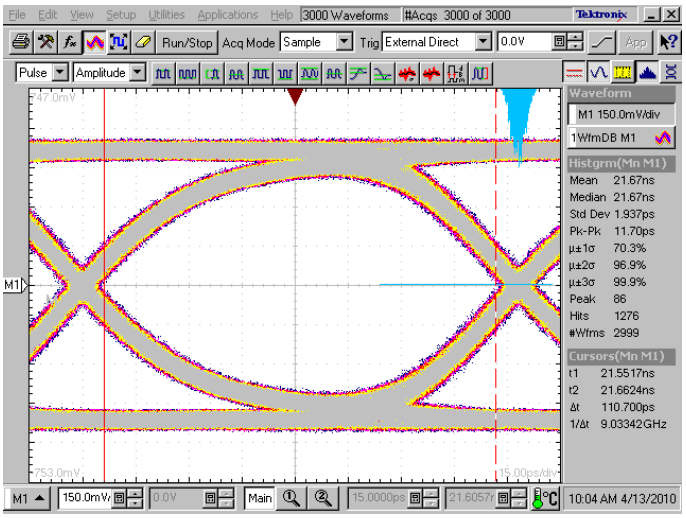
5.0 Gbps RX signal eye without PI3PCIE3412A



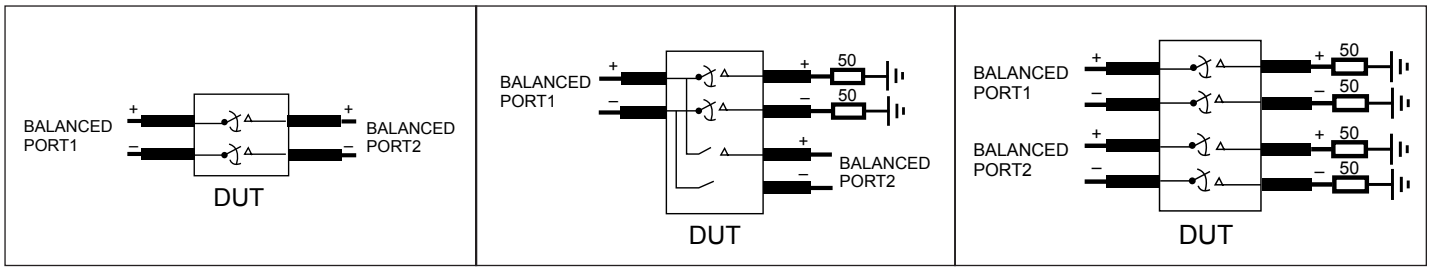
5.0 Gbps RX signal eye with PI3PCIE3412A



8.0 Gbps RX signal eye without PI3PCIE3412A



8.0 Gbps RX signal eye with PI3PCIE3412A

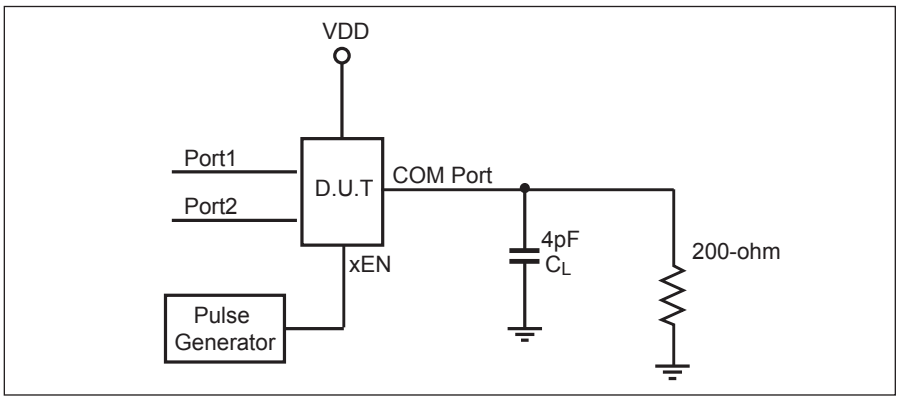


Diff. Insertion Loss and Return Test Circuit

Diff. Off Isolation Test Circuit

Diff. Near End Xtalk Test Circuit

Test Circuit for Electrical Characteristics(1-5)



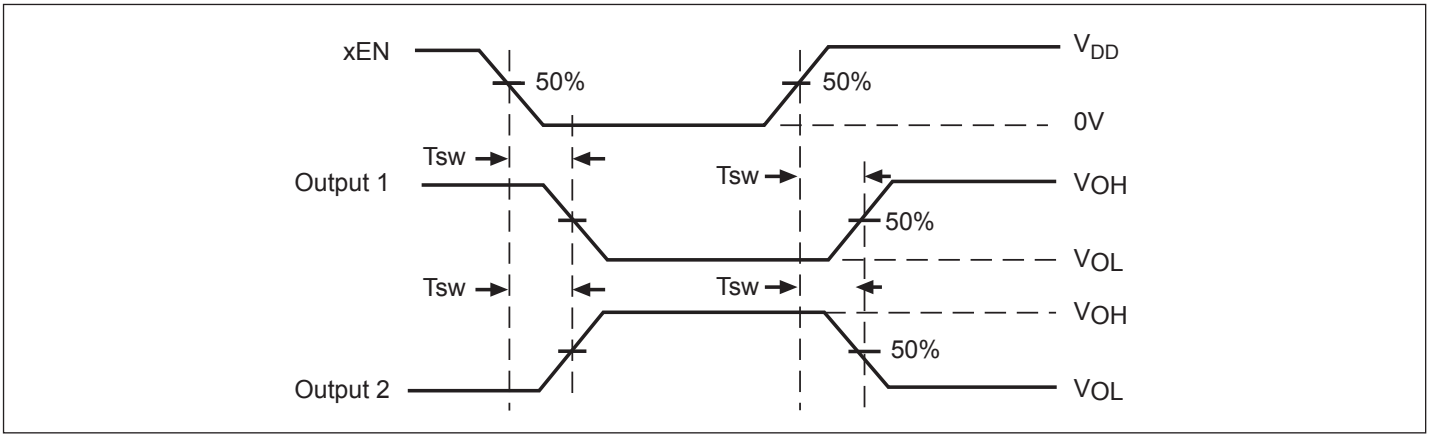
Notes:

1. C_L = Load capacitance: includes jig and probe capacitance.
2. R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator
3. Output 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
   Output 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
4. All input impulses are supplied by generators having the following characteristics: PRR ≤ MHz, $Z_O = 50\Omega$, $t_R \leq 2.5$ns, $t_F \leq 2.5$ns.
5. The outputs are measured one at a time with one transition per measurement.

Switch Positions

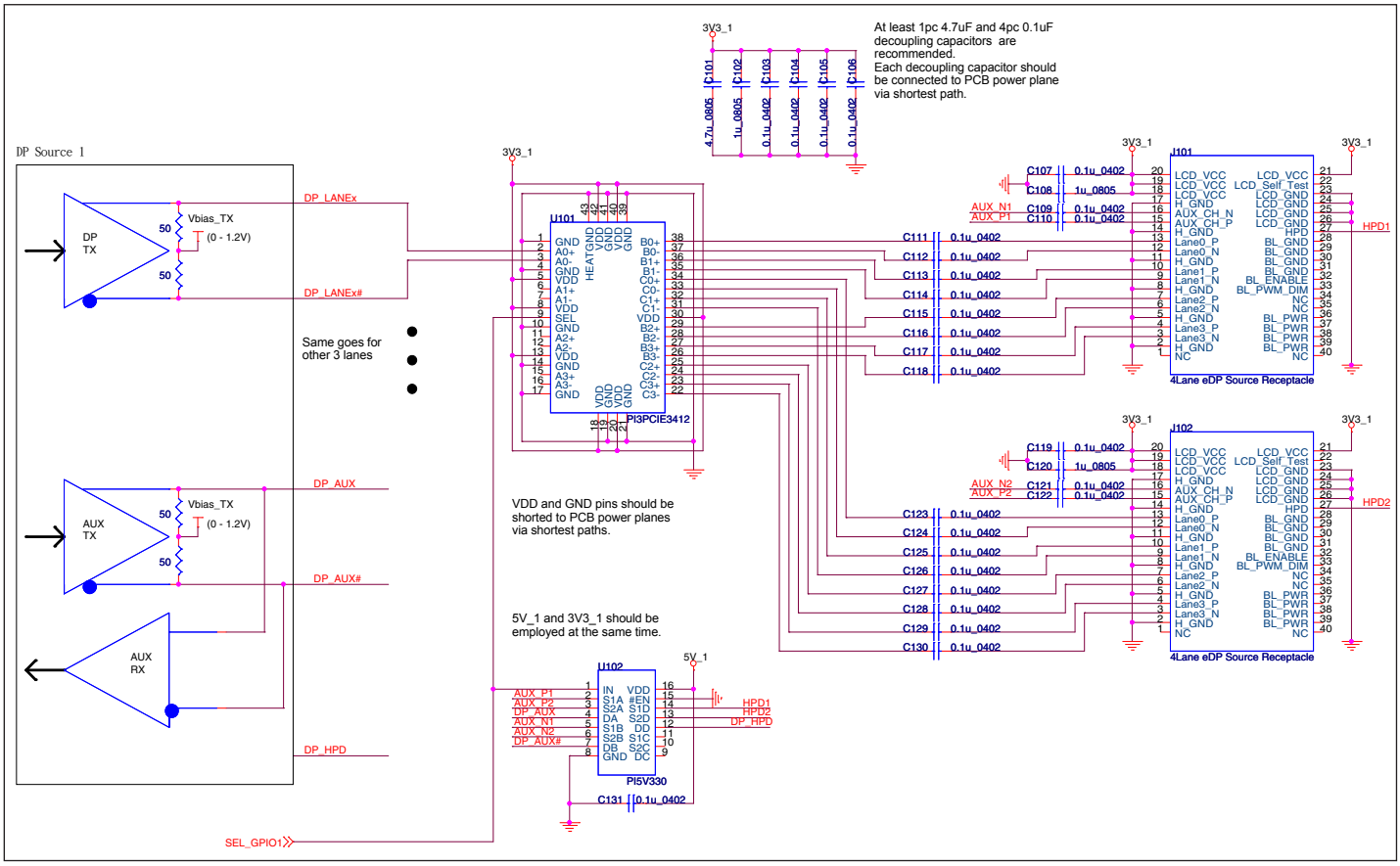
Test	Switch
t_{PLZ}, t_{PZL}	3.0V
t_{PHZ}, t_{PZH}	GND
Prop Delay	Open

Switching Waveforms



Voltage Waveforms Enable and Disable Times

DP1.2 Application



Part Marking Information

ZH Package

PI3PCIE
3412AZHE
○ YYWWXX̄

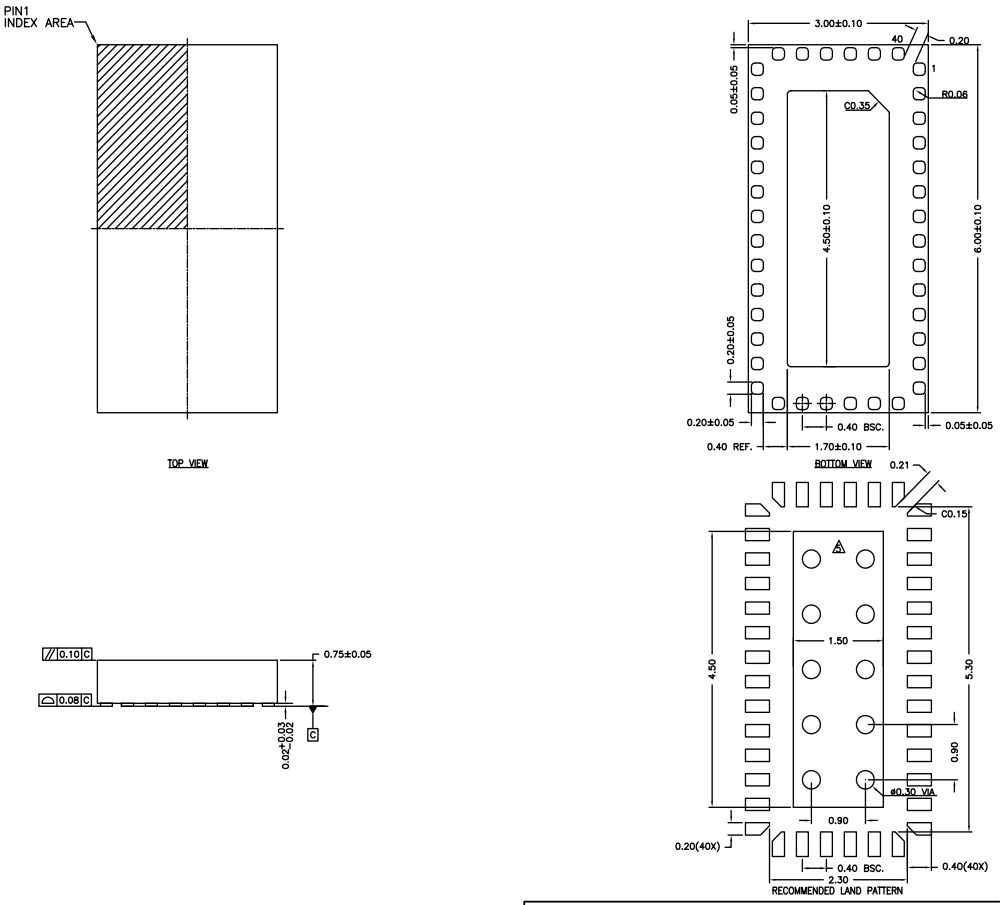
Y : Year
W : Workweek
1st X: Assembly Code
2nd X: Fab Code

ZL Package

PI3PCIE
3412AZLE
○ YYWWXX̄

Y : Year
W : Workweek
1st X: Assembly Code
2nd X: Fab Code

Packaging Mechanical : 40-TQFN (ZL)



NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED)

DATE: 09/29/17

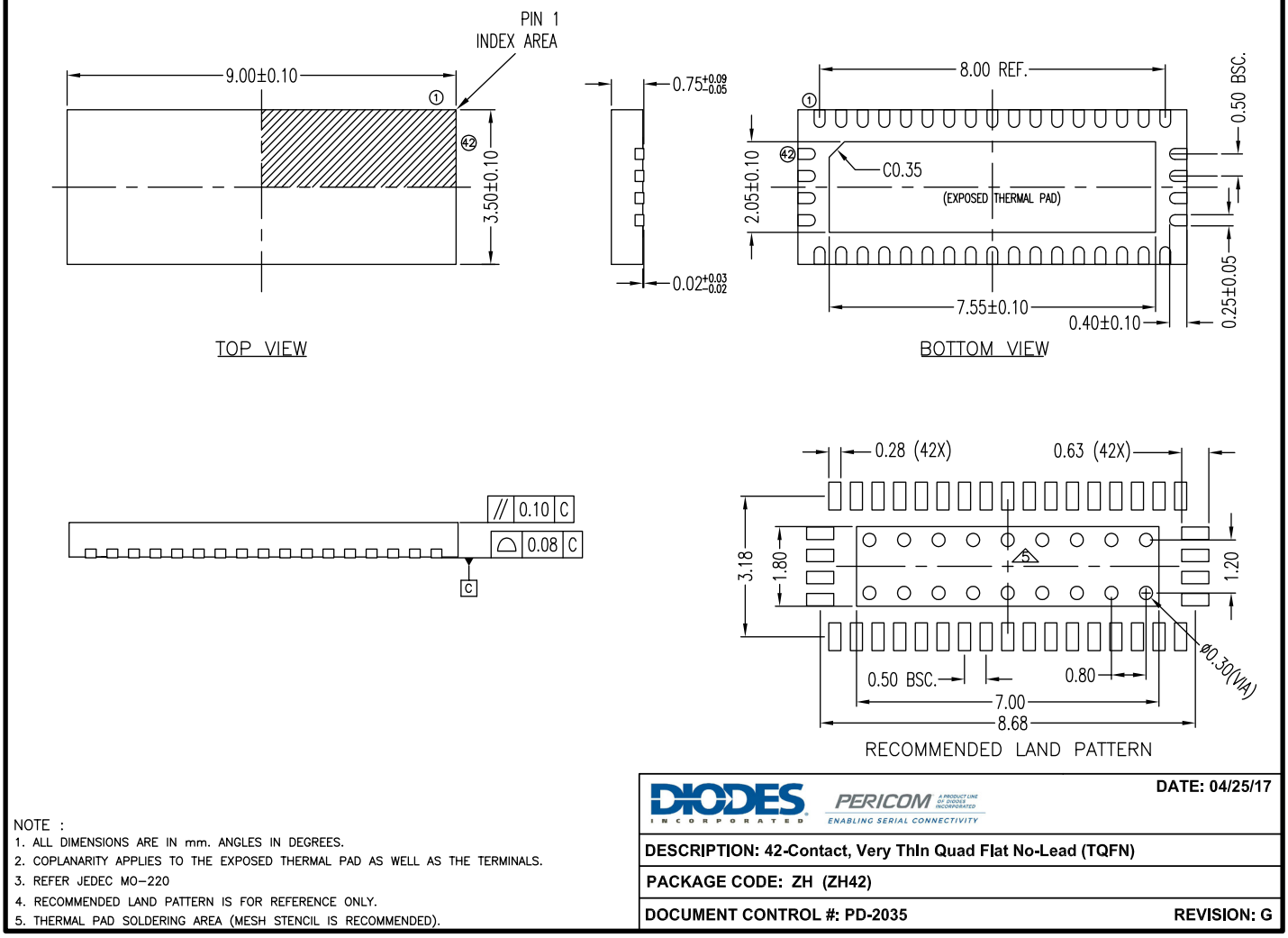
DESCRIPTION: 40-Pin, TQFN 3X6mm

PACKAGE CODE: ZL (ZL40)

DOCUMENT CONTROL #: PD-2165 REVISION: C

17-0681

Packaging Mechanical : 42-TQFN (ZH)



17-0266

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Code	Package Code	Package Description
PI3PCIE3412AZLEX	ZL	40-pin, 3x6mm(TQFN)
PI3PCIE3412AZHEX	ZH	42-contact, Very Thin Quad Flat No-Lead (TQFN)

Notes:

- Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel

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