AN4558(AN6552), AN4558S(AN6552S)

Dual Operational Amplifiers

■ Outline

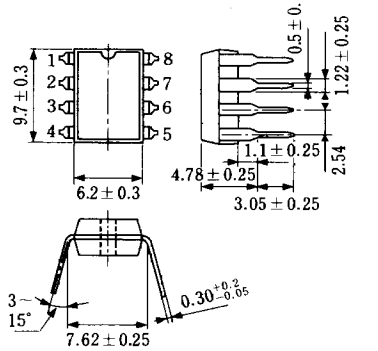
The AN4558(AN6552) and the AN4558S(AN6552S) are dual operational amplifiers with phase compensation circuits built-in, and suited for application to various electronic circuits such as active filters and audio preamplifiers.

■ Features

- Phase compensation circuit
- High gain, low noise
- Output short-circuit protection
- Slew rate : SR=1V/μs typ.

AN4558(AN6552)

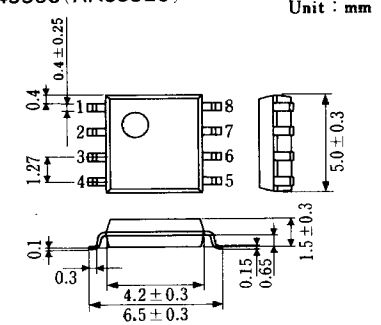
Unit : mm



8-Lead DIL Plastic Package

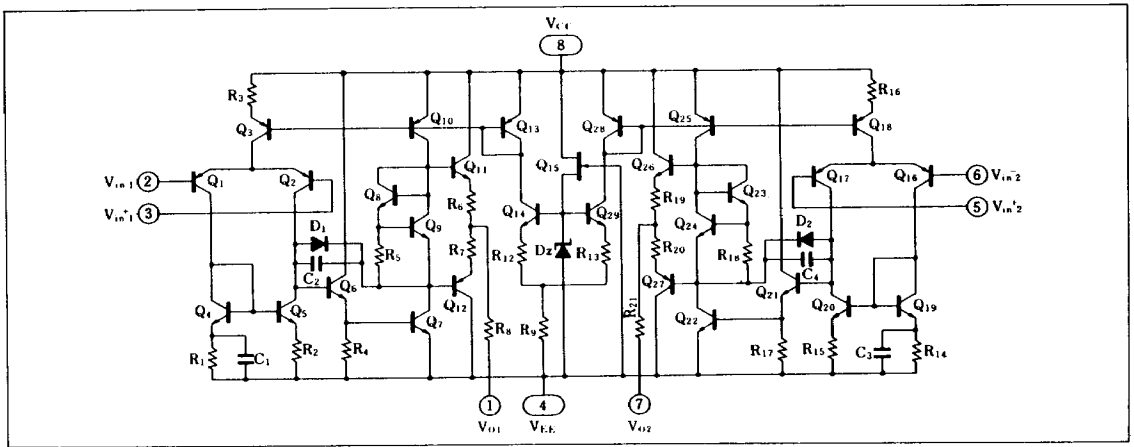
AN4558S(AN6552S)

Unit : mm



8-Lead PANAFLAT Package(SO-8D)

■ Schematic Diagram



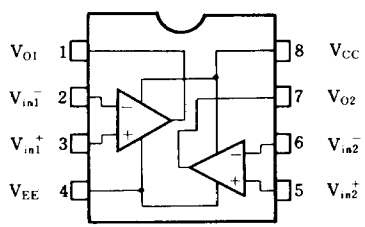
■ Absolute Maximum Ratings (Ta = 25℃)

Item			Symbol	Rating	Unit
Voltage	Supply Voltage		V_{CC}	±18	V
	Differential Input Voltage		V_{ID}	±30	V
	Common-Mode Input Voltage		V_{ICM}	±15	V
Power Dissipation	AN4558 (AN6552)		P_D	500	mW
	AN4558S (AN6552S)			360	
Temperature	Operating Ambient Temperature		T_{opr}	−20 ~ +75	℃
	Storage Temperature	AN4558 (AN6552)	T_{stg}	−55 ~ +150	℃
		AN4558S (AN6552S)		−55 ~ +125	

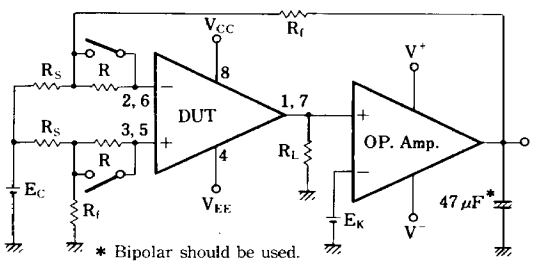
■ Electrical Characteristics (V_{CC} = 15V, V_{EE} = −15V, Ta = 25℃)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Input Offset Voltage	$V_{I(offset)}$	1	$R_S \leqq 10k\Omega$		0.5	6	mV
Input Offset Current	I_{IO}	1			5	200	nA
Input Bias Current	I_{Bias}	1				500	nA
Voltage Gain	G_V	1	$R_L \geqq 2k\Omega$, $V_O = \pm 10V$	86	100		dB
Maximum Output Voltage	$V_{O(max.)}$	2	$R_L \geqq 10k\Omega$	±12	±14		V
			$R_L \geqq 2k\Omega$	±10	±13		V
Common-Mode Input Voltage Width	V_{CM}	3		±12	±14		V
Common-Mode Rejection Ratio	CMR	1		70	90		dB
Supply Voltage Rejection Ratio	SVR	1			30	150	μV/V
Power Consumption	P_C	4	$R_L = \infty$		90	170	mW
Slew Rate	SR	5	$R_L \geqq 2k\Omega$		1.0		V/μs
Input Referred Noise Voltage	V_{ni}	6	R_S = 1kΩ, B = 10Hz ~ 30kHz		2.5		μV_{rms}

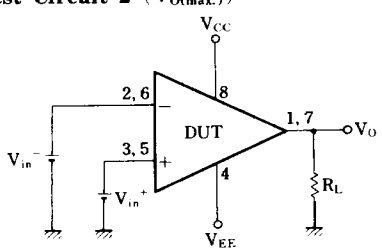
■ Pin Connection



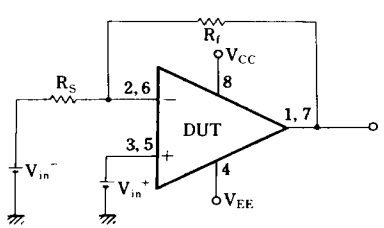
Test Circuit 1 ($V_{I(offset)}$, I_{IO}, I_{Bias}, G_V, CMR, SVR)



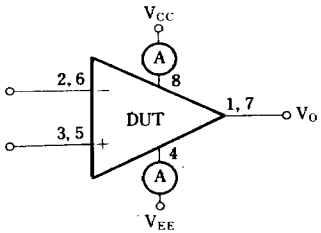
Test Circuit 2 ($V_{O(max.)}$)



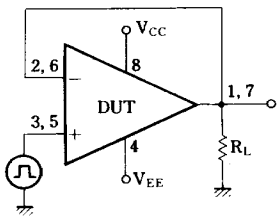
Test Circuit 3 (V_{CM})



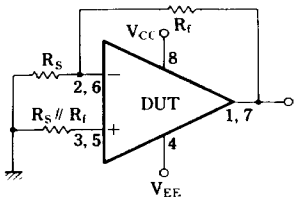
Test Circuit 4 (P_C)



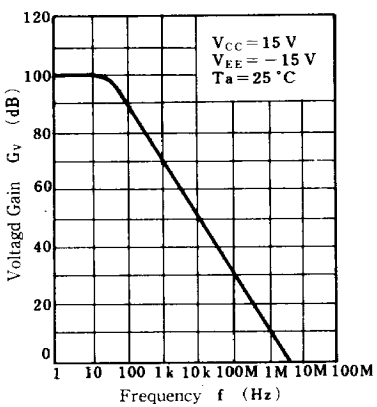
Test Circuit 5 (SR)



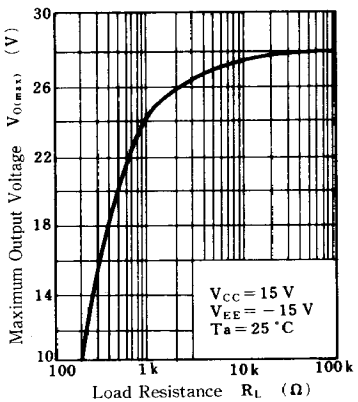
Test Circuit 6 (V_{ni})



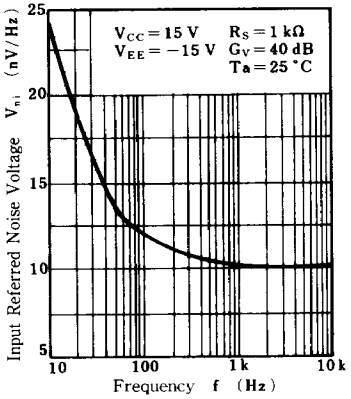
$G_V - f$



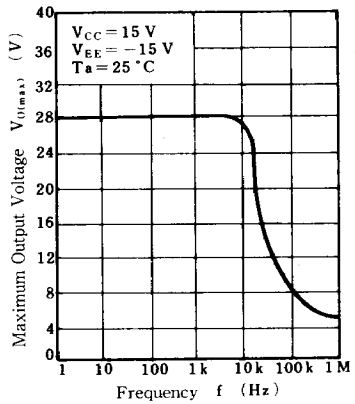
$V_{O(max)} - R_L$



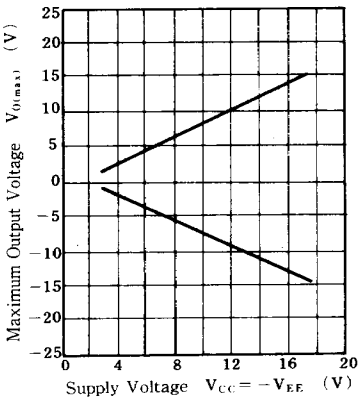
$V_{ni} - f$



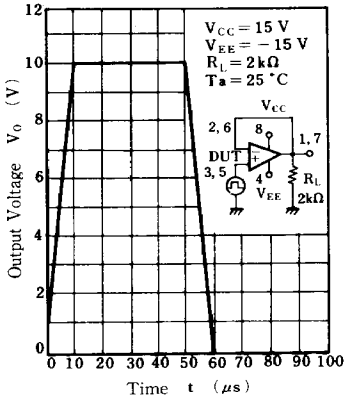
$V_{O(max)} - f$



$V_{O(max)} - V_{CC}, V_{EE}$



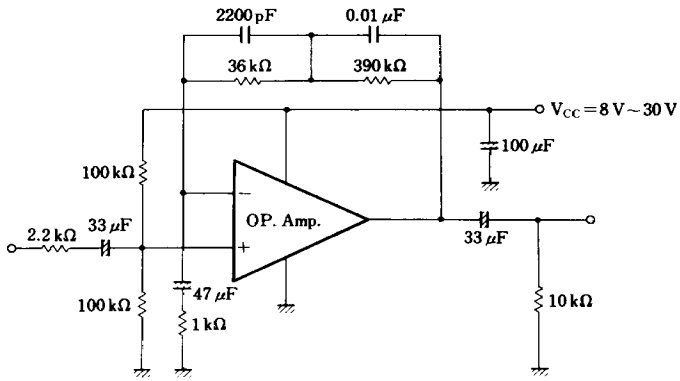
$V_O - t$



Panasonic

■ Application Circuit

RIAA Pre-Amp. (Single Voltage Operation)



■ Pin

Pin No.	Pin Name
1	Ch. 1 Output
2	Ch. 1 Invert Input
3	Ch. 1 Non Invert Input
4	V_{EE} (GND)
5	Ch. 2 Non Invert Input
6	Ch. 2 Invert Input
7	Ch. 2 Output
8	Vcc