

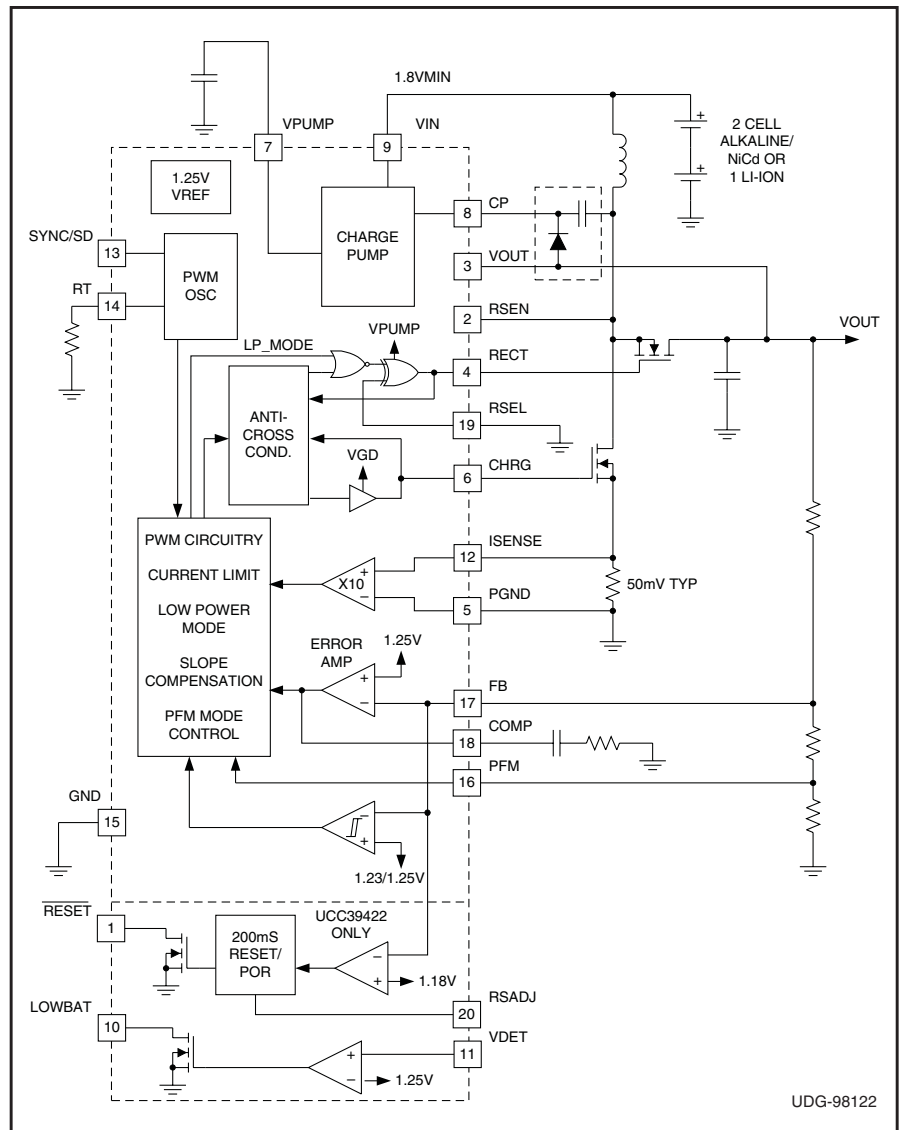
Multimode High Frequency PWM Controller

PRELIMINARY

FEATURES

- Operation Down to an Input Voltage of 1.8V
- High Efficiency Boost or Flyback (Buck-Boost) Topologies
- Drives External FETs for High Current Applications
- Up to 2MHz Oscillator
- Synchronizable Fixed Frequency Operation
- High Efficiency Low Power Mode
- High Efficiency at Very Low Power with Programmable Variable Frequency Mode
- Pulse by Pulse Current Limit
- 5 μ A Supply Current in Shutdown
- 150 μ A Supply Current in Sleep Mode
- Selectable NMOS or PMOS Rectification
- Built-in Power on Reset (UCC39422 Only)
- Built-in Low Voltage Detect (UCC39422 Only)

SIMPLIFIED BLOCK DIAGRAM AND APPLICATION CIRCUIT



DESCRIPTION

The UCC39421 family of synchronous PWM controllers is optimized to operate from dual Alkaline/NiCd cells or a single Lithium-Ion (Li-Ion) cell, and convert to adjustable output voltages from 2.5V to 8V. For applications where the input voltage does not exceed the output, a standard boost configuration is utilized. For other applications where the input voltage can swing above and below the output, a 1:1 coupled-inductor (Flyback or SEPIC) is used in place of the single inductor. Fixed frequency operation can be programmed, or synchronized to an external clock source. In applications where at light loads variable frequency mode is acceptable, the IC can be programmed to automatically enter PFM (Pulse Frequency Modulation) mode for an additional efficiency benefit.

Synchronous rectification provides excellent efficiency at high power levels, where N or P type MOSFETs can be used. At lower power levels (10-20% of full load) where fixed frequency operation is required, Low Power Mode is entered. This mode optimizes efficiency by cutting back on the gate drive of the charging FET. At very low power levels, the IC enters a variable frequency mode (PFM). PFM can be disabled by the user.

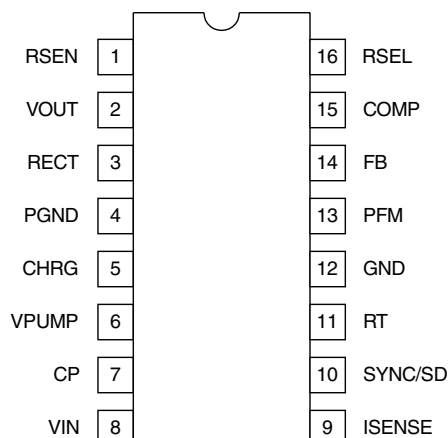
Other features include pulse by pulse current limiting, and a low 5 μ A quiescent current during shutdown. The UCC39422 incorporates programmable Power on Reset circuitry and an uncommitted comparator for low voltage detection. The available packages are 20 pin TSSOP, or 20 pin N for the UCC39422, and 16 pin TSSOP, or 16 pin N for the UCC39421.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VIN, VOUT, VPUMP)	8V
CP	8V
RSEN	–0.3 to 12V
SYNC/SD	–0.3 to 5V
ISENSE	–0.3 to 1V
Storage Temperature	–65°C to +150°C
Junction Temperature	–55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

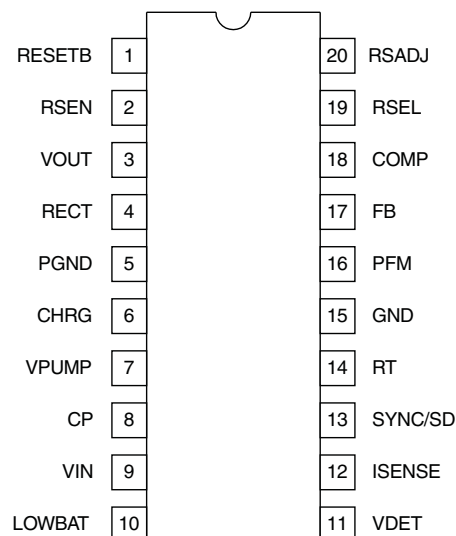
All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

TSSOP-16, DIL-16 (TOP VIEW) N, PW Packages



CONNECTION DIAGRAMS

TSSOP-20, DIL-20 (TOP VIEW) N, PW Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ for UCC29421/2, 0°C to $+70^{\circ}\text{C}$ for UCC39421/2; $R_T=100\text{K}$, $V_{VPUMP}=6\text{V}$, $V_{VIN}=3\text{V}$

PARAMETER	TEST CONDITIONS	MIN		MAX	UNITS
VIN Section					
Minimum Start-up Voltage			1.5	1.8	V
Operating Current	Not in PFM Mode, No Load		35	60	μA
Sleep Mode Current	PFM Mode, No Load		35	60	μA
Shutdown Supply Current	SYNC/SD = High		1.5	4	μA
Startup Frequency	$V_{IN} = 1.8\text{V}$	60	120	190	kHz
Startup Off Time	$V_{IN} = 1.8\text{V}$		2	5	μs
Startup CS Threshold	$V_{IN} = 1.8\text{V}$		36	56	mV
Minimum PUMP or VOUT Voltage to Exit Startup		2.2	2.5	2.8	V
VPUMP Section					
Regulation Voltage	$V_{VOUT}=3.3\text{V}$	5.5		6.6	V
Operating Current	Outputs OFF		100	275	μA
Sleep Mode Current			5	15	μA
Shutdown Supply Current	SYNC/SD = High, $V_{OUT} = 3\text{V}$, $V_{VPUMP} = 3\text{V}$		2	15	μA
CP Voltage to Turn On Pump Switch	$V_{VPUMP} = 5\text{V}$		5.3	5.5	V
Pump Switch $R_{DS(on)}$			4		Ω

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PARAMETER	TEST CONDITIONS	MIN		MAX	UNITS
VOUT Section					
Operating Current			500	650	μA
Sleep Mode Current		50	100	150	μA
Shutdown Supply Current	SYNC/SD = High		1	2.2	μA
V_{PUMP} to V_{OUT} Threshold to Enable N-Channel Rectifier	$V_{\text{OUT}} = 3.3\text{V}$	1.4	1.7	2.0	V
Error Amp Section					
Regulation Voltage	$2\text{V} < V_{\text{IN}} < 5\text{V}$	1.21	1.24	1.27	V
FB Input Current	$V_{\text{FB}} = 1.25\text{V}$		100	350	nA
Max Sinking Current, I_{OL}	$V_{\text{COMP}} = 1\text{V}$, $V_{\text{FB}} = \text{Regulation Voltage} + 50\text{mV}$	6.5	13	20	μA
Max Sourcing Current, I_{OH}	$V_{\text{COMP}} = 0\text{V}$, $V_{\text{FB}} = \text{Regulation Voltage} - 50\text{mV}$	-20	-13	-6.5	μA
Transconductance	$V_{\text{FB}} = \text{Regulation Voltage} \pm 4\text{mV}$	150	270	370	μS
Unity Gain Bandwidth	$C_C = 330\text{pF}$		100		kHz
Max Output Voltage	$V_{\text{FB}} = 0\text{V}$		1.9	2.3	V
Oscillator Section					
Frequency Stability	$R_T = 350\text{k}$	100	150	190	kHz
	$R_T = 100\text{k}$	375	475	575	kHz
	$R_T = 35\text{k}$	0.9	1.2	1.4	MHz
RT Voltage		0.600	0.625	0.650	V
SYNC Threshold		0.9	1.2	1.6	V
SYNC Input Current	SYNC/SD = 2.5V			200	nA
Max SYNC High Time	To Avoid Shutdown	11	20	29	μs
SYNC Range	$R_T = 100\text{k}$	$1.1f_o$		$1.5f_o$	kHz
Current Sense Section					
Gain		8	10	11	V/V
Overcurrent Limit Threshold			150	200	mV
Unity Gain Bandwidth			25		MHz
COMP Voltage to I_{SENSE} Accuracy	$I_{\text{SENSE}} = 70\text{mV}$	0.8	1.0	1.2	V
PWM Section					
Maximum Duty Cycle	$V_{\text{ISENSE}} = 0\text{V}$, $V_{\text{FB}} = 0\text{V}$	80	88		%
Minimum Duty Cycle	$V_{\text{FB}} = 1.5\text{V}$			0	%
Low Power Mode V_{COMP} Threshold	At COMP pin	0.5	0.6	0.7	V
Slope Compensation Accuracy	$R_T = 350\text{k}$, $R_{\text{SLOPE}} = 20\text{k}$	1.4	2.8	4.0	A/s
Rectifier Zero Current Threshold	RSEL = GND	-2	15	28	mV
	RSEL = VIN	-28	-15	2	mV
RSEL Threshold		0.5	0.9	1.3	V
PFM Section					
PFM Disable Threshold		0.17	0.22	0.27	V
Comp Hold During Sleep	$V_{\text{PFM}} = 0.4$		0.45		V
Startup Delay After Sleep	$V_{\text{FB}} < 1.23\text{V}$		4	9	μs
FB Voltage to Sleep Off		1.19	1.22	1.25	V
FB Voltage to Sleep On		1.22	1.25	1.28	V
Low Power Mode Timer After Sleep			250	450	μs

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PARAMETER	TEST CONDITIONS	MIN		MAX	UNITS
VGSW Drive Section					
Rise Time	$C_O = 1\text{nF}$		18	35	ns
Fall Time	$C_O = 1\text{nF}$		14	30	ns
Output High	$I_{OUT} = -100\text{mA}$, Respect to VPUMP		0.4	0.65	V
	$I_{OUT} = -1\text{mA}$, Respect to VPUMP		4	10	mV
Output Low	$I_{OUT} = 100\text{mA}$		0.2	0.35	V
	$I_{OUT} = 1\text{mA}$		2	6	mV
Charge Off to Rectifier On Delay		10	30	50	ns
RECT Drive Section					
Rise Time	$C_O = 1\text{nF}$		20	40	ns
Fall Time	$C_O = 1\text{nF}$		14	30	ns
Output High	$I_{OUT} = -100\text{mA}$, Respect to VPUMP		0.2	0.5	V
	$I_{OUT} = -1\text{mA}$, Respect to VPUMP		5	10	mV
Output Low Rectifier	$I_{OUT} = 100\text{mA}$		0.2	0.35	V
	$I_{OUT} = 1\text{mA}$		2	6	mV
Rectifier Off to Charge On Delay		10	20	50	ns
RESET Section (UCC39422 Only)					
Reset Timeout	$C_{RSADJ} = 0.33\mu\text{F}$	100	250	400	ms
Reset Threshold	% Below Regulation Voltage	-7	-5.5	-4	%
Output Low Voltage	Reset Condition, $I = 5\text{mA}$		0.1	0.25	V
Output Leakage	RESET = 8V		0.05	0.2	μA
Voltage Detection Section (UCC39422 Only)					
Threshold Voltage		1.18	1.26	1.34	V
Output Low Voltage	$I = 5\text{mA}$		0.15	0.3	V
Output Leakage	LOWBAT = 8V		0.05	0.25	μA

PIN DESCRIPTIONS

COMP: This is the output of the transconductance error amplifier. Connect the compensation components from this pin to ground.

CHRG: This is the gate drive output for the N-channel charge MOSFET. Connect it to the gate directly, or through a low value gate resistor.

CP: This is the input for the charge pump. For applications requiring a charge pump, connect this pin to the charge pump diode and flying capacitor, as shown in the applications diagram of Fig 5. For applications where no charge pump is required, this pin should be grounded.

FB: The feedback input is the inverting input to the transconductance error amplifier. Connect this pin to a resistive divider between V_{OUT} and ground. The output voltage will be regulated to:

$$V_{OUT} = 1.25 \cdot \frac{R1}{(R1 + R2)}$$

where R1 goes to GND and R2 goes to V_{OUT} .

GND: This is the signal ground pin for the device. It should be tied to the local ground plane.

ISENSE: This is the input to the X10 wide bandwidth current sense amplifier. Connect this pin to the high side of the current sense resistor. An internal current is sourced out this pin for slope compensation. For applications requiring slope compensation (or filtering of the current sense signal), use a resistor in series with this pin.

LOWBAT: This is the open drain output of the uncommitted comparator. (UCC39422 only). This output is low when the VDET pin is above 1.25V.

PIN DESCRIPTIONS (cont.)

PFM: This is the programming pin for the PFM (Pulse Frequency Modulation) Mode threshold. Connect this pin to a resistive divider off of the FB pin (or VOUT) to set the PFM threshold. To disable PFM Mode, connect this pin to ground (below 0.2V).

PGND: This is the power ground pin for the device. Connect it directly to the ground return of the current sense resistor.

RECT: This is the gate drive output for the synchronous rectifier. Connect it to the gate of the P or N channel MOSFET directly, or through a low value gate resistor.

RECTSEN: This pin is used to sense the voltage across the synchronous rectifier for commutation. In boost configurations, connect this pin through a 1K resistor to the junction of the two MOSFETs and the inductor. In flyback and SEPIC configurations, connect this pin through a 1K resistor to the junction of the drain of the synchronous rectifier and the secondary side winding of the coupled inductor.

RSADJ: A capacitor from this pin to ground sets the reset delay. (UCC39422 only)

RSEL: This pin programs the device for N channel or P channel synchronous rectifiers by inverting the phase of the RECT gate drive output. Connect this pin to ground for N-channel MOSFETs, connect it to V_{IN} for P-channel MOSFETs.

RESET: This is the open drain output of the Reset comparator. (UCC39422 only) and is active low.

RT: A resistor from this pin to ground programs the frequency of the pulse width modulator.

SYNC/SD: This dual function pin is the SYNC and Shutdown input. To synchronize the internal clock to an external source, this pin must be driven above 2.0V. The clock syncs to the rising edge of the input. To shutdown the converter, this pin must be held high (above 2.0V) for a minimum of 20μsec. If not used, this pin should be grounded.

VPUMP: This is the output of the charge pump. For applications requiring a charge pump, connect a 1μF capacitor from this pin to ground. Otherwise, connect this pin to the higher of V_{IN} or V_{OUT}, and decouple with a 0.1μF capacitor.

VOUT: Connect this pin to the output voltage. This input is used for sensing the voltage across the synchronous rectifier and for bootstrapping the gate drive to the charge FET and should be decoupled with a 0.1μF capacitor.

VIN: This is the input power pin of the device. Connect this pin to the input voltage source. A 0.1μF decoupling capacitor should be connected between this pin and ground.

VDET: This is the non-inverting input to an uncommitted comparator. This input may be used for detecting a low battery condition. (UCC39422 only)

APPLICATION INFORMATION

The UCC39421 is a high frequency, synchronous PWM controller optimized for portable, battery powered applications where size and efficiency are of critical importance. It includes high speed, high current FET drivers for those converter applications requiring low RDS_{ON} external MOSFETs. A detailed block diagram is shown in Fig 1.

Optimizing Efficiency

The UCC39421 optimizes efficiency, extending battery life, by its low quiescent current and its synchronous rectifier topology. The additional features of Low Power Mode and PFM Mode maintain high efficiency over a wide range of load current. These features will be discussed in detail.

Power Saving Modes

Since this is a peak current mode controller, the error amplifier output voltage sets the peak inductor current required to sustain the load. The UCC39421 incorporates two special modes of operation designed to optimize efficiency over a wide range of load current. This is done by comparing the error amplifier output voltage (on the COMP pin) to two fixed thresholds (one of which is user programmable). If the error amplifier output voltage drops below the first threshold, Low Power (LP) mode will be entered. If the error amplifier output voltage drops even further, below a second user programmable threshold, PFM Mode will be entered. These modes of operation are designed to maintain high efficiency at light load, and are described in detail below. Refer to the simplified block diagram of Fig. 2 for the control logic.



APPLICATION INFORMATION (cont.)

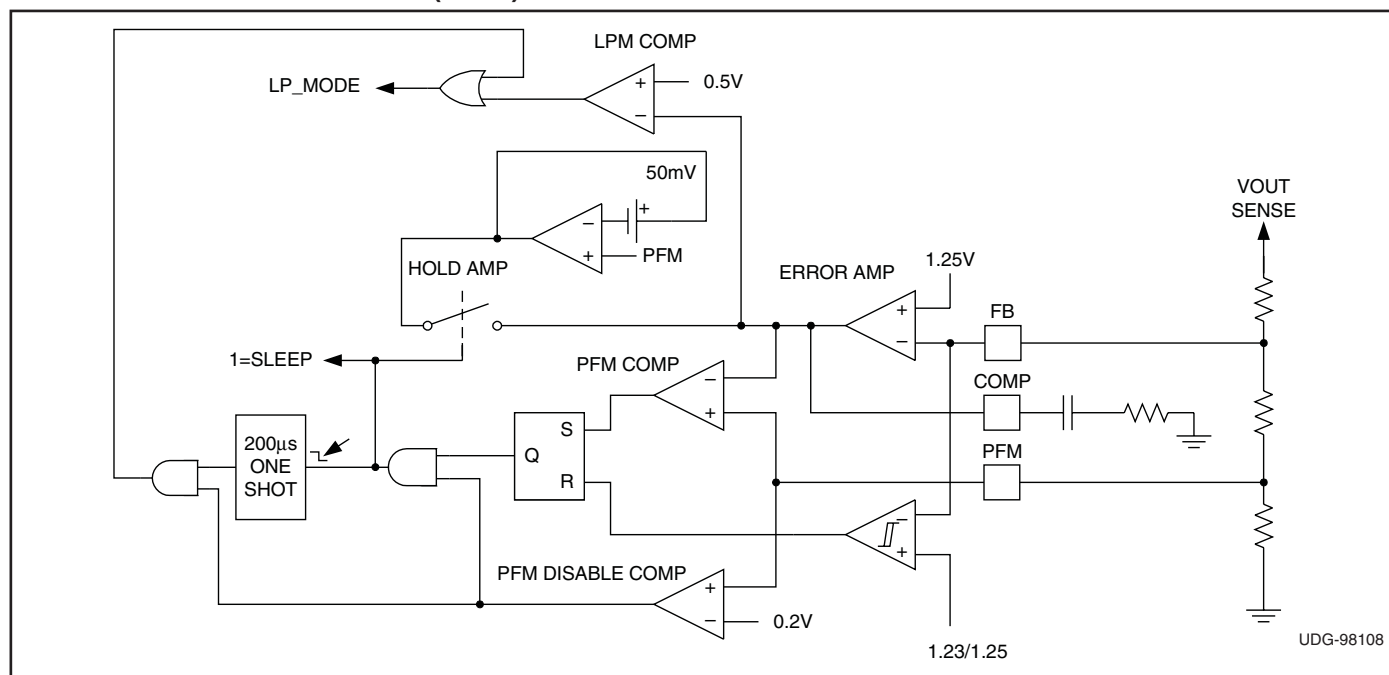


Figure 2. Simplified block diagram of Low Power and Pulse Mode control logic.

Low Power Mode

During normal operation, at medium to high load currents, the switching frequency remains fixed, programmed by the resistor on the RT pin. At these higher loads, the gate drive output on the CHRG pin (for the N channel charge FET) will be the higher of V_{IN} or V_{PUMP} . When the load current drops (sensed by a drop in the error amp voltage), the UCC39421 will automatically enter LP mode, and the gate drive voltage on the CHRG pin will be reduced to lower gate drive losses. This helps to maintain high efficiency at light loads where the gate drive losses begin to dominate and the lowest possible $R_{ds(on)}$ is not required. If the load increases, normal or “High Power” mode will resume. The expression for gate drive power loss is given by equation 1. It can be seen that the power varies as a function of the applied gate voltage squared.

$$P_{GATELOSS} = \frac{Q_G \cdot V_G^2 \cdot f}{V_S} \quad (1)$$

Where Q_g is the total gate charge and V_s is the gate voltage specified in the MOSFET manufacturer’s data sheet, V_g is the applied gate drive voltage, and f is the switching frequency.

The nominal COMP voltage where LP mode will be entered is 0.5V. Given the internal offset and gain of the current sense amplifier, this corresponds to a peak switch current of:

$$I_{PEAK} = \frac{(0.5 - 0.3)}{K \cdot R_{SENSE}} = \frac{0.02}{R_{SENSE}} \quad (2)$$

Where 0.5V is the threshold for LP mode, 0.3V is the internal offset and K is the nominal current sense amplifier gain of 10 and R_{SENSE} is the value of the current sense resistor. If the peak inductor current is below this value, the UCC39421 will enter LP mode and the gate drive voltage on the CHRG pin will be equal to V_{in} . At peak currents higher than this, the gate drive voltage will be the higher of V_{IN} or V_{PUMP} .

PFM Mode

At very light loads, the UCC39421 will enter PFM Mode. In this mode, when the error amplifier output voltage drops below the PFM threshold, the controller goes into sleep mode until V_{OUT} has dropped slightly (20mV measured at the feedback pin). At this time, the controller will turn back on and operate at fixed frequency for a short duration (typically a few hundred microseconds) until the output voltage has increased and the error amplifier output voltage has dropped below the PFM threshold once again. Then the converter will turn off and the cycle will repeat. This results in a very low duty cycle of operation, reducing all losses and greatly improving light load efficiency. During sleep mode, most of the circuitry internal to the UCC39421 is powered down, reducing quiescent current and maximizing efficiency.

APPLICATION INFORMATION (cont.)

The peak inductor current at which this mode will be entered is user programmable, by setting the voltage on the PFM pin. This can be done with a single resistor in series with the feedback divider, as shown in the application diagrams. The nominal peak current threshold for PM mode will be defined by:

$$I_{PEAK} \cong \frac{\left(\frac{1.25 \cdot R1}{(R1 + R2)} \right) - 0.3}{K \cdot R_{SENSE}} \quad (3)$$

Where 0.3V is the internal offset and K is the nominal current sense amplifier gain of 10 and R_{SENSE} is the value of the current sense resistor. Note that in this case, the PFM pin voltage is set by the R1/R2 resistive divider off of the FB pin, which is regulated to 1.25V.

To further increase efficiency in Pulse mode, the gate drive on the CHRG pin will be held in the LP mode for 200μsec each time the controller comes on. This keeps gate drive losses low, even though the error amplifier output voltage may overshoot slightly when coming out of PFM. During sleep mode, the COMP pin is forced to 50mV above the PFM pin voltage. This minimizes error amplifier overshoot when coming out of sleep mode, and prevents erroneously tripping the PFM comparator.

Disabling PFM Mode

The user may disable PFM mode by pulling the PFM pin below 0.2V. In this case, the UCC39421 will remain on, in fixed frequency operation at all load currents. The PFM pin can also be driven, through a resistive divider, off of an output from the system controller. This allows the system controller to prepare for an expected step increase in load, improving the converter's large signal transient response. An example of this is shown in Fig 3.

Choosing a Topology and Optimal Synchronous Rectifier

The UCC39421 is designed to be very flexible, and can be used in Boost, Flyback and SEPIC topologies. It can operate from input voltages between 1.8 and 8.0V. Output voltages can be between 2.5V and 8.0V. (Note that at higher input voltages, such as from four or five Alkaline or Nickel cells or two Li-ion cells, a buck regulator

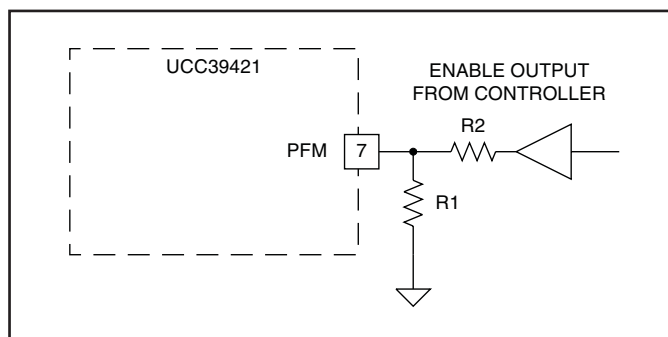


Figure 3. Driving the PFM pin from a controller output.

would usually be employed.) It will also drive either N-channel or P-channel MOSFET synchronous rectifiers. Table 1 can be used to select the appropriate topology for a given combination of input and output voltage requirements. Although it is designed to operate as a peak current mode controller, it can also be configured for voltage mode control. This will be discussed in a later section.

The user can program the gate drive output on the RECT pin for N-channel MOSFETs by grounding the RSEL pin, or for P-channel MOSFETs by connecting the RESEL pin to VIN. Table 2 is used to determine whether an N or P channel synchronous rectifier should be used.

Note: In all cases, low voltage logic MOSFETs should be used to achieve the lowest possible on-resistance for the highest efficiency.

The application diagrams in Figs 4-8 illustrate the use of the UCC39421 in all the topologies, using N and P channel rectifiers. They will be discussed in detail in the next section.

Note that the higher the frequency of operation, the more critical the MOSFET gate charge becomes for efficiency, particularly at light loads. However, high load currents demand lower $R_{DS(ON)}$, which will tend to increase gate charge. These two parameters should be balanced. At lower frequencies, the gate charge will become less important, at 1MHz or more, it is critical.

Table 1. Selecting Topology Based on Input and Output Voltage Requirements

Cell Type	No. of Cells	V _{IN} Range	V _{OUT}	Topology
Alkaline or NiCd, NiMH	2	1.8V - 3.0V	3.0 < V < 8.0	Boost
	3	2.7V - 4.5V	2.5 < V < 3.9	Flyback or SEPIC
			4.5 < V < 8.0	Boost
Li-Ion	1	2.3V - 4.2V	2.5 < V < 3.6	Flyback or SEPIC
			4.2 < V < 8.0	Boost

APPLICATION INFORMATION (cont.)

Boost Topology

The boost topology is simple and efficient, and should be used whenever the desired output voltage is greater than the maximum input voltage.

Boost Using Two N-Channel MOSFETs

A boost converter using two N-channel MOSFETs is shown in Fig 4. This configuration is optimal for output voltages below 4V, where the output voltage may not be high enough to provide optimal gate drive for a P-channel MOSFET. Note that in this case, a charge pump is required to provide proper gate drive levels. This

is easily accomplished by adding an external diode and a capacitor, as shown. The diode connects from the output voltage to the CP pin. It should be an ultrafast or a Schottky diode. A 0.1μF ceramic capacitor is connected from the drain of the charge FET to the CP pin. This is the “flying” cap that will be charged to ($V_{OUT} - V_{DIODE}$) every time the charge FET is on. A charge pump reservoir cap is connected from the VPUMP pin to ground. It should be at least 1μF. A high speed active rectifier inside the UCC39421 charges the pump capacitor from the CP pin. The charge pump voltage will be:

Table II. Selecting Synchronous Rectifier Based on Topology and Output Voltage

Topology	VOUT	Synchronous Rectifier
Boost	$3.0 < V < 8.0$	P-channel (low voltage logic)
	$V < 4.0$	N-channel (low voltage logic) <i>Note: Requires a diode and a capacitor for the charge pump</i>
Flyback	$2.5 < V < 3.0$	N-channel (low voltage logic) <i>Note: Requires a diode and a capacitor for the charge pump</i>
	$3.0 < V < 8.0$	N-channel (low voltage logic)
SEPIC	$3.0 < V < 8.0$	P-channel (low voltage logic)

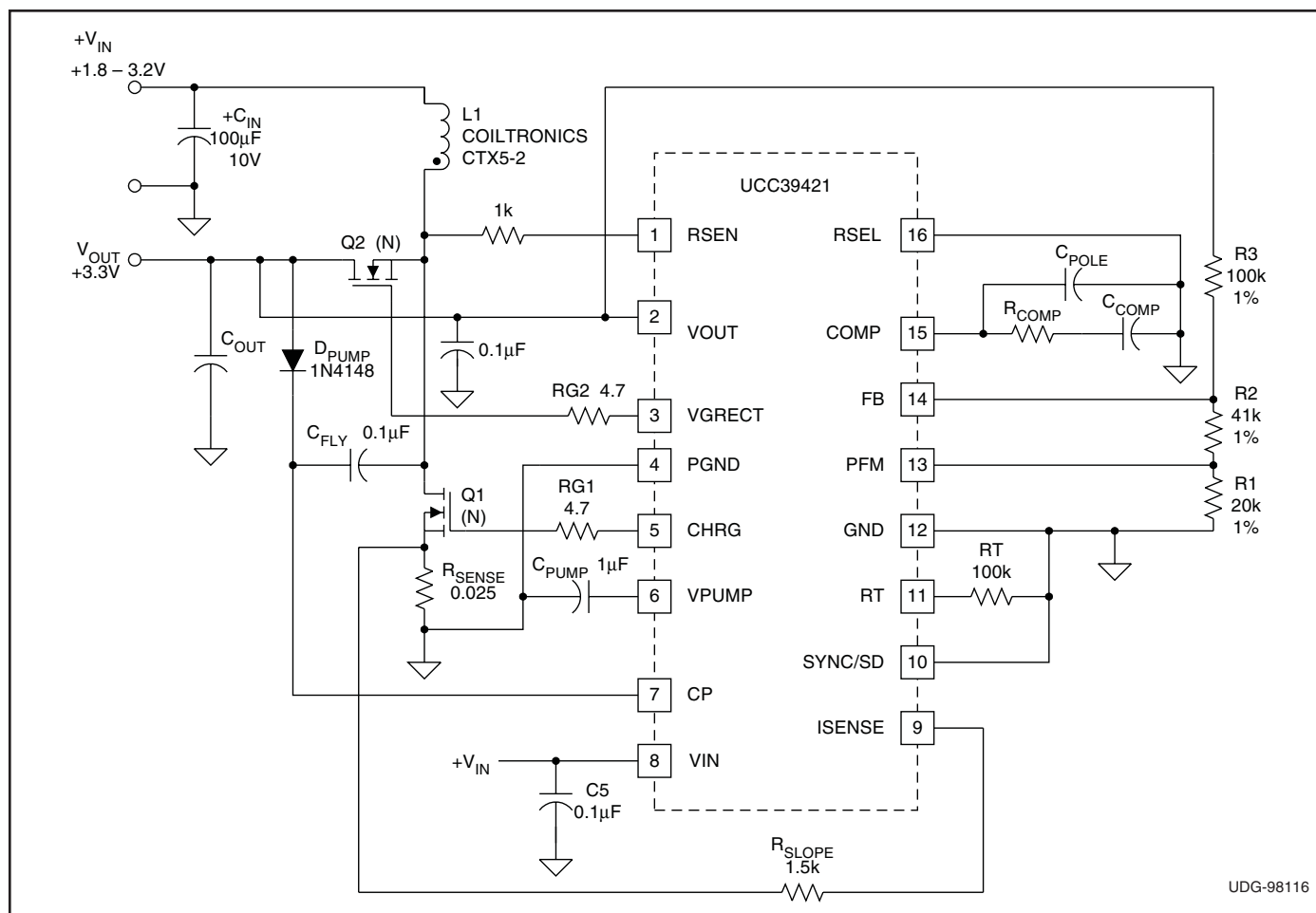


Figure 4. Application diagram for the boost topology using an N-channel synchronous rectifier.

APPLICATION INFORMATION (cont.)

$$V_{PUMP} \cong 2 \bullet V_{OUT} \quad (4)$$

For a block diagram of the charge pump logic, refer to Fig 12.

Note: A charge pump should not be used at output voltages over 4.0V to avoid pump voltages exceeding 8V.

For other applications, where the charge pump is not required, the CP pin should be grounded and the pin should be connected to either V_{OUT} or V_{IN} , whichever is greater.

Boost Using N & P Channel MOSFETs

For output voltages greater than the input and greater than about 3.0V, a P-channel MOSFET may be used for the synchronous rectifier. This configuration is shown in Fig 5. In this case, the VPUMP pin should be connected to V_{OUT}. This configuration can be used for a 3.3V output if a low voltage logic MOSFET is used.

Relating Peak Inductor Current to Average Output Current for the Boost Converter

For a continuous mode boost converter, the average output current is related to the peak inductor current by the following:

$$I_{PEAK} = \left(\frac{I_{OUT}}{(1-D)} \right) + \frac{di}{2} \quad (5)$$

where D is the duty cycle and the inductor ripple current, dl , is defined as:

$$di = \frac{t_{ON} \cdot V_{IN}}{I} = \frac{D \cdot V_{IN}}{f \cdot I} \quad (6)$$

where f is the switching frequency and L is the inductor value. The duty cycle is defined as:

$$D = \left(\frac{V_O - V_{IN}}{V_O} \right) \quad (7)$$

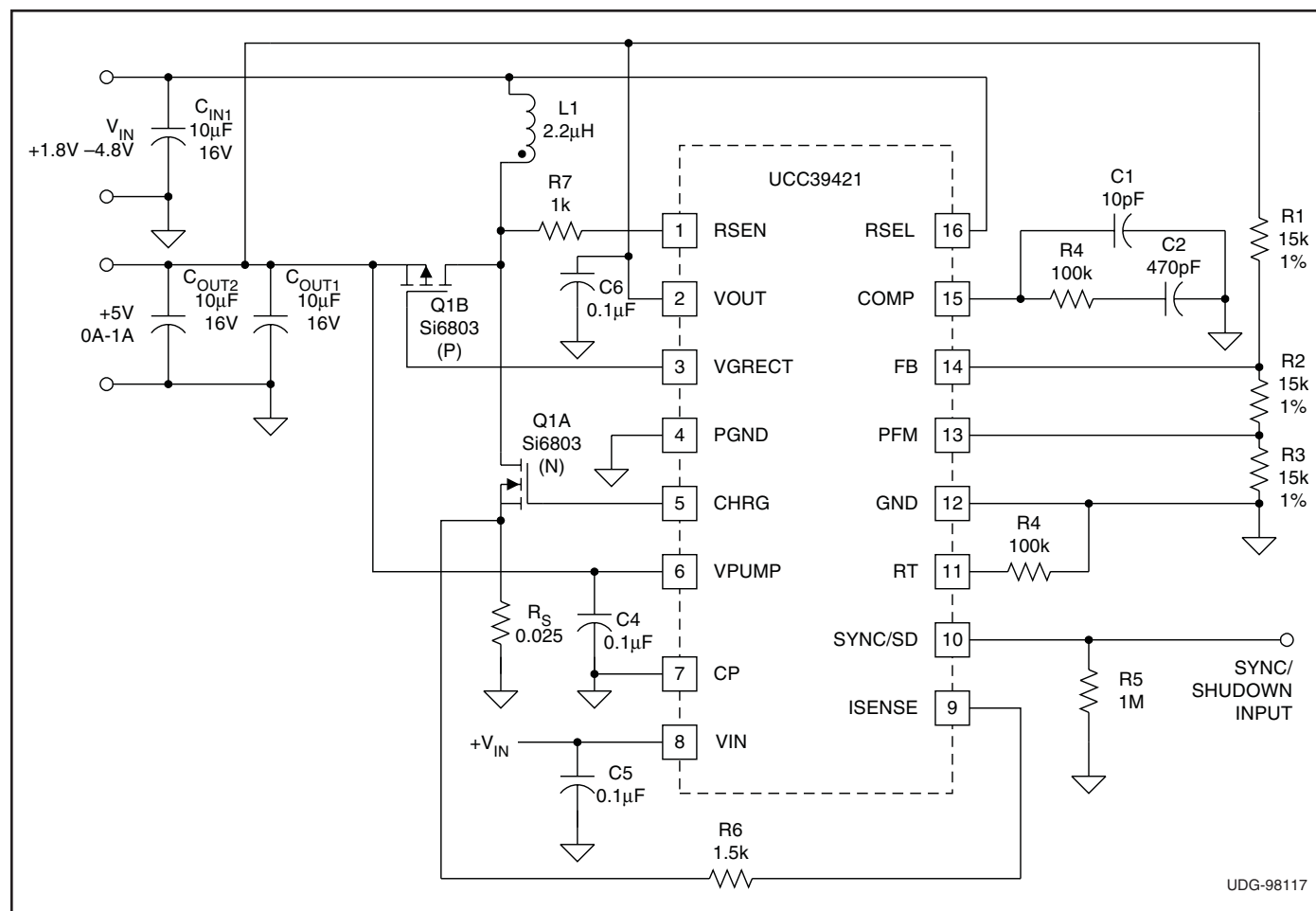


Figure 5. Application diagram for the boost topology using a P-channel synchronous rectifier.

APPLICATION INFORMATION (cont.)

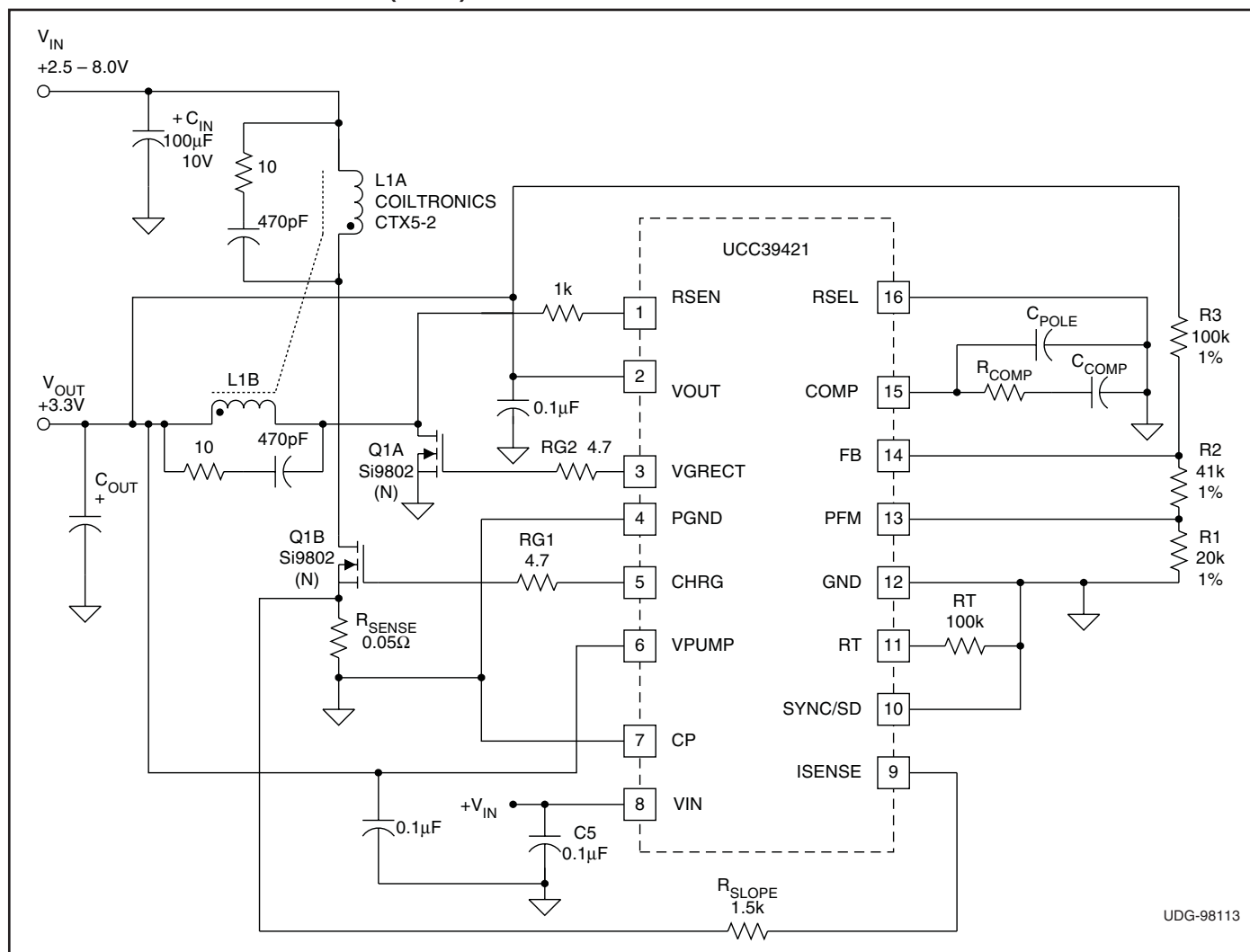


Figure 6. Application diagram for the flyback topology using an N-channel synchronous rectifier.

Substituting equations (6) and (7) into equation (5) yields:

$$I_{PEAK} = \frac{I_O}{\left(1 - \left(\frac{V_O - V_{IN}}{V_O}\right)\right)} + \frac{V_{IN}}{2 \bullet f \bullet L} \bullet \left(\frac{V_O - V_{IN}}{V_O}\right) \quad (8)$$

Note: In these equations, the voltage drop across the rectifier has been neglected.

Flyback Topology Using N-Channel MOSFETs

A flyback converter using the UCC39421 is shown in Fig 6. It uses a standard two-winding coupled inductor

with a 1:1 turns ratio. The advantage of this topology is that the output voltage can be greater or less than the input voltage, as shown in Table 1. For example, this is ideal for generating 3.3V from a Lithium-Ion cell. Note that RC snubbers are placed across the primary and secondary windings to reduce ringing due to leakage inductance. These are optional, and may not be required in the application.

Note that for converters where V_{IN} and V_{OUT} may both be below 3V, a charge pump is needed to provide adequate gate drive. This is illustrated in the example of Fig. 7.

APPLICATION INFORMATION (cont.)

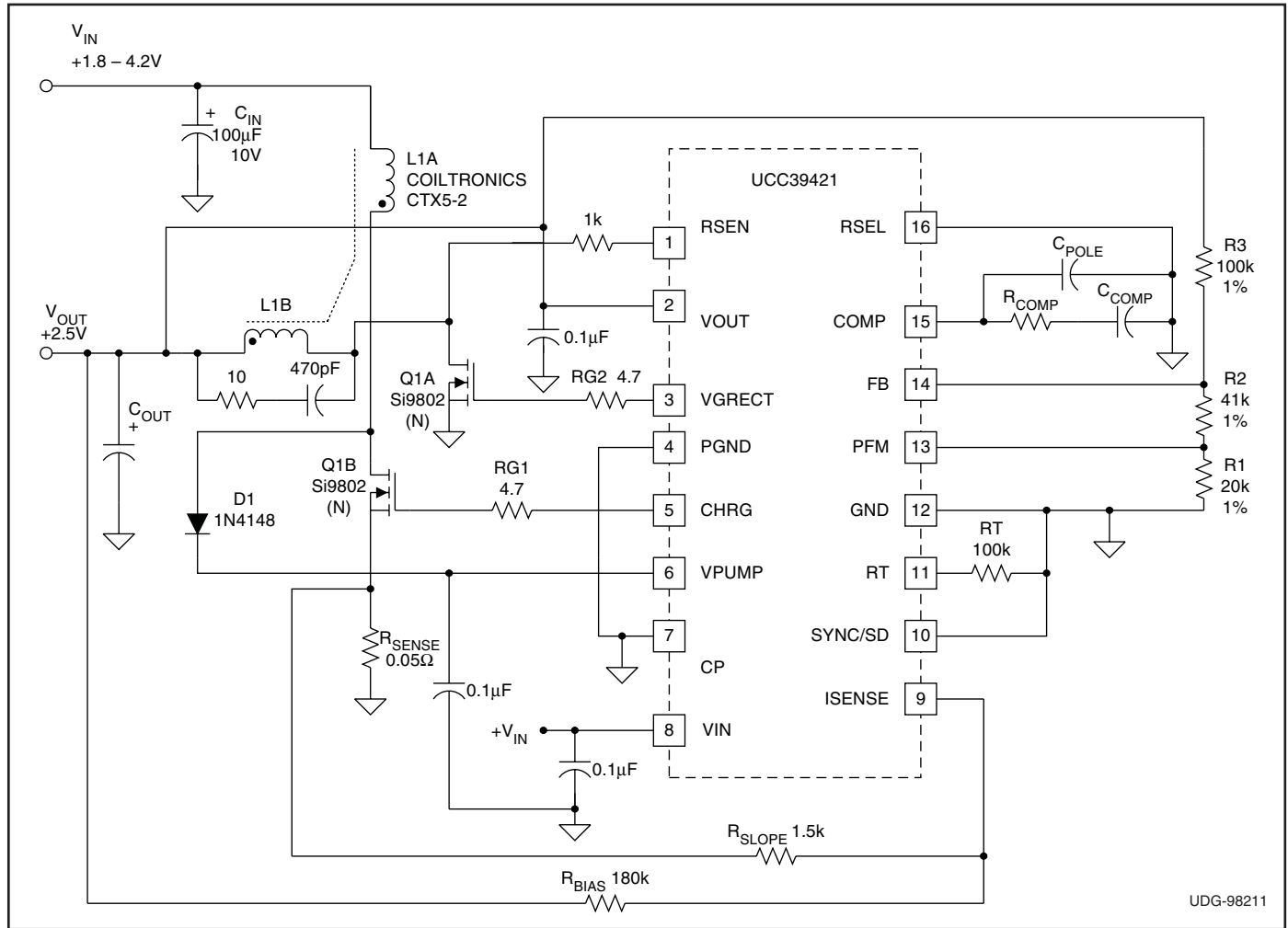


Figure 7. Flyback converter using charge pump input for low voltage operation.

Relating Peak Inductor Current to Average Output Current for the Flyback Converter

For a continuous mode flyback converter, the average output current is related to the peak inductor current by the following:

$$I_{PEAK} = \left(\frac{I_{OUT}}{1-D} \right) + \frac{di}{2} \quad (9)$$

Where D is the duty cycle and the inductor ripple current, di, is defined as:

$$di = \frac{t_{ON} \cdot V_{IN}}{L} = \frac{D \cdot V_{IN}}{f \cdot L} \quad (10)$$

Where f is the switching frequency and L is the inductor value. The duty cycle is defined as:

$$D = \left(\frac{V_O}{V_{IN} + V_O} \right) \quad (11)$$

Substituting equations (10) and (11) into equation (9) yields:

$$I_{PEAK} = \frac{I_O}{\left(1 - \left(\frac{V_O}{V_{IN} + V_O} \right) \right)} + \frac{V_{IN}}{2 \cdot f \cdot L} \cdot \left(\frac{V_O}{V_{IN} + V_O} \right) \quad (12)$$

Figure 7 shows an example of a converter where both V_{IN} and V_{OUT} may be quite low in voltage. In this case, a diode has been added to peak detect the voltage on the drain of the charge FET and use it for the pump input voltage. This is used to drive the gates of the FETs. To assure that the pump voltage will be used (rather than V_{IN} , which may be low), resistor R_{BIAS} has also been added to the I_{SENSE} input to inhibit LP mode. This technique is discussed further in the section about Changing the Low Power Threshold.

APPLICATION INFORMATION (cont.)

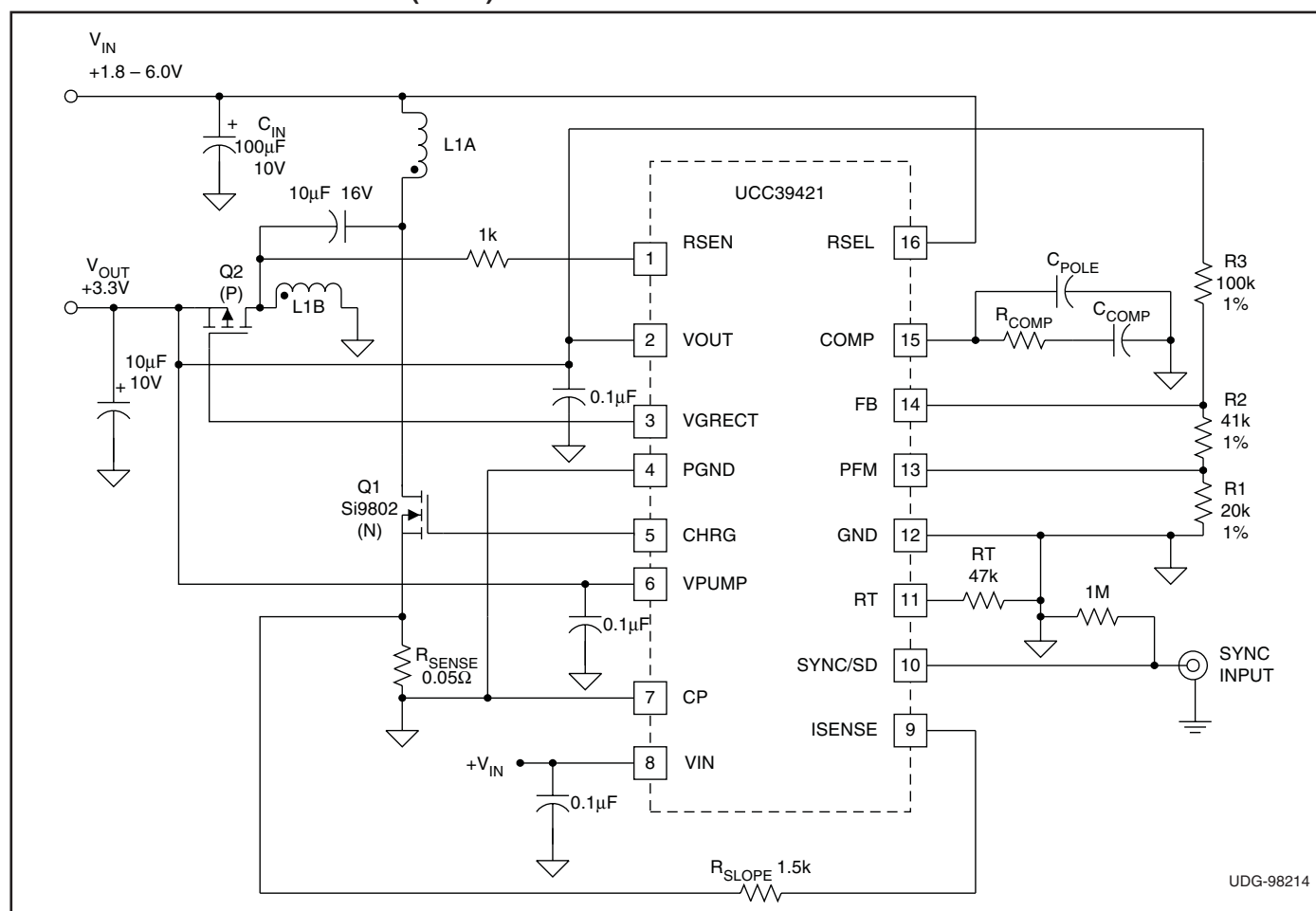


Figure 8. Application diagram for the SEPIC topology using a P-channel synchronous rectifier.

SEPIC Topology Using N & P Channel MOSFETs

The UCC39421 may also be used in the SEPIC (Single Ended Primary Inductance Converter) topology. This topology, which is similar to the flyback, uses a capacitor to aid in energy transfer from input to output. This configuration is shown in Fig 8. The N-channel synchronous rectifier has been changed to a P-channel and moved to the other end of the inductor's secondary winding, and a new capacitor has been placed across the dotted ends of the two windings. The SEPIC topology offers the same advantage of the flyback in that it can generate an output voltage that is greater or less than the input voltage.

However it also offers improved efficiency. Although it requires an additional capacitor in the power stage, it greatly reduces ripple current in the input capacitor and improves efficiency by transferring the energy in the leakage inductance of the coupled inductor to the output. This also provides snubbing for the primary and secondary windings, eliminating the need for RC snubbers. Note that the capacitor must have low ESR, with sufficient ripple current rating for the application. Another advantage of the SEPIC is that the inductors don't have to be on the same core.

APPLICATION INFORMATION (cont.)

PWM Duty Cycle and Slope Compensation

All boost and flyback converters using peak current mode control are susceptible to a phenomenon known as sub-harmonic oscillation when operated in the continuous conduction mode beyond 50% duty cycle. Continuous conduction mode (CCM) means that the inductor current never goes to zero during the switching cycle. For a CCM boost converter, the required duty cycle for a given input and output voltage (neglecting voltage drops across the MOSFET switches) is given by equation (7). This is shown graphically for a number of common output voltages in Fig 9. For example, it can be seen that for a 3.3V output (using the boost topology) slope compensation will not be required because the duty cycle will never exceed 50%.

For the flyback topology, using a coupled inductor with a 1:1 turns ratio, the duty cycle is defined by equation (11). This is shown graphically for a number of common output voltages in Fig. 10.

To prevent sub-harmonic oscillation beyond 50% duty cycle, a technique called slope compensation is used, which modifies the slope of the current ramp. This is accomplished by adding a part of the timing ramp to the current sense input. In the UCC39421 this can be done by simply adding a resistor in series with the ISENSE input. A current is sourced within the IC which is proportional to the internal timing ramp voltage. The value of the resistor will determine the amount of slope compensation added.

The slope compensation output current at the ISENSE pin is equal to:

$$I_{SLOPE} = \frac{1}{R_T} A / \mu \text{sec} \quad (13)$$

where R_T is the timing resistor in Ohms (Ω), The required slope compensation resistor for a boost configuration is given by:

$$R_{SLOPE} = \frac{(V_{OUT} - 2 \cdot V_{IN(min)}) \cdot R_{SENSE} \cdot R_T}{L} \quad (14)$$

where is the current sense resistor value in Ohms (Ω) and L is the inductor value in microHenries (μH), For a flyback topology, using a 1:1 turns ratio, the equation becomes:

$$R_{SLOPE} = \frac{(V_{OUT} - V_{IN(min)}) \cdot R_{SENSE} \cdot R_T}{L} \quad (15)$$

If the converter is operated in the discontinuous conduction mode (inductor current drops to zero), no slope compensation is required. The point at which this mode boundary occurs is a function of switching frequency, input voltage, output voltage, load current and inductor value. However, in general the converter will be more efficient when operated in the continuous conduction mode due to the lower peak currents.

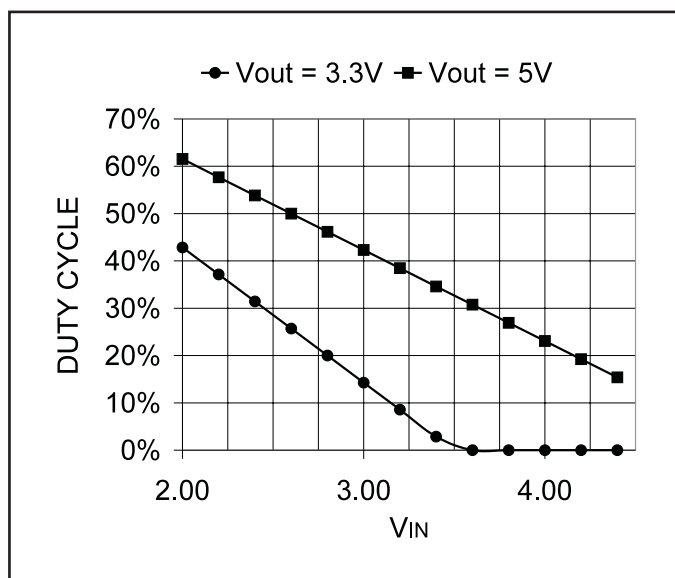


Figure 9. Duty cycle of CCM boost converter as a function of input and output voltage.

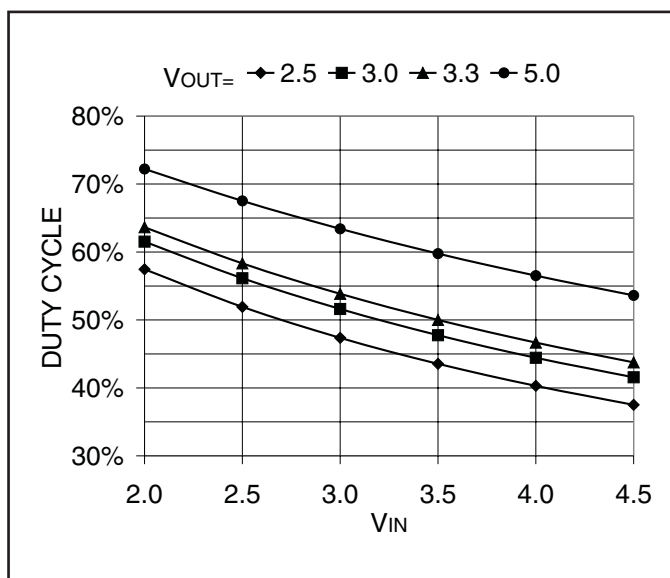


Figure 10. Duty cycle of CCM flyback converter as a function of input and output voltage.

APPLICATION INFORMATION (cont.)

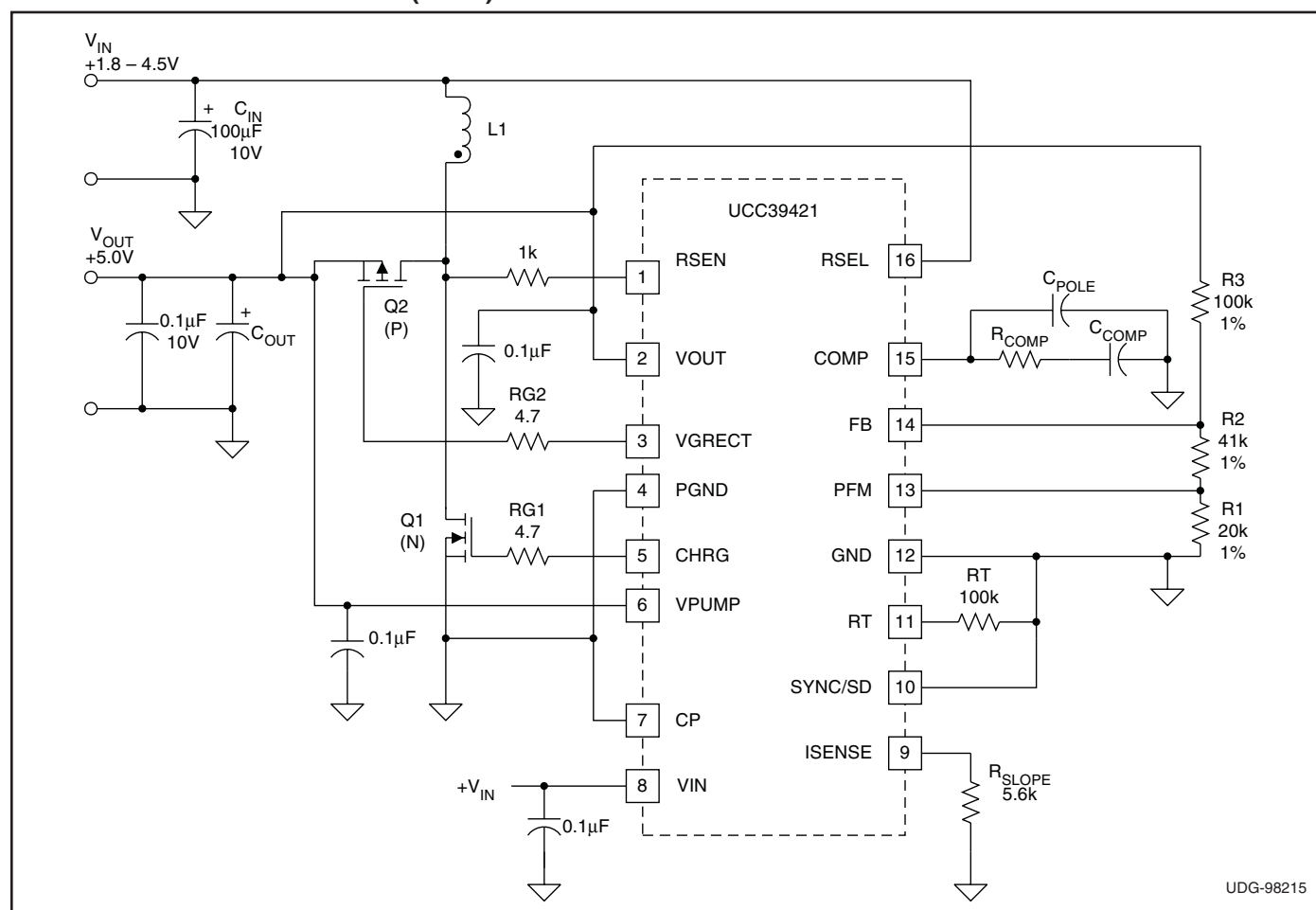


Figure 11. Typical boost configuration using voltage mode control

Voltage Mode Control

The UCC39421 can be operated as a voltage mode controller by connecting a 5.6k resistor from the ISENSE pin to ground. The internal current source will generate an artificial ramp voltage on this input. In this case, no slope compensation is required, and no current sense resistor is required in series with the source of the N-channel MOSFET. A typical application diagram is shown in Fig 11. However, in this configuration there will be no overcurrent protection. In addition, the Pulse and Low Power modes, designed to increase efficiency at light loads, will operate at different load currents. This is because the internal error amplifier's output voltage is no longer a direct function of load current, but rather of duty cycle. When operating in CCM, the duty cycle is largely a function of input and output voltage, not load current. At light enough loads however, the converter will go into discontinuous mode and the error amplifier will drop low enough to activate the Low Power and Pulse modes.

Start Up

The UCC39421 incorporates a unique feature to help it start-up at low input voltages. If the input voltage is below 2.5V at start-up, a separate control circuit takes over until V_{OUT} or V_{PUMP} gets above 2.5V. In this mode, the charge MOSFET is turned on for 5 μ sec, or until the voltage on the ISENSE pin reaches 36mV, whichever occurs first. The charge MOSFET then remains off for a fixed time of 2.5 μ sec, and the body diode of the synchronous rectifier MOSFET is used to supply current to the output. This cycle repeats until either V_{OUT} or V_{PUMP} exceeds 2.5V. This results in constant off time control, with a minimum switching frequency of approximately 120kHz. During this low voltage start-up mode, all other internal circuitry is off, including the synchronous rectifier drive and the slope compensation current source. The peak inductor current during this mode is limited to:

$$I_{PEAK} = \frac{.036}{R_{SENSE}} \quad (13)$$

APPLICATION INFORMATION (cont.)

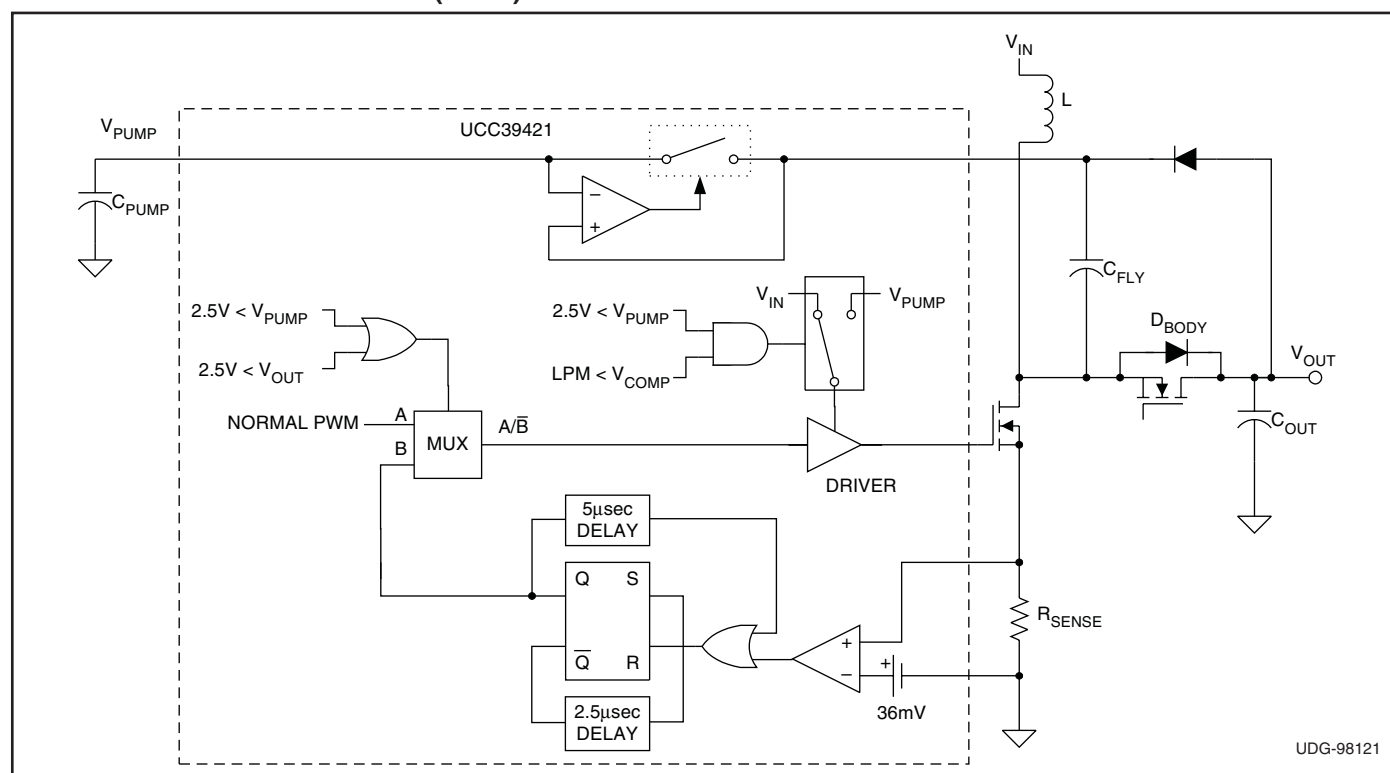


Figure 12. Simplified diagram of low voltage start-up and charge pump control logic.

If input voltages below 2.5V are expected, it is important to use a low voltage logic N-channel MOSFET (with a threshold voltage around 1V or less) to guarantee start-up at full load.

A block diagram of the low voltage start-up logic is shown in Fig 12.

Anti Cross-Conduction and Adaptive Synchronous Rectifier Commutation Logic

When operating in the continuous conduction mode (CCM), the charge MOSFET and the synchronous rectifier MOSFET are simply driven out of phase, so that when one is on the other is off. There is a built-in time delay of about 30nsec to prevent any cross-conduction.

In the event that the converter is operating in the discontinuous conduction mode (DCM), the synchronous rectifier needs to be turned off sooner, when the rectifier current drops to zero. Otherwise, the output will begin to discharge as the current reverses and goes back through the rectifier to the input. (This obviously cannot happen when using a conventional diode rectifier). To prevent this, the UCC39421 incorporates a high speed comparator which senses the voltage on the synchronous rectifier (using the RSEN input) for purposes of commutation. In

the boost and SEPIC topologies, the synchronous rectifier is turned off when the voltage on the RSEN pin goes negative with respect to V_{OUT} . For this reason it is important to have the V_{OUT} pin well decoupled.

In the flyback topology however (using a ground referenced N-channel MOSFET rectifier), the rectifier voltage is sensed on the MOSFET drain, with respect to ground rather than V_{OUT} . The voltage polarity in this case is opposite that of the boost and SEPIC topologies. This problem is solved with the adaptive logic within the UCC39421. During each charge cycle, while the N-channel charge FET is on, a latch is set if the voltage on the RSEN pin exceeds $V_{IN}/2$. This indicates a flyback topology, since this node will be equal to or greater than V_{IN} at this time. In the case of the boost and the SEPIC, the voltage at the RSEN input will be near or below ground, and the latch will not be set. This allows the UCC39421 to sense which topology is in use and adapt the synchronous rectifier commutation logic accordingly. Note that the RSEN input must have a series resistor to limit the current when going below ground. Values less than or equal to 1k are recommended to prevent time delay due to stray capacitance.

APPLICATION INFORMATION (cont.)

Current Sense Amplifier and Leading Edge Blanking

The UCC39421 includes a high speed current sense amplifier with a nominal gain of 10 to minimize losses associated with the current sense resistor. The amplifier was designed to provide good response and minimal propagation delay, allowing switching frequencies over 2MHz. The current sense resistor should be chosen to provide a maximum peak voltage of 100mV at full load, with the minimum input voltage.

A leading edge blanking time of 40nsec is provided to filter out leading edge spikes in the current sense waveform. In most applications, this will eliminate the need for a filter cap on the ISENSE pin.

Overcurrent Protection

The UCC39421 includes a peak current limit function. If the voltage on the ISENSE pin exceeds 0.15V after the initial blanking period, the pulse will be terminated and the charge MOSFET will be turned off.

Sync/Shutdown Input

The SYNC/SD pin has two functions; it may be used to synchronize the UCC39421's switching frequency to an external clock, or to shutdown the IC entirely. In shutdown, the quiescent current is reduced to just a few microamps.

To synchronize the internal clock to an external source, the SYNC/SD pin must be driven high, above 2.0V minimum. The circuitry syncs to the rising edge of the input, the pulse width is not critical.

To shutdown the converter, the SYNC/SD pin must be held high (above 2.0V) for a minimum of 20μsec.

This pin should be grounded if not used.

Changing the Low Power Mode Threshold

For some applications the user may want to lower the Low Power (LP) mode threshold, or even eliminate this feature altogether. For example, if a boost topology is being used, and the input voltage is below 2.5V, the gate drive to the charge FET may want to be derived from the pump (or output) voltage under all load conditions, rather than from V_{IN} . This means the converter would never be allowed to operate in LP mode.

Although the LP mode threshold is internally fixed at 0.5V (referenced to the pin), the point at which the LP mode is entered can be easily modified by adding a single resistor, as shown in Fig 13. Resistor R_{BIAS} forms a divider with R_{SLOPE} (used for slope compensation) and adds a DC offset to the current sense input, raising the output voltage of the sense amplifier and "fooling" the LP mode comparator into thinking the load is higher than it is. The required bias resistor to transition out of LP mode for a given peak current can be calculated using the following equation:

$$R_{BIAS} = \frac{R_{SLOPE} \cdot V_{OUT}}{0.02 - I_{PEAK} \cdot R_{SENSE}} \quad (14)$$

Due to the current sense amplifier gain of 10 and the internal offset of 300mV, an offset of just 20mV or more at the ISENSE pin will inhibit LP mode altogether. Note that inhibiting LP mode does not prevent PFM from working, as long as the PFM pin is set to a voltage higher than:

$$(10 \cdot V_{ISENSE}) + 0.3V \quad (15)$$

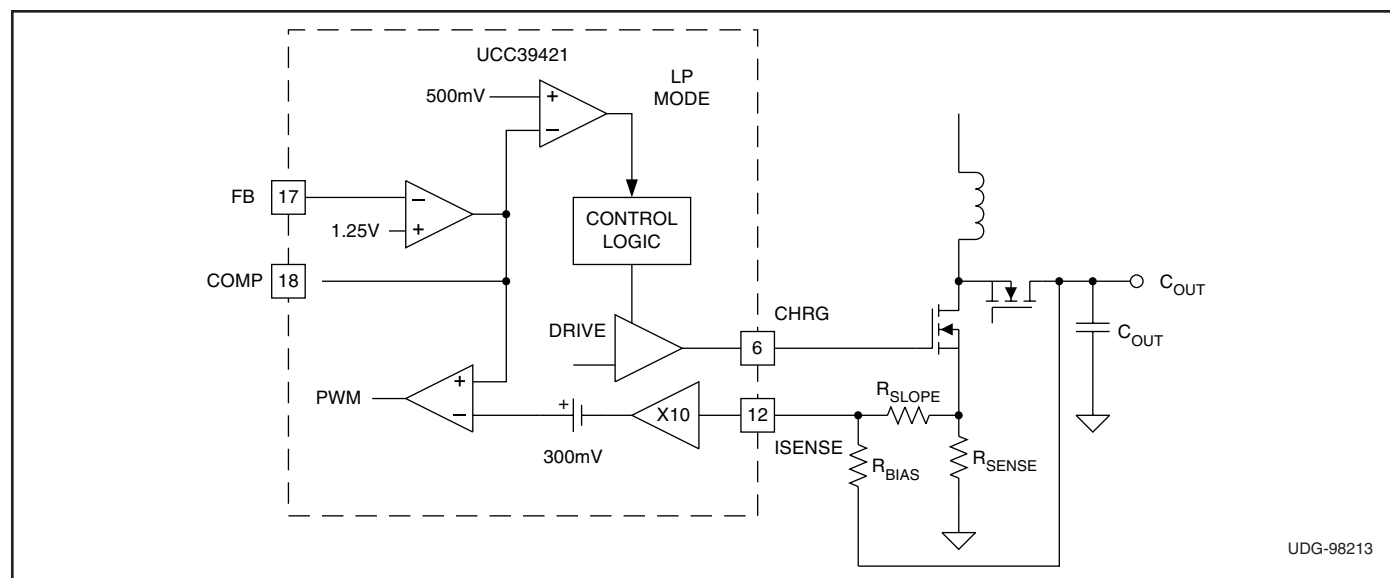


Figure 13. Modifying Low Power (LP) mode threshold.

APPLICATION INFORMATION (cont.)

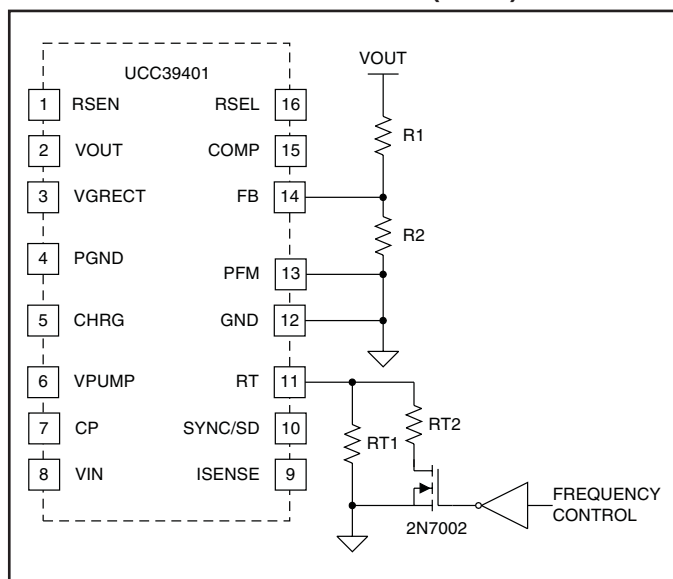


Figure 14. Changing the PWM frequency.

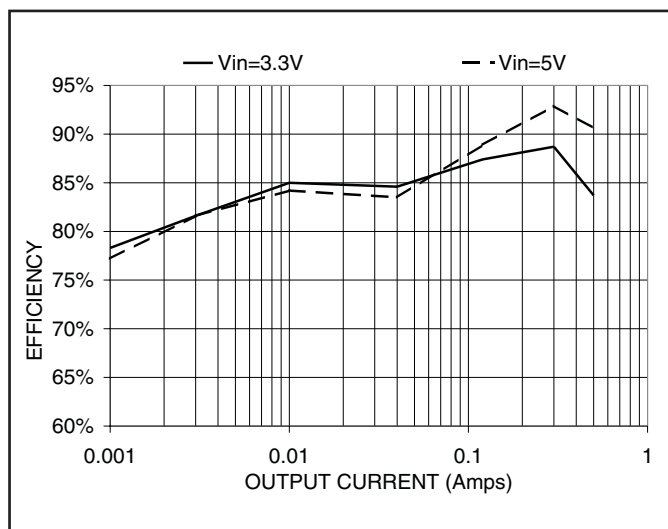


Figure 15. Non-synchronous 12V boost efficiency.
($f=550\text{KHz}$, $L=6.8\mu\text{H}$ DT3316P-682, IRF7601, MBR0530, $\text{VPFM}=0.5\text{V}$)

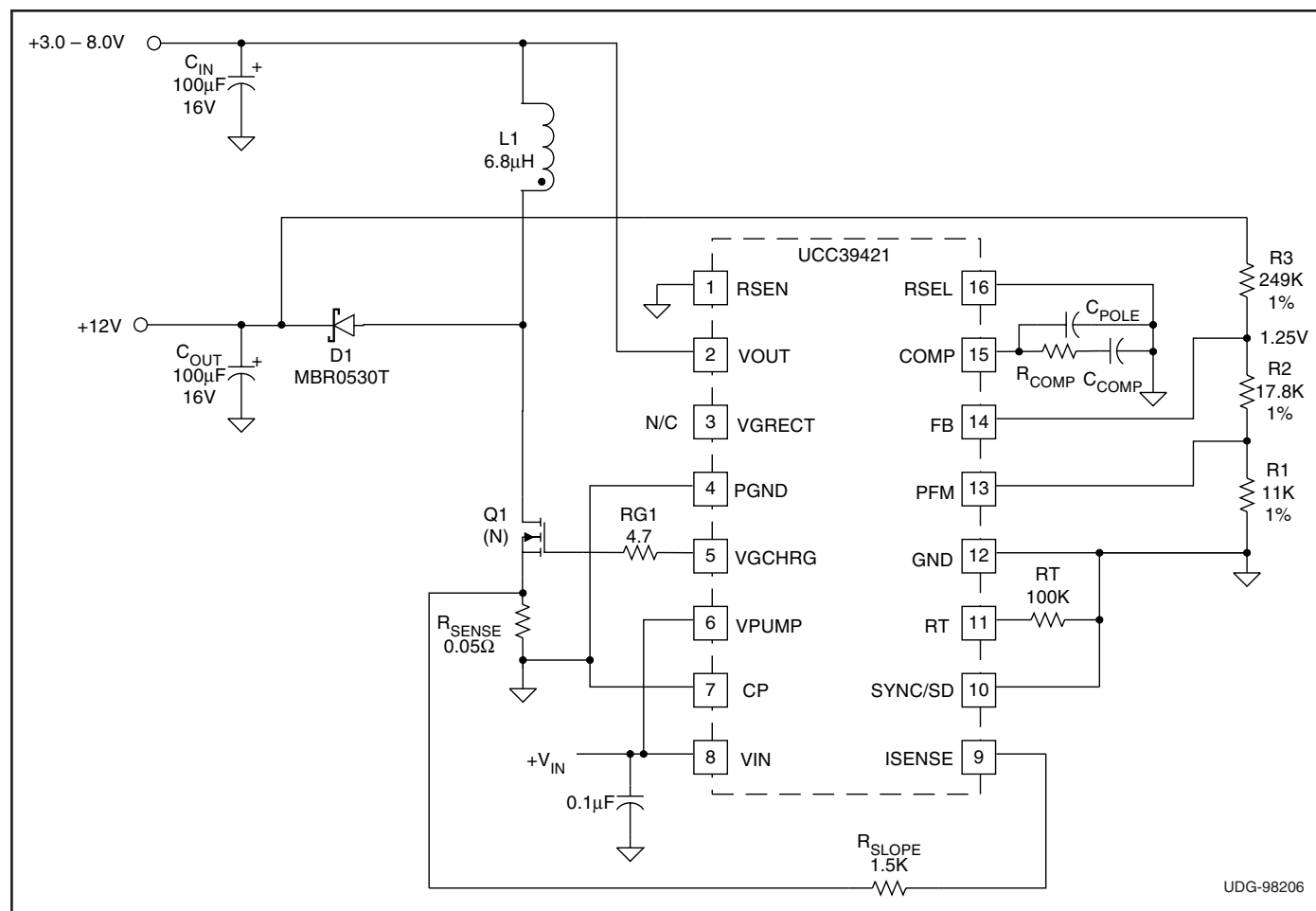


Figure 16. Non-synchronous boost converter for higher output voltages.

APPLICATION INFORMATION (cont.)

Programming the PWM Frequency

Some applications may want to remain in a fixed frequency mode of operation, even at light load, rather than going into PFM mode. This lowers efficiency at light load. One way to improve the efficiency while maintaining fixed frequency operation is to lower the PWM frequency under light load conditions. This can be easily done, as shown in Fig 14. By adding a second timing resistor and a small MOSFET switch, the host can switch between two discrete frequencies at any time.

Non-Synchronous Boost for Higher Output Voltage Applications

The UCC39421 can also be used in a non-synchronous application to provide output voltages greater than 8 volts from low voltage inputs. An example of a 12V boost application is shown in Fig 16. Since none of the IC pins are exposed to the boosted voltage, the output voltage is limited only by the ratings of the external MOSFET, rectifier and filter capacitor. At these higher output voltages, good efficiency is maintained since the rectifier drop is small compared to the output voltage. Note that PFM mode can still be used to maintain high efficiency at light load. Typical efficiency causes are shown in Fig. 15.

Since all the power supply pins (VIN, VOUT, VPUMP) operate off the input voltage, it must be >2.5V and high enough to assure proper gate drive to the charge FET.

UCC39422 Features

The UCC39422 is a 20 pin device which adds a reset function and an uncommitted comparator to the UCC39421. A simplified diagram of the reset circuit is shown in Fig 17.

The reset circuit monitors the voltage at the feedback (FB) pin and issues a reset if the feedback voltage drops below 1.175V. This represents a 6% drop in output voltage. Monitoring the voltage internally at the FB pin eliminates the need for another external voltage divider. The RESET output is an open drain output which is active low during reset. It stays low until the feedback voltage is above 1.175V for a period of time called the reset pulse width, which is user programmable. An external capacitor on the RSADJ pin and an internal 1μA current source determine the reset pulse width, according to the following equation:

$$t_{RESET} \cong C_{RESET} \cdot 1.18 \quad (16)$$

where t_{RESET} is the reset pulse width in seconds, and C_{RESET} is the capacitor value in microFarads (μF).

An adaptive glitch filter is included to prevent nuisance trips. This is implemented using a gm amplifier to charge an 8pF capacitor to 1.175V before declaring a reset. This provides a delay which is inversely proportional to the magnitude of the feedback voltage error. The delay time is approximated by the following equation:

$$t_{DELAY} \cong \frac{0.25}{1.175 - V_{FB}} \mu\text{sec} \quad (17)$$

where t_{DELAY} is the filter delay time in microseconds. Note that the maximum current from the gm amplifier is limited to 2μA, limiting the minimum time delay to 4.8μsec.

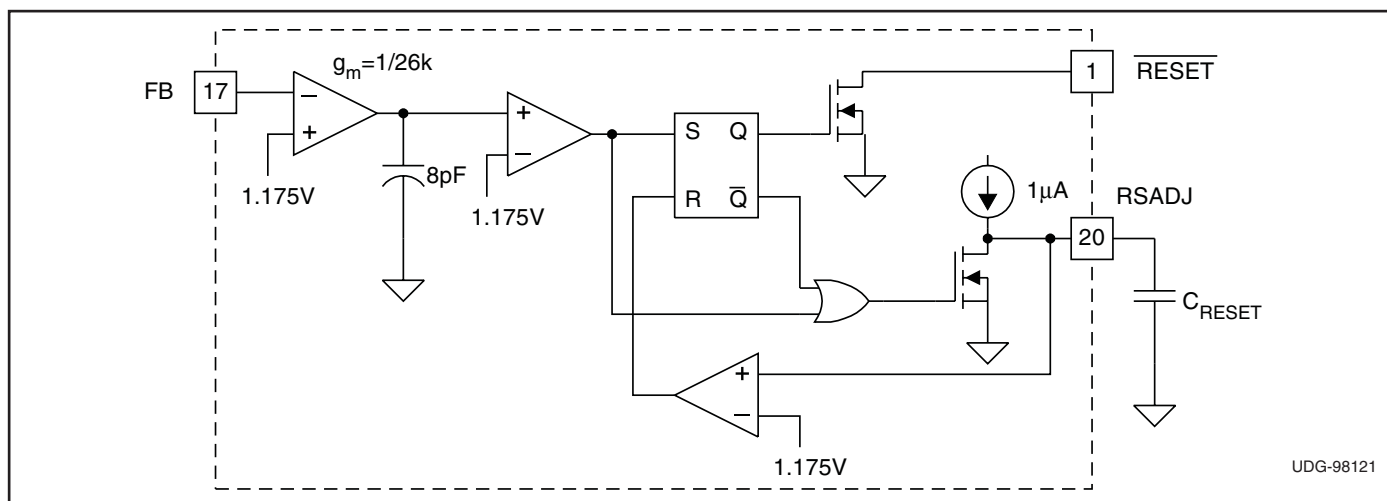


Figure 17. Reset circuitry.

APPLICATION INFORMATION (cont.)

A typical application schematic using the UCC39422 is shown in Fig. 18. In this example, R1 and R2 have been selected to trip the LOWBAT output when V_{IN} drops below 2.0V. Note that the RESET and LOWBAT outputs are open drain and require a pullup.

Selecting the Inductor

The inductor must be chosen based on the desired operating frequency and the maximum load current. Higher frequencies allow the use of lower inductor values, reducing component size. Higher load currents will require larger inductors with higher current ratings and less winding resistance to minimize losses. The inductor must be rated for operation at the highest anticipated peak current. Refer to equations (8) and (12) to calculate the peak inductor current for a boost or flyback design, based on V_{IN} , V_{OUT} , maximum load, frequency and inductor value. Some manufacturers rate their parts for

maximum energy storage in micro-Joules (μJ). This is expressed by:

$$E = 0.5 \cdot L \cdot I_{PEAK}^2 \quad (18)$$

where E is the required energy rating in micro-Joules. L is the inductor value in microHenries (μH) (with current applied), and I_{PEAK} is the peak current in amps that the inductor will see in the application. Another way in which inductor ratings are sometimes specified is the maximum volt-seconds applied. This is given simply by:

$$E \bullet T = \frac{V_{IN} \bullet D}{f} \quad (19)$$

where ET is the required rating in V- μ sec, D is the duty cycle for a given V_{IN} and V_{OUT} , and f is the switching frequency in MHz. Refer to equations (7) and (11) to calculate the duty cycle for a CCM boost or flyback converter.

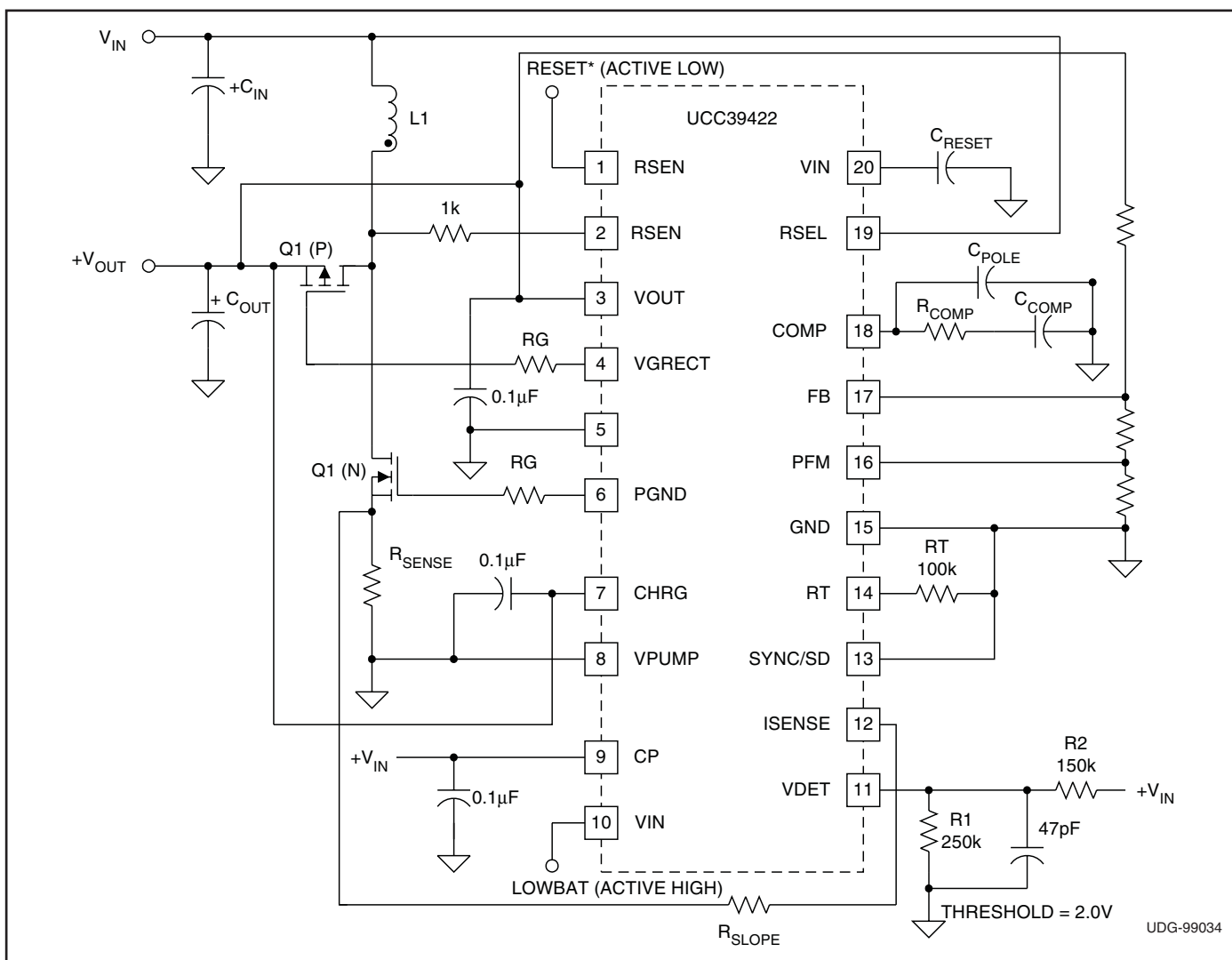


Figure 18. Typical UCC39422 application.

APPLICATION INFORMATION (cont.)

Table III. SMT commercial inductor manufacturers.

Coilcraft Inc. • (800) 322-2645. 1102 Silver Lake RD, Cary, IL 60013
Coiltronics Inc. • (407) 241-7876 6000 Park of Commerce Blvd, Boca Raton, FL 33487
Dale Electronics, Inc. • (605) 665-9301 East Highway 50, Yankton, SD 57078
Pulse Engineering Ltd. • (204) 633-4321 300 Keewatin Street, Winnipeg, MB R2X 2R9
Sumida • Voice (65) 296-3388 • Fax (65) 293-3390 Block 996, Bendemeer Rd., #04-05/06 Singapore 33944
BH Electronics • (612) 894-9590 12219 Wood Lake Drive, Burnsville, MN 55337
Tokin America Inc. • (408) 432-8020 155 Nicholson Lane, San Jose CA 95134

In any case, the inductor must use a low loss core designed for high frequency operation. High frequency ferrite cores are recommended. Some manufacturers of off-the-shelf surface mount designs are listed in Table III. For flyback and SEPIC topologies, use a two winding coupled inductor. SEPIC designs can also use two discrete inductors.

Selecting the Filter Capacitor

The input and output filter capacitors must have low ESR and low ESL. Surface mount tantalum, OSCON or multi-layer ceramics (MLC's) are recommended. The capacitor selected must have the proper ripple current rating for the application. Some recommended capacitor types are listed in Table IV.

Table IV. Recommended SMT Filter Capacitors

Manufacturer	Part Number	Features
AVX	TPS series	Low ESR tantalum
Kemet	T410 series	Low ESR tantalum
Murata	GRM series	Low ESR ceramic
Sanyo	OSCON series	Low ESR organic
Sprague	591D series	Low ESR, low profile tantalum
	594D series	Low ESR tantalum
Tokin	Y5U, Y5V Type	Low ESR ceramic

Circuit Layout and Grounding

As with any high frequency switching power supply, circuit layout, hookup and grounding are critical for proper operation. Although this may be a relatively low power, low voltage design, these issues are still very important. The MOSFET turn-on and turn-off times necessary to maintain high efficiency at high switching frequencies of 1MHz or more result in high dv/dt and di/dt's. This makes stray circuit inductance especially critical. In addition, the high impedances associated with low power designs,

such as in the feedback divider, make them especially susceptible to noise pickup.

Layout

The component layout should be as tight as possible to minimize stray inductance. This is especially true of the high current paths, such as in series with the MOSFETs and the input and output filter caps.

The components associated with the feedback, compensation and timing should be kept away from the power components (MOSFETs, inductor). Keep all components as close to the IC pins as possible. Nodes that are especially noise sensitive are the FB and RT pins. Other sensitive pins are COMP and PFM.

Grounding

A ground plane is highly recommended. The PGND pin of the UCC39421 should be close to the grounded end of the current sense resistor, the input filter cap, and the output filter cap. The GND pin should be close to the grounded end of the RT resistor, the feedback divider resistor, the ISENSE cap (if used), and the compensation network.

MOSFET Gate Resistors

The UCC39421 includes low impedance CMOS output drivers for the two external MOSFET switches. The CHRG output has a nominal resistance of 4Ω, and the RECT has a nominal resistance of 2Ω. For high frequency operation using low gate charge MOSFETs, no gate resistors are required. To reduce high frequency ringing at the MOSFET gates, low value series gate resistors may be added. These should be non-inductive resistors, with a value of 2Ω to 10Ω, depending on the frequency of operation. Lower values will result in better switching times, improving efficiency.

Minimizing Output Ripple and Noise Spikes

The amount of output ripple will be determined primarily by the type of output filter capacitor and how it is connected in the circuit. In most cases, the ripple will be dominated by the ESR (Equivalent Series Resistance) and ESL (Equivalent Series Inductance) of the cap, rather than the actual capacitance value. Low ESR and ESL capacitors are mandatory in achieving low output ripple. Surface mount packages will greatly reduce the ESL of the capacitor, minimizing noise spikes. To further minimize high frequency spikes, a surface mount ceramic capacitor should be placed in parallel with the main filter cap. For best results, a capacitor should be chosen whose self-resonant frequency is near the frequency of the noise spike. For high switch frequencies, ceramic capacitors alone may be used, reducing size and cost.

APPLICATION INFORMATION (cont.)

For applications where the output ripple must be extremely low, a small LC filter may be added to the output. The resonant frequency should be below the selected switching frequency, but above that of any dynamic loads. The filter's resonant frequency is given by:

$$f_{RES} = \frac{1}{2\pi\sqrt{L \bullet C}} \quad (20)$$

Where f is the frequency in Hz, L is the filter inductor value in Henries and C is the filter capacitor value in Farads. It is important to select an inductor rated for the maximum load current and with minimal resistance to re-

duce losses. The capacitor should be a low impedance type, such as a tantalum.

If an LC ripple filter is used, the feedback point can be taken before or after the filter, as long as the filter's resonant frequency is well above the loop crossover frequency. Otherwise the additional phase lag will make the loop unstable. The only advantage to connecting the feedback after the filter is that any small voltage drop across the filter inductor will be corrected for in the loop, providing the best possible voltage regulation. However, the resistance of the inductor is usually low enough that the voltage drop will be negligible.