4-digit LCD car clock

PCF1171C

NAPC/PHILIPS SEMICOND   64E D

FEATURES

- Driving standard 3½ or a 4-digit LCD
- Internal voltage regulator for 5 V LCD
- Option for external stabilized voltage supply
- 4.19 MHz oscillator
- Integrated oscillator output capacitor and polarization resistor
- Operating ambient temperature: −40 to +85 °C
- 40-lead plastic mini-pack (VSO40FD).

GENERAL DESCRIPTION

The PCF1171C is a single chip, 4.19 MHz CMOS clock circuit indicating hours and minutes. It is designed to drive a 3½ or 4-digit liquid crystal display (LCD). Two single-pole, single-throw switches accomplish all time setting functions. A bonding option allows the selection of 12-hour or 24-hour display mode. The circuit is battery-operated via an internal 5 V voltage regulator or by an external stabilized voltage supply.
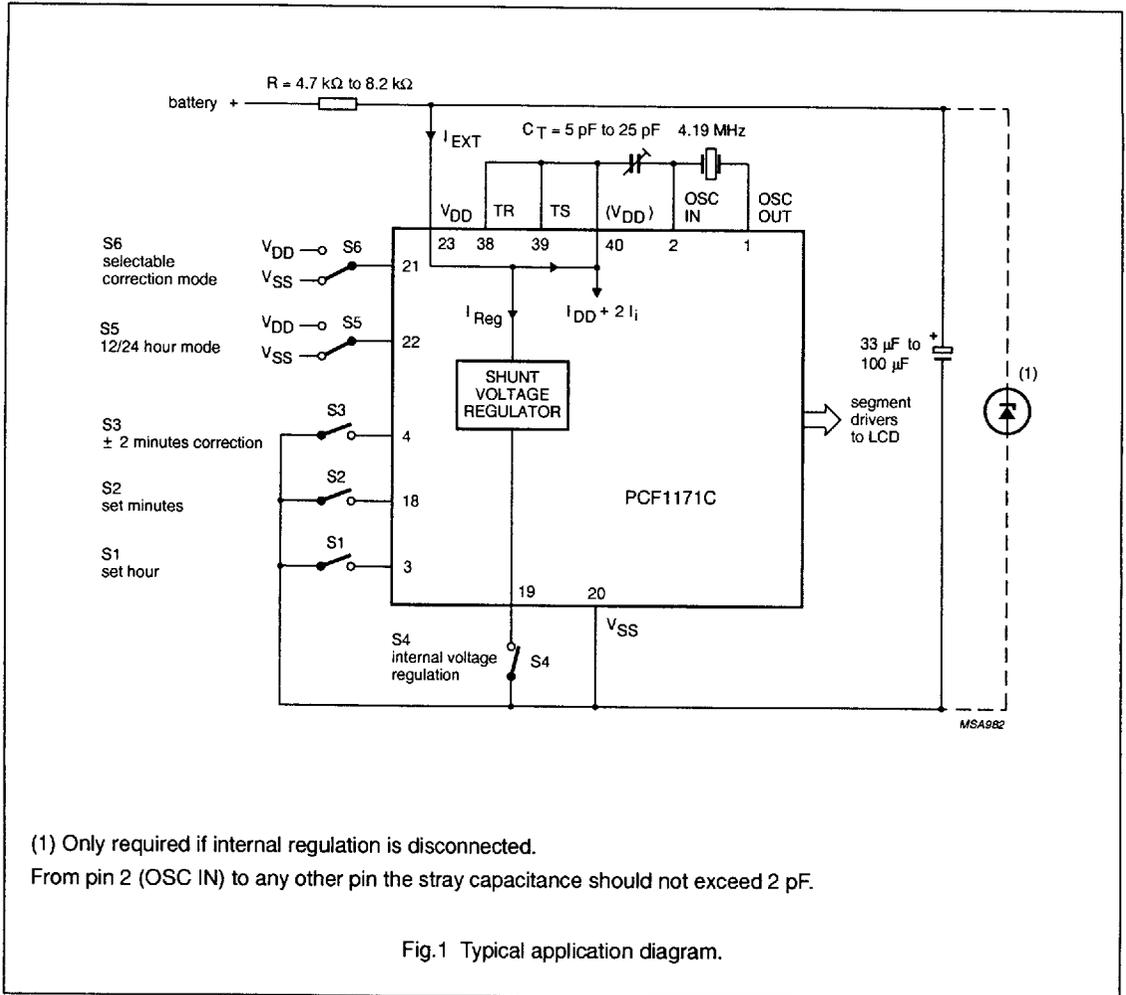
ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF1171CT	40	VSO40FD	plastic	SOT158B
PCF1171CU	–	uncased chip in tray	–	–

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(1) Only required if internal regulation is disconnected.

From pin 2 (OSC IN) to any other pin the stray capacitance should not exceed 2 pF.

Fig.1 Typical application diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
OSC OUT	1	oscillator output
OSC IN	2	oscillator input
S1	3	set hour
S3	4	±2 minute correction
BP	5	64 Hz backplane driver (common of LCD)
ADEG1	6	segment driver
C1	7	segment driver
E2	8	segment driver
D2	9	segment driver
C2	10	segment driver
E3	11	segment driver
D3	12	segment driver
C3	13	segment driver
E4	14	segment driver
D4	15	segment driver
C4	16	segment driver
B4	17	segment driver
S2	18	set minutes
S4	19	internal voltage regulation
V_{SS}	20	negative supply
S6	21	selectable correction mode
S5	22	12/24-hour mode
V_{DD}	23	positive supply
A4	24	segment driver
F4	25	segment driver
G4	26	segment driver
B3	27	segment driver
A3	28	segment driver
F3	29	segment driver
G3	30	segment driver
P1,P2	31	colon flashing
P3,P4	32	colon static
B2	33	segment driver
A2	34	segment driver
F2	35	segment driver
G2	36	segment driver
B1	37	segment driver
TR	38	test reset; connect to (V_{DD})

SYMBOL	PIN	DESCRIPTION
TS	39	test speed-up; connect to (V_{DD})
(V_{DD})	40	positive supply for test and oscillator inputs

Fig.2 Pin configuration.
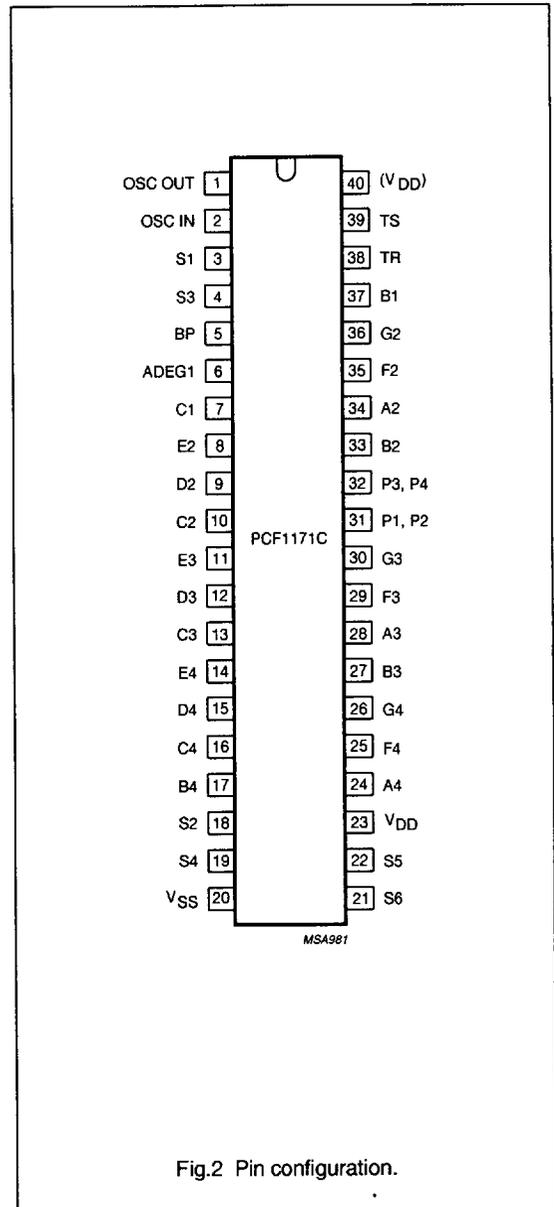
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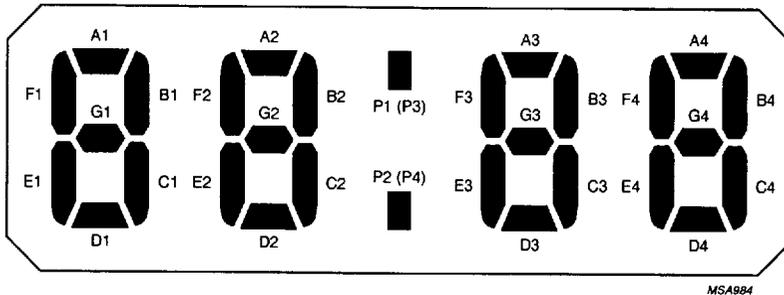
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Fig.3 Segment designation of LCD.

TIME

Fig.4 Display mode.

SWITCH FUNCTIONS

Time set mode

Switch inputs S1, S2 and S3 have an internal pull-up resistor to facilitate use of single-pole, single-throw contacts. A specific debounce circuit is integrated as protection against contact debounce and parasitic voltages.

SWITCH S1

Set hours, S6 selects mode of correction.

SWITCH S2

Set minutes, S6 selects mode of correction. When S2 is closed, in addition to the minute correction, the second counter is set to zero. Release of S2 sets the second counter running.

SWITCHES S1 AND S2

Segment test: if S1 and S2 are pressed simultaneously all LCD segments are switched on. When the switches are released, the clock starts at 1 : 00 in the 12-hour mode or 0 : 00 in the 24-hour mode.

Switch options

SWITCH S3

Time correction ±2 minutes, only operates between 58 minutes 00 seconds and 1 minute 59 seconds. By pressing S3 the clock resets to the full hour with minutes and seconds at zero.

SWITCH S4

Internal regulation: S4 is closed; the internal voltage regulator is active and the voltage supply for the LCD is 5 V.
External regulation: S4 is open, the circuit has to be supplied with an externally regulated voltage.

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SWITCH S5

12-hour display mode: S5 is connected to V_{DD} for 12-hour operation.
24-hour display mode: S5 is connected to V_{SS} for 24-hour operation.

SWITCH S6

Single set correction mode: S6 is connected to V_{DD}; each closure of S1 or S2 advances the counter by one.
Continuous set correction mode: S6 is connected to V_{SS}; each closure of S1 or S2 advances the counter by one and after one second continues with one advance per second until S1 or S2 is released.

Testing

In normal operation the test inputs TR (pin 38) and TS (pin 39) have to be connected to V_{DD} (pin 23). A test frequency (64 Hz) is available at BP (pin 5). The test mode is activated by connecting TS to V_{SS} (pin 20). All output frequencies are then increased by a factor of 65 536. In this mode the maximum input frequency is 100 kHz (external generator at OSC IN). By connecting TR to V_{SS} all counters (seconds, minutes and hours) are stopped. After connecting TR to V_{DD} all counters start from an initial state.

Switch functions also operate in the test mode.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage with respect to V_{SS} with internal regulaton disconnected;	note 1	–	8	V
V_{n-20}	voltage range (any pin)		$V_{SS}-0.3$	$V_{DD}+0.3$	V
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–55	+125	°C

Note

1. Connecting the supply voltage with reverse polarity, will not harm the circuit, provided the current is limited to 10 mA by the external resistor.

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CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C; crystal: f = 4.194304 MHz; R_s = 50 Ω; C_L = 12 pF; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage					
	external regulation		3	–	6	V
	internal regulation	I_{REG} = 1 mA	4	5	6	V
I_{REG}	regulation current with internal regulation		0.2	–	5	mA
I_{DD}	current consumption	all switches open; without LCD; internal regulation disconnected; note 1	50	400	700	μA
r_o	differential internal impedance	I_{REG} = 1 mA	–	–	150	Ω
Oscillator (pins 1 and 2; note 2)						
t_{osc}	start time		–	–	200	ms
$\Delta f/f_{osc}$	frequency stability	ΔV_{DD} = 100 mV	–	0.2×10^{-6}	1×10^{-6}	
R_{fb}	feedback resistance		0.1	–	1	$M\Omega$
C_i	input capacitance		–	–	9	pF
C_o	output capacitance		19	24	29	pF
Switches S1, S2 and S3 (pins 18, 3 and 4) and test inputs, TS, TR (pins 38 and 39)						
I_i	input current	with inputs connected to V_{SS}	50	150	500	μA
t_d	debounce time		32	–	150	ms
R_S	segment driver output resistance	I_L = ±50 μA	–	1	2.5	$k\Omega$
R_{BP}	backplane driver output resistance	I_L = ±250 μA	–	0.2	0.5	$k\Omega$
f_{BP}	backplane driver output frequency		–	64	–	Hz
	LCD DC offset voltage	R_L = 200 kΩ; C_L = 1 nF	–	–	±50	mV

Notes

1. The current I_{EXT} = I_{REG} + I_{DD} + 2 x I_i (+ LCD current).
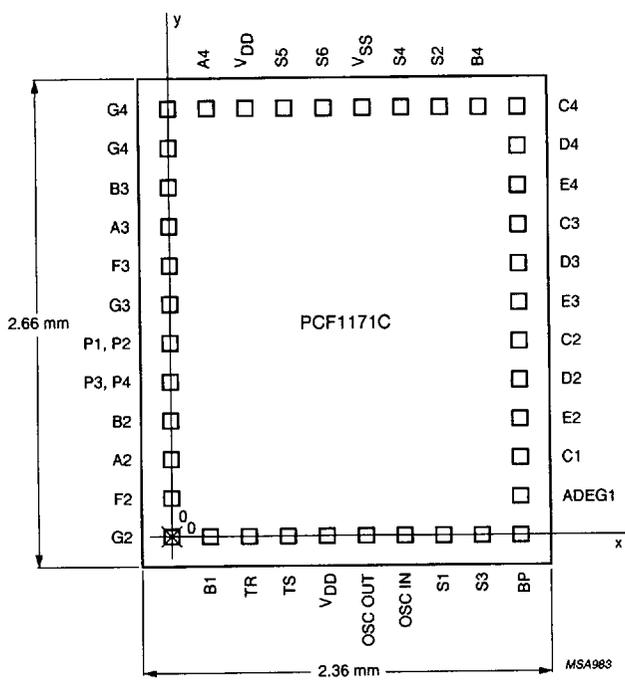2. For correct operation of the oscillator: $V_{DD} \geq 3$ V.

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CHIP DIMENSIONS AND BONDING PAD LOCATIONS

Fig.5 Bonding pad locations; 40 terminals.

Chip area: 6.28 mm².

Bonding pad dimensions: 110 μm x 110 μm.

Chip thickness: 381 ±25 μm.

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Table 1 Bonding pad locations (dimensions in μm).
All x/y coordinates are referenced to the pad G2, see Fig.5.

PAD	X	Y	PAD	X	Y
OSC OUT	1060	0	S6	860	2320
OSC IN	1260	0	S5	660	2320
S1	1460	0	V_{DD}	460	2320
S3	1680	0	A4	240	2320
BP	1920	0	F4	0	2320
ADEG1	1920	240	G4	0	2080
C1	1920	460	B3	0	1860
E2	1920	660	A3	0	1660
D2	1920	860	F3	0	1460
C2	1920	1060	G3	0	1260
E3	1920	1260	P1,P2	0	1060
D3	1920	1460	P3,P4	0	860
C3	1920	1660	B2	0	660
E4	1920	1860	A2	0	460
D4	1920	2080	F2	0	240
C4	1920	2320	G2	0	0
B4	1680	2320	B1	240	0
S2	1460	2320	TR	460	0
S4	1260	2320	TS	660	0
V_{SS}	1060	2320	V_{DD}	860	0
chip corner (max. value)	−220	−170			