

NL27WZ125

Dual Buffer with 3-State Outputs

The NL27WZ125 is a high performance dual noninverting buffer operating from a 1.65 V to 5.5 V supply.

Features

- Extremely High Speed: t_{PD} 2.6 ns (typical) at $V_{CC} = 5$ V
- Designed for 1.65 V to 5.5 V V_{CC} Operation
- Over Voltage Tolerant Inputs and Outputs
- LVTTL Compatible – Interface Capability With 5 V TTL Logic with $V_{CC} = 3$ V
- LVC MOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current Substantially Reduces System Power Requirements
- 3-State OE Input is Active-Low
- Replacement for NC7WZ125
- Chip Complexity = 72 FETs
- Pb-Free Package is Available

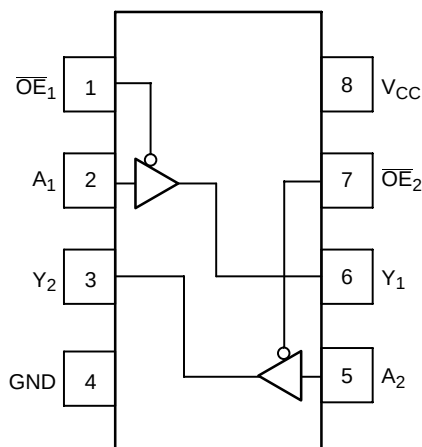


Figure 1. Pinout (Top View)

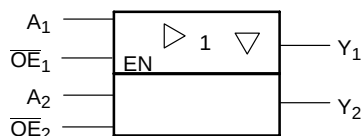


Figure 2. Logic Symbol



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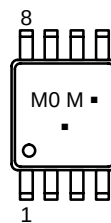
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US8
US SUFFIX
CASE 493

MARKING DIAGRAM



M0 = Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

PIN ASSIGNMENT

Pin	Function
1	$\overline{OE}_1$
2	A_1
3	Y_2
4	GND
5	A_2
6	Y_1
7	$\overline{OE}_2$
8	V_{CC}

FUNCTION TABLE

Input		Output
$\overline{OE}_n$	A_n	Y_n
L	L	L
L	H	H
H	X	Z

X = Don't Care
n = 1, 2

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

NL27WZ125

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type	Tape and Reel Size†
	Logic Circuit Indicator	No. of Gates per Package	Temp Range Identifier	Technology	Device Function	Package Suffix		
NL27WZ125US	NL	2	7	WZ	125	US	US8	178 mm, 3000 Unit
NL27WZ125USG	NL	2	7	WZ	125	US	US8 (Pb-Free)	178 mm, 3000 Unit

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	− 0.5 to + 7.0	V
V_I	DC Input Voltage	− 0.5 to + 7.0	V
V_O	DC Output Voltage Output in High Impedance State Output in HIGH or LOW State	− 0.5 to + 7.0 − 0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current $V_I < GND$	− 50	mA
I_{OK}	DC Output Diode Current $V_O < GND$	− 50	mA
I_O	DC Output Sink Current	± 50	mA
I_{CC}	DC Supply Current per Supply Pin	± 100	mA
I_{GND}	DC Ground Current per Ground Pin	± 100	mA
T_{STG}	Storage Temperature Range	− 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T_J	Junction Temperature under Bias	+ 150	°C
θ_{JA}	Thermal Resistance (Note 1)	250	°C/W
P_D	Power Dissipation in Still Air at 85°C	250	mW
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage Operating Data Retention Only	1.65 1.5	5.5 5.5	V
V_I	Input Voltage (Note 5)	0	5.5	V
V_O	Output Voltage (HIGH or LOW State)	0	5.5	V
T_A	Operating Free-Air Temperature	− 40	+ 85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate $V_{CC} = 2.5 V \pm 0.2 V$ $V_{CC} = 3.0 V \pm 0.3 V$ $V_{CC} = 5.0 V \pm 0.5 V$	0 0 0	20 10 5	ns/V

5. Unused inputs may not be left open. All inputs must be tied to a high- or low-logic input voltage level.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			–40°C ≤ T _A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	High-Level Input Voltage		1.65 2.3 to 5.5	0.75 V _{CC} 0.7 V _{CC}			0.75 V _{CC} 0.7 V _{CC}		V
V _{IL}	Low-Level Input Voltage		1.65 2.3 to 5.5			0.25 V _{CC} 0.3 V _{CC}		0.25 V _{CC} 0.3 V _{CC}	V
V _{OH}	High-Level Output Voltage V _{IN} = V _{IL} or V _{IH}	I _{OH} = 100 μA I _{OH} = –3 mA I _{OH} = –8 mA I _{OH} = –12 mA I _{OH} = –16 mA I _{OH} = –24 mA I _{OH} = –32 mA	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5	V _{CC} – 0.1 1.29 1.9 2.2 2.4 2.3 3.8	V _{CC} 1.52 2.1 2.4 2.7 2.5 4.0		V _{CC} – 0.1 1.29 1.9 2.2 2.4 2.3 3.8		V
V _{OL}	Low-Level Output Voltage V _{IN} = V _{IL}	I _{OL} = 100 μA I _{OL} = 3 mA I _{OL} = 8 mA I _{OL} = 12 mA I _{OL} = 16 mA I _{OL} = 24 mA I _{OL} = 32 mA	1.65 to 5.5 2.3 2.7 3.0 3.0 4.5		0.08 0.20 0.22 0.28 0.38 0.42	0.1 0.24 0.3 0.4 0.4 0.55 0.55		0.1 0.24 0.3 0.4 0.4 0.55 0.55	V
I _{IN}	Input Leakage Current	V _{IN} = V _{CC} or GND	5.5			±0.1		±1.0	μA
I _{OFF}	Power Off Leakage Current	V _{OUT} = 5.5 V V _{IN} = 5.5 V	0			1.0		10	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			1.0		10	μA
I _{OZ}	3-State Output Leakage	V _{IN} = V _{IL} or V _{IH} 0V ≤ V _{OUT} ≤ 5.5 V	2.3 to 5.5			±0.5		±5	μA

AC ELECTRICAL CHARACTERISTICS (t_R = t_F = 3.0 ns)

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			–40°C ≤ T _A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay AN to YN (Figures 3 and 4)	R _L = 1 MΩ C _L = 15 pF	1.8 ± 0.15 2.5 ± 0.2	2.0 1.0		12 7.5	2.0 1.0	13 8	ns
		R _L = 1 MΩ C _L = 15 pF	3.3 ± 0.3	0.8		5.2	0.8	5.5	
		R _L = 500 Ω C _L = 50 pF		1.2		5.7	1.2	6.0	
		R _L = 1 MΩ C _L = 15 pF	5.0 ± 0.5	0.5		4.5	0.5	4.8	
		R _L = 500 Ω C _L = 50 pF		0.8		5.0	0.8	5.3	
t _{OSLH} t _{OSHL}	Output to Output Skew (Note 6)	R _L = 500 Ω C _L = 50 pF	3.3 ± 0.3			1.0		1.0	ns
		R _L = 500 Ω C _L = 50 pF	5.0 ± 0.5			0.8		0.8	
t _{PZH} t _{PZL}	Output Enable Time (Figures 5, 6 and 7)		1.8 ± 0.15 2.5 ± 0.2	3.0 1.8		14 8.5	3.0 1.8	15 9.0	ns
			3.3 ± 0.3	1.2		6.2	1.2	6.5	
			5.0 ± 0.5	0.8		5.5	0.8	5.8	
t _{PHZ} t _{PLZ}	Output Enable Time (Figures 5, 6 and 7)		1.8 ± 0.15 2.5 ± 0.2	2.5 1.5		12 8.0	2.5 1.5	13 8.5	ns
			3.3 ± 0.3	0.8		5.7	0.8	6.0	
			5.0 ± 0.5	0.3		4.7	0.3	5.0	

6. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. This specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	$V_{CC} = 5.5 \text{ V}$, $V_I = 0 \text{ V}$ or V_{CC}	7.0	pF
C_{OUT}	Output Capacitance	$V_{CC} = 5.5 \text{ V}$, $V_I = 0 \text{ V}$ or V_{CC}	7.0	pF
C_{PD}	Power Dissipation Capacitance (Note 7)	10 MHz, $V_{CC} = 3.3 \text{ V}$, $V_I = 0 \text{ V}$ or V_{CC} 10 MHz, $V_{CC} = 5.5 \text{ V}$, $V_I = 0 \text{ V}$ or V_{CC}	18 27	pF

7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

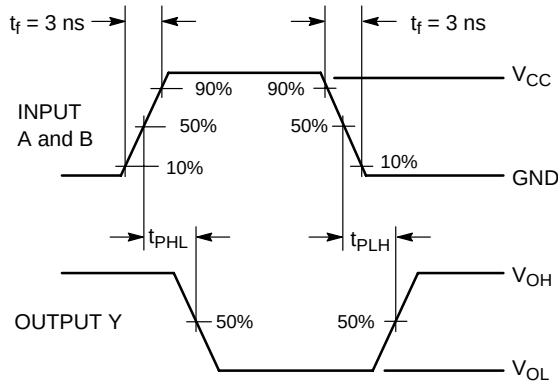
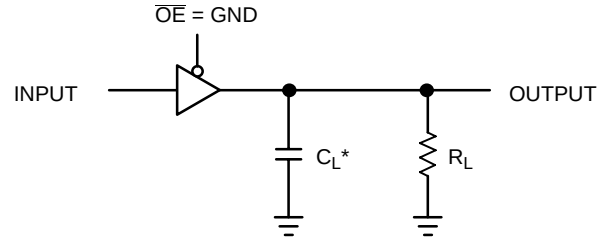


Figure 3. Switching Waveform



*Includes all probe and jig capacitance.
A 1 MHz square input wave is recommended for propagation delay tests.

Figure 4. T_{PLH} or T_{PHL}

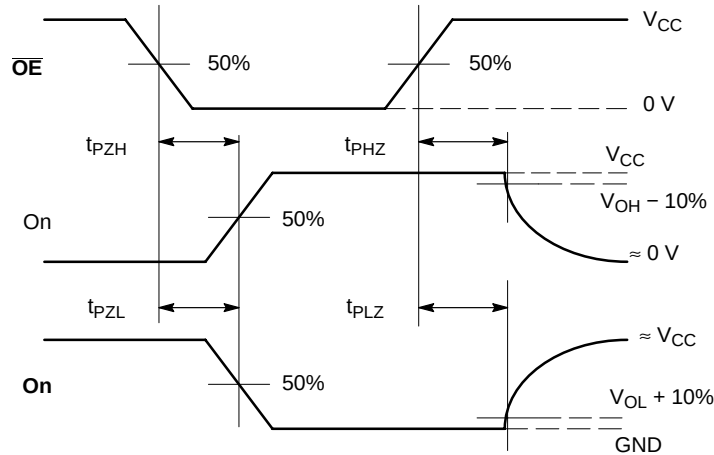
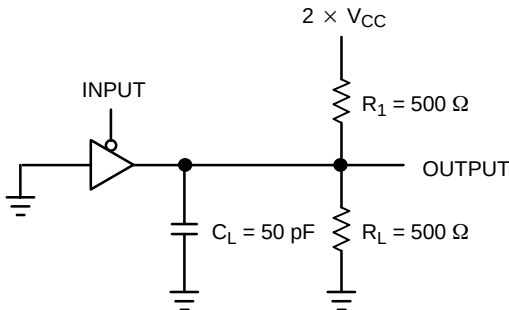
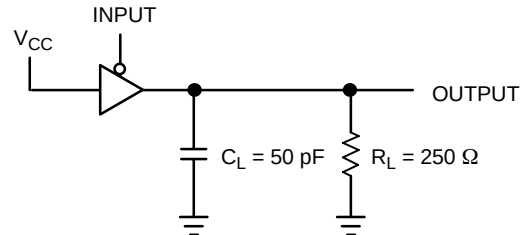


Figure 5. AC Output Enable and Disable Waveform



A 1 MHz square input wave is recommended for propagation delay tests.

Figure 6. T_{PZL} or T_{PL}



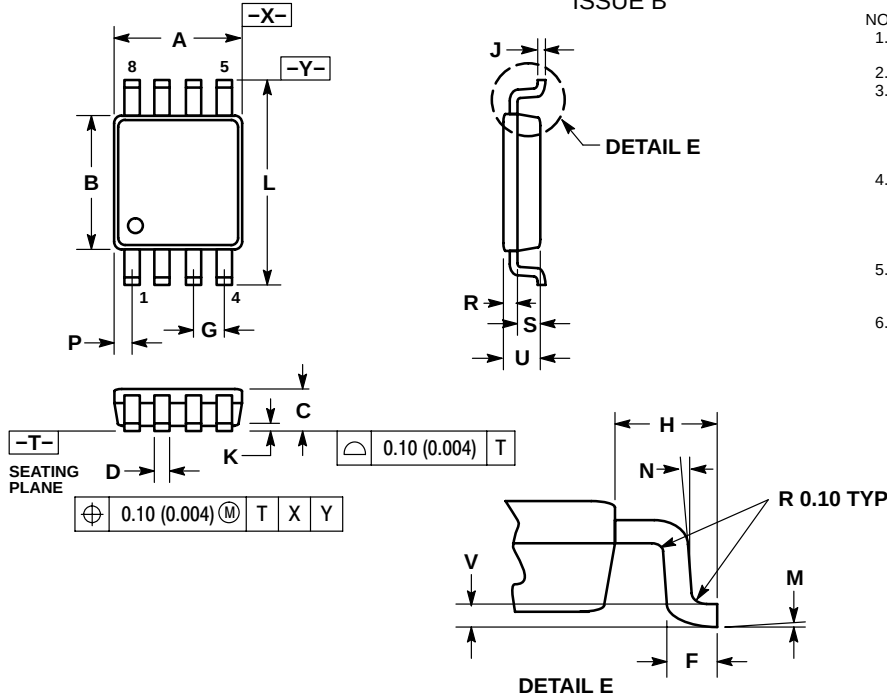
A 1 MHz square input wave is recommended for propagation delay tests.

Figure 7. T_{PZH} or T_{PHZ}

NL27WZ125

PACKAGE DIMENSIONS

US8
US SUFFIX
CASE 493-02
ISSUE B

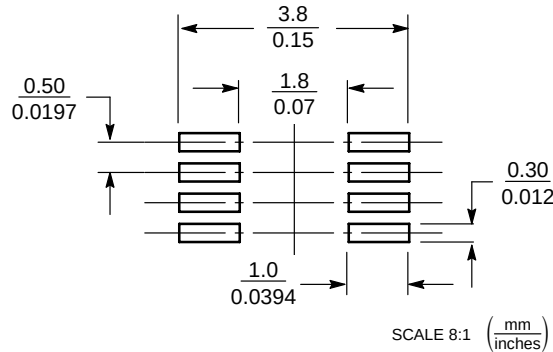


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION "A" DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR. MOLD FLASH, PROTRUSION AND GATE BURR SHALL NOT EXCEED 0.140 MM (0.0055") PER SIDE.
4. DIMENSION "B" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSION. INTER-LEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.140 (0.0055") PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076-0.0203 MM. (300-800 °).
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED ± 0.0508 (0.002 °).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.90	2.10	0.075	0.083
B	2.20	2.40	0.087	0.094
C	0.60	0.90	0.024	0.035
D	0.17	0.25	0.007	0.010
F	0.20	0.35	0.008	0.014
G	0.50 BSC		0.020 BSC	
H	0.40 REF		0.016 REF	
J	0.10	0.18	0.004	0.007
K	0.00	0.10	0.000	0.004
L	3.00	3.20	0.118	0.126
M	0 °	6 °	0 °	6 °
N	5 °	10 °	5 °	10 °
P	0.23	0.34	0.010	0.013
R	0.23	0.33	0.009	0.013
S	0.37	0.47	0.015	0.019
U	0.60	0.80	0.024	0.031
V	0.12 BSC		0.005 BSC	

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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