

CMOS Logic MN4000B Series

6932852 PANASONIC INDL/ELECTRONIC

MN4046B/MN4046BS

66C 05012 D T-50-17

MN4046B / MN4046BS**Phase-Locked Loops****Description**

This MN4046B/S are phase-locked loop circuits composed of two phase comparators, VCO, source follower and zener diode. The two comparators have common signal inputs $SIGN_{IN}$ and $COMP_{IN}$.

$SIGN_{IN}$ should be used by directly connecting to large voltage signals or by connecting small voltage signal through serial capacitors.

Small voltage signals are adjusted to the linear area of the amplifier by the self-bias circuit.

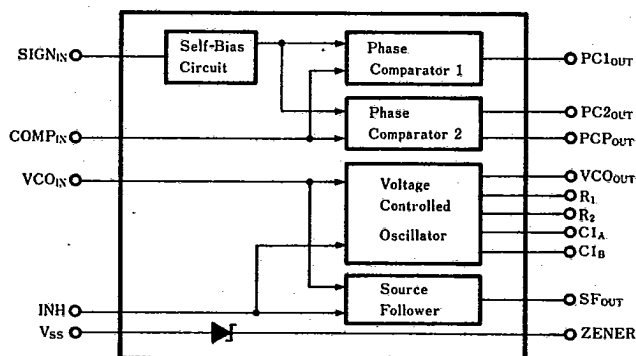
Phase comparator 1 is an Exclusive-OR gate which outputs digital error signal $PC1_{OUT}$, and shifts phase by 90° with the central frequency between $SIGN_{IN}$ signal and $COMP_{IN}$ signal (50% duty cycle).

Phase comparator 2 outputs digital error signals $PC2_{OUT}$ and PCP_{OUT} and phase shifts between $SIGN_{IN}$ and $COMP_{IN}$ (duty cycle is arbitrary) is 0° .

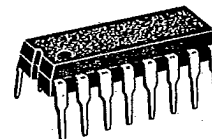
The frequency of signal VCO_{OUT} obtained by the linear VCO is defined by the voltage of input VCO_{IN} and the constant of the resistor and capacitor connected to R_1 , R_2 , $C1A$ and $C1B$.

When VOC_{IN} signal is necessary and there is no space for loading, source follower output SF_{OUT} together with an external resistor is used. When inhibit input INH is "1" level, stand-by power dissipation can be minimized because the VCO and source follower are disabled.

A zener diode should be used to adjust the power supply source. The MN4046B/S can be widely used for modulation and demodulation of FM and FSK, composition and discrimination of frequencies, tone decoding, synchronization and adjustment of data, and conversion of voltage and frequencies.

Block Diagram

P-3

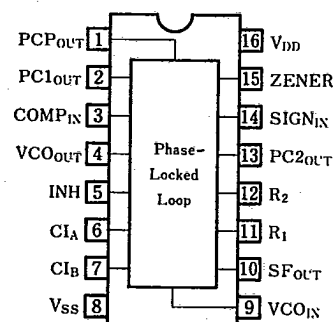


16-Pin • Plastic DIL Package

P-4



16-Pin • Panaflat Package (SO-16D)

Pin Configuration

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■ Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Unit
Supply Voltage	V_{DD}	-0.5~+18	V
Input Voltage	V_I	-0.5~ $V_{DD}+0.5^*$	V
Output Voltage	V_O	-0.5~ $V_{DD}+0.5^*$	V
Peak Input · Output Current	$\pm I_I$	max. 10	mA
Power Dissipation (per package)	P_D	max. 400 Decrease up to 200mW rating at 8mW/°C	mW
Power Dissipation (per output terminal)	P_D	max. 100	mW
Operating Ambient Temperature	T_{opr}	-40~+85	°C
Storage Temperature	T_{stg}	-65~+150	°C

* $V_{DD} + 0.5V$ should be under 18V■ DC Characteristics ($V_{SS}=0V$)

Item	V_{DD} (V)	Sym- bol	Conditions	Ta=-40°C		Ta=25°C		Ta=85°C		Unit
				min.	max.	min.	max.	min.	max.	
Quiescent Power Supply Current	5	I_{DD}	INH = H, SIGN _{IN} = H	—	20	—	20	—	150	μA
	10			—	40	—	40	—	300	
	15			—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	$V_I = V_{SS}$ or V_{DD} $ I_O < 1\mu A$	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	$V_I = V_{SS}$ or V_{DD} $ I_O < 1\mu A$	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$ I_O < 1\mu A$ $V_O = 0.5V$ or $4.5V$ $V_O = 1V$ or $9V$ $V_O = 1.5V$ or $13.5V$	—	1.5	—	1.5	—	1.5	V
	10			—	3	—	3	—	3	
	15			—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$ I_O < 1\mu A$ $V_O = 0.5V$ or $4.5V$ $V_O = 1V$ or $9V$ $V_O = 1.5V$ or $13.5V$	3.5	—	3.5	—	3.5	—	V
	10			7	—	7	—	7	—	
	15			11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	$V_O = 0.4V$, $V_I = 0$ or $5V$ $V_O = 0.5V$, $V_I = 0$ or $10V$ $V_O = 1.5V$, $V_I = 0$ or $15V$	0.52	—	0.44	—	0.36	—	mA
	10			1.3	—	1.1	—	0.9	—	
	15			3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	$V_O = 4.6V$, $V_I = 0$ or $5V$ $V_O = 9.5V$, $V_I = 0$ or $10V$ $V_O = 13.5V$, $V_I = 0$ or $15V$	0.52	—	0.44	—	0.36	—	mA
	10			1.3	—	1.1	—	0.9	—	
	15			3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	$V_O = 2.5V$, $V_I = 0$ or $5V$	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	$V_I = 0$ or $15V$	—	0.3	—	0.3	—	1	μA
Input Capacitance		C_I		—	—	—	7.5	—	—	pF

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■ Electrical Characteristics

- Switching Characteristics ($T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{V}$, $C_L = 50\text{pF}$)

Item	V_{DD} (V)	Symbol	Condition	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}		—	60	180	ns
	10			—	30	90	
	15			—	20	60	
Output Fall Time	5	t_{THL}		—	60	180	ns
	10			—	30	90	
	15			—	20	60	

● Phase · Comparator

Item	V_{DD} (V)	Symbol	Condition	min.	typ.	max.	Unit
Input Resistance	5	R_{IN}		—	750	—	$k\Omega$
	10			—	220	—	
	15			—	140	—	
	15	$COMP_{IN}$		—	—	—	
Minimum Input Sensitivity	5	V_{IN}	AC Couple-SIGN _{IN}	—	150	—	mV _{P-P}
	10		$R_1 = 10k\Omega$, $R_2 = \infty$	—	150	—	
	15		$C_1 = 100\text{pF}$	—	200	—	
DC Couple-SIGN _{IN} : COMP _{IN} Low Level	5	V_{IL}		—	—	1.5	V
	10			—	—	3	
	15			—	—	4	
DC Couple-SIGN _{IN} : COMP _{IN} High Level	5	V_{IH}		3.5	—	—	V
	10			7	—	—	
	15			11	—	—	

● Voltage Control Oscillator

Item	V _{DD} (V)	Symbol	Condition		min.	typ.	max.	Unit
Maximum Frequency	5	f _{max}	VCO _{IN} = V _{DD}		0.5	1	—	MHz
	10		R ₁ = 10kΩ, R ₂ = ∞		1	2	—	
	15		C ₁ = 50pF		1.3	2.7	—	
Temperature-Frequency Stability	5		R ₂ = ∞		—	0.12	—	% / °C
	10				—	0.04	—	
	15				—	0.015	—	
Linearity	5	R ₂ = ∞		VCO _{IN} = 2.50V ± 0.30V R ₁ > 10kΩ	—	0.50	—	%
	10			VCO _{IN} = 5.00V ± 2.50V R ₁ > 400kΩ	—	0.25	—	
	15			VCO _{IN} = 7.50V ± 5.00V R ₁ = 1MΩ	—	0.25	—	
Output Duty Cycle	5 ~ 15	δ			—	50	—	%
Input Resistance (VCO _{IN})	5 ~ 15	R _{IN}			—	10 ⁶	—	MΩ

● Source · Follower

Item	V_{DD} (V)	Symbol	Condition	min.	typ.	max.	Unit
Offset Voltage	5		$VCO_{IN} - SF_{OUT}$	—	1.5	—	V
	10		$R_{SF} = 50k\Omega$	—	1.7	—	
	15			—	1.8	—	
Linearity	5		$VCO_{IN} = 2.50V \pm 0.30V$, $R_{SF} > 50k\Omega$	—	0.3	—	%
	10		$VCO_{IN} = 5.00V \pm 2.50V$, $R_{SF} > 50k\Omega$	—	1.0	—	
	15		$VCO_{IN} = 7.50V \pm 5.00V$, $R_{SF} > 50k\Omega$	—	1.3	—	

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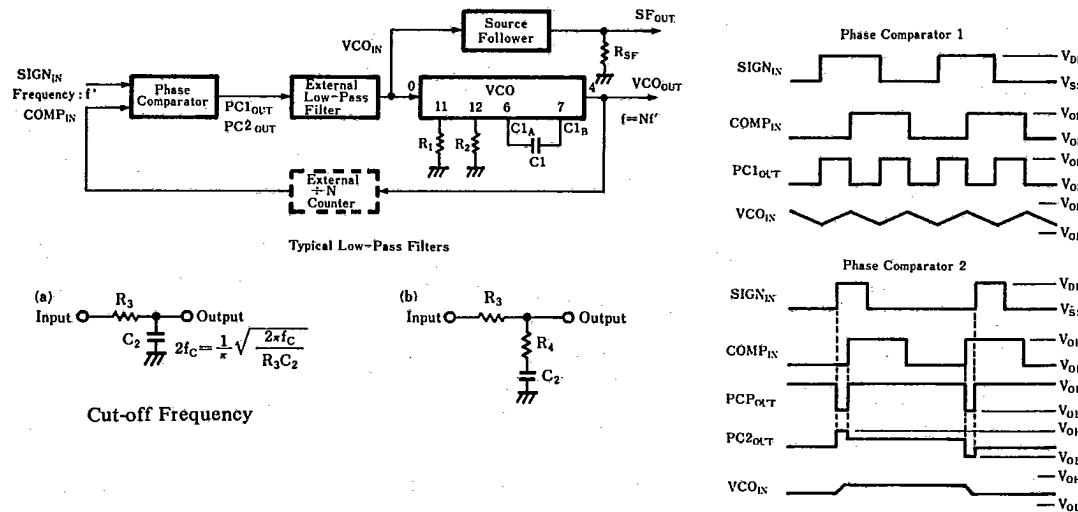
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• Zener Diode

Item	V _{DD} (V)	Symbol	Condition	min.	typ.	max.	Unit
Zener Voltage		V _Z	I _Z = 50 μA	—	7.3	—	V
Action Resistance		R _Z	I _Z = 1 mA	—	25	—	Ω

(Fig. 1) General PLL Connections

(Fig. 2) Phase Comparator Mode Diagrams
