CMOS High-Speed 8-Bit Bidirectional CMOS/TTL Interface Level Converter

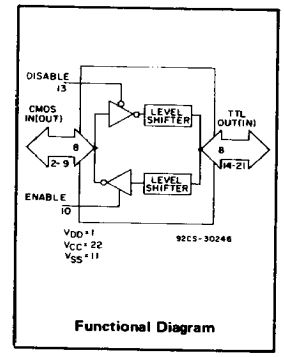
The RCA-CD40115 is a high-speed 8-bit integrated circuit designed to interface CMOS logic levels with TTL logic levels on the data bus of microprocessor-based systems. CMOS/TTL interface is provided by eight parallel bidirectional buffer/level converters. Buffer INPUT/OUTPUT terminals are either inputs or outputs depending on the desired direction of data flow. A low on both the ENABLE and DISABLE control inputs selects the direction of data flow from CMOS Inputs to TTL Outputs. A high on both control inputs selects the direction of data flow from TTL Inputs to CMOS Outputs. A low on the ENABLE and a high on the DISABLE inhibits data flow in either direction and places the CMOS Outputs in a high-impedance (3-state) mode.

The TTL Input/Output terminals and the ENABLE and DISABLE control inputs are TTL-compatible without the use of external pull-up resistors. The TTL input logic 0 to logic 1 transition occurs at a level of approximately 1.5 volts. The ENABLE and DISABLE inputs may be driven to the V_{DD} rail; therefore, either TTL or CMOS logic drivers, capable of sinking one TTL load, may be used to determine the direction of data flow. The large CMOS and TTL output buffers in this device have high output sink and source current capability and can drive the data bus capacitance with a transition time of approximately 0.1 ns/pF. This fast output transition time, together with the small propagation delay time of the device, allow high-speed operation.

The CD40115 is supplied in a 22-lead hermetic dual-in-line ceramic package.

Features:

- **Eight inverting channels with 5V-to-12V or 12V-to-5V level conversion**
- **Three operating modes:**
  - **CMOS-to-TTL level conversion**
  - **TTL-to-CMOS level conversion**
  - **Interface off; high-impedance CMOS input/output**
- **Low propagation delay time:**
  - **CMOS-to-TTL conversion — 10 ns typ.**
  - **TTL-to-CMOS conversion — 30 ns typ.**
- **High TTL sink current — 30 mA typ.**
- **No external TTL input pull-up resistors required**
- **High speed drive of large data bus capacitances**
- **Input/output and power supply terminals located for ease of PC board layout**



Functional Diagram

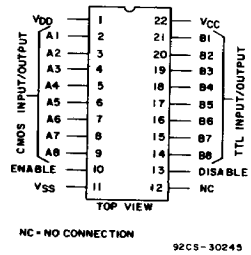
Applications:

- **Interface CMOS microprocessor with TTL memories and peripheral devices**
- **Interface between and within logic systems which combine CMOS and TTL devices**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE (Voltages referenced to VSS Terminal)

V_{DD}	−0.5 to +12.6 V
V_{CC}	−0.5 to +6 V
INPUT VOLTAGE RANGE:	
Data Inputs, CMOS to TTL	−0.5 to V_{DD}+0.5 V
Data Inputs, TTL to CMOS	−0.5 to V_{CC}+0.5 V
Enable, Disable Inputs	−0.5 to V_{DD}+0.5 V
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −55°C to +100°C	500 mW
For T_A = +100 to +125°C	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T_A = Full Package-Temperature Range	100 mW
OPERATING TEMPERATURE RANGE (T_A)	−55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance of 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C



TERMINAL ASSIGNMENT

TRUTH TABLE

ENABLE	DISABLE	FUNCTION
0	0	Convert CMOS Level to TTL Level
1	1	Convert TTL Level to CMOS Level
0	1	High Impedance (Z)
1	0	Invalid*

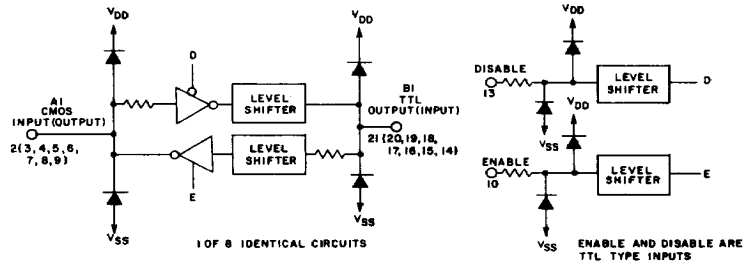
0 = Low Level 1 = High Level

Z = High Impedance on CMOS Output side; TTL side are inputs.

INVALID = Both CMOS and TTL sides are ON as outputs.

See Operating and Handling Considerations — Bypassing and Unused Inputs.

* Excessively high currents from V_{DD} to V_{SS} could flow in this mode during power turn-on or turn-off if other IC's drive into the bus lines (on either the TTL or CMOS side). This high current condition could occur during a transient or steady-state invalid mode.



Input (Output)		Output (Input)	
Data	Terminal No.	Data	Terminal No.
A1	2	B1	21
A2	3	B2	20
A3	4	B3	19
A4	5	B4	18
A5	6	B5	17
A6	7	B6	16
A7	8	B7	15
A8	9	B8	14

Fig. 1 — Functional block diagram.

STATIC ELECTRICAL CHARACTERISTICS At T_A = 25°C, V_{DD} = 12 V, V_{CC} = 5 V

CHARACTERISTIC		TEST CONDITIONS	TYPICAL VALUES	UNITS
Data Flow — CMOS Inputs to TTL Outputs				
Quiescent Device Current, From V_{DD} Supply,	I_{DD}		4	mA
From V_{CC} Supply,	I_{CC}		5	μA
Input Current,	I_{IN}	V_{IN}=0,12 V; Any CMOS input	±50	μA
Output Current,	I_{OH}	V_{OH}=3 V, V_{IL}=2 V	15	mA
	I_{OL}	V_{OL}=0.4 V, V_{IH}=10 V	30	
Data Flow — TTL Inputs to CMOS Outputs				
Quiescent Device Current, From V_{DD} Supply,	I_{DD}		4	mA
From V_{CC} Supply,	I_{CC}		5	μA
Input Current,	I_{IL}	V_{IL}=0 to 0.7 V; Any TTL input	−250	μA
	I_{IH}	V_{IH}=2.3 V; Any TTL input	−50	
Output Current,	I_{OH}	V_{OH}=11.5 V, V_{IL}=0.7 V	20	mA
	I_{OL}	V_{OL}=0.5 V, V_{IH}=2.3 V	20	
CMOS 3-State Output Leakage Current,	I_{OUT}	V_O=0,12 V, V_{IN}=0,5 V	±50	μA
Enable and Disable Inputs				
Input Current,	I_{IL}	V_{IL}=0 to 0.7 V	−250	μA
	I_{IH}	V_{IH}=2.3 V (TTL)	−50	
	I_{IH}	V_{IH}=12 V (CMOS)	50	

DYNAMIC ELECTRICAL CHARACTERISTICS At T_A = 25°C, V_{DD} = 12 V, V_{CC} = 5 V

CHARACTERISTIC	TEST CONDITIONS		TYPICAL VALUES		UNITS
	INPUT	OUTPUT	C_L=50 pF	C_L=200 pF	
Propagation Delay Times, Data-In to Data-Out, t_{PHL}, t_{PLH}	CMOS	TTL	10	15	ns
	TTL	CMOS	30	40	
Enable or Disable to Data-Out, t_{PHZ}, t_{PZH}, t_{PLZ}, t_{PZL}			35		ns
Transition Time, t_{THL}, t_{TLH}	CMOS	TTL	10	15	ns
	TTL	CMOS	10	15	