

54LS/74LS563 011122 OCTAL D-TYPE LATCH (With 3-State Outputs)

DESCRIPTION — The '563 is a high speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

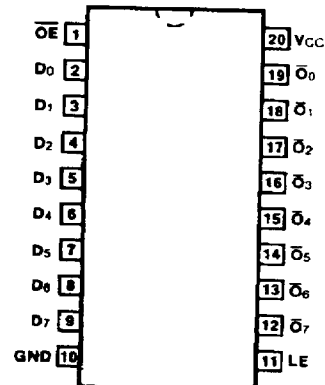
This device is functionally identical to the 'LS573, but has inverted outputs. For truth tables, discussion of operations and ac and dc specifications, please refer to the 'LS373 data sheet, but note that the data to output delays are 5.0 ns longer for the 'LS563 than for the 'LS373.

- INPUTS AND OUTPUTS ON OPPOSITE SIDES OF PACKAGE ALLOWING EASY INTERFACE WITH MICROPROCESSORS
- USEFUL AS INPUT OR OUTPUT PORT FOR MICROPROCESSORS
- FUNCTIONALLY IDENTICAL TO 'LS573
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

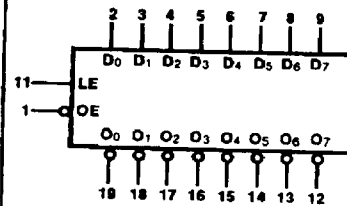
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0\text{ V} \pm 5\%$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$	$V_{CC} = +5.0\text{ V} \pm 10\%$, $T_A = -55^\circ\text{C to } +125^\circ\text{C}$	
Plastic DIP (P)	A	74LS563PC		9Z
Ceramic DIP (D)	A	74LS563DC	54LS563DM	4E
Flatpak (F)	A	74LS563FC	54LS563FM	4F

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$D_0 - D_7$	Data Inputs	
LE	Latch Enable Input (Active HIGH)	0.5/0.25
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.25
$\overline{O}_0 - \overline{O}_7$	3-State Latch Outputs	0.5/0.25
		65/15
		(25)/(7.5)