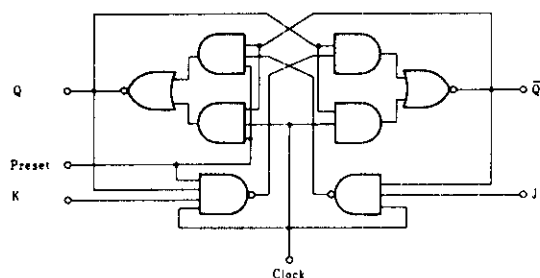
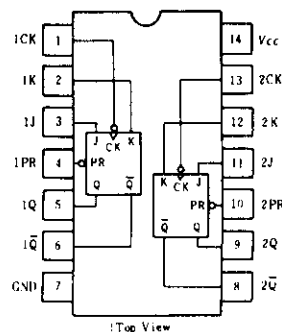


HD74LS113 ● Dual J-K Negative-edge-triggered Flip-Flops (with Preset)

■ BLOCK DIAGRAM (1/2)



■ PIN ARRANGEMENT



■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Clock frequency	f_{clock}	0	—	30	MHz
Pulse width	CK	20	—	—	ns
	PR	25	—	—	
Setup time	"H" level	20↓	—	—	ns
	"L" level	20↓	—	—	
Hold time	t_h	0↓	—	—	ns

Note) ↓: The arrow indicates the falling edge.

■ FUNCTION TABLE

Inputs				Outputs	
Preset	Clock	J	K	Q	$\bar{Q}$
L	X	X	X	H	L
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q_0	$\bar{Q}_0$

Notes) H: high level, L: low level, X: irrelevant

↓: transition from high to low level

Q_0 : level of Q before the indicated steady-state input conditions were established.

$\bar{Q}_0$: complement of Q_0 or level of $\bar{Q}$ before the indicated steady-state input conditions were established.

Toggle: each output changes to the complement of its previous level on each active transition indicated by ↓.

■ ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$)

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input voltage	V_{IH}		2.0	—	—	V
	V_{IL}		—	—	0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75\text{V}$, $V_{IH}=2\text{V}$, $V_{IL}=0.8\text{V}$, $I_{OH}=-400\mu\text{A}$	2.7	—	—	V
	V_{OL}	$V_{CC}=4.75\text{V}$, $V_{IL}=0.8\text{V}$, $I_{OL}=4\text{mA}$ $V_{IH}=2\text{V}$, $I_{OL}=8\text{mA}$	—	—	0.4 0.5	V
Input current	J, K	$V_{CC}=5.25\text{V}$, $V_I=2.7\text{V}$	—	—	20	μA
	Preset		—	—	60	
	Clock		—	—	80	
	J, K	$V_{CC}=5.25\text{V}$, $V_I=0.4\text{V}$	—	—	-0.4	mA
	Preset		—	—	-0.8	
	Clock		—	—	-0.8	
	J, K	$V_{CC}=5.25\text{V}$, $V_I=7\text{V}$	—	—	0.1	mA
	Preset		—	—	0.3	
	Clock		—	—	0.4	
Short-circuit output current	I_{OS}	$V_{CC}=5.25\text{V}$	-20	—	-100	mA
Supply current **	I_{CC}	$V_{CC}=5.25\text{V}$	—	4	8	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75\text{V}$, $I_{IH}=-18\text{mA}$	—	—	-1.5	V

* $V_{CC}=5\text{V}$, $T_a=25^\circ\text{C}$

** With all outputs open, I_{CC} is measured with the Q and $\bar{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

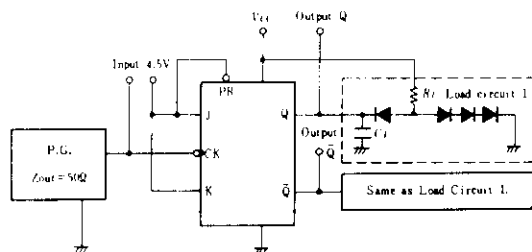
■ SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$)

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	f_{max}			$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$	30	45	—	MHz
Propagation delay time	t_{PLH}	Preset Clock	Q, $\bar{Q}$		—	11	20	ns
	t_{PHL}				—	15	30	ns

■ TESTING METHOD

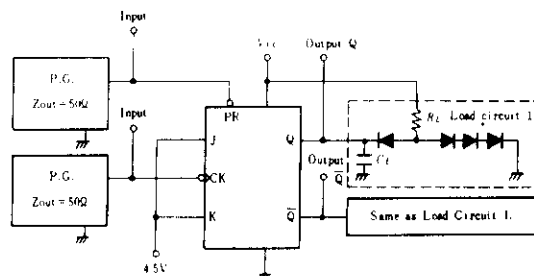
1.1) Test Circuit

1.1) f_{max} , t_{PLH} , t_{PHL} (Clock $\rightarrow$ Q, $\bar{Q}$)



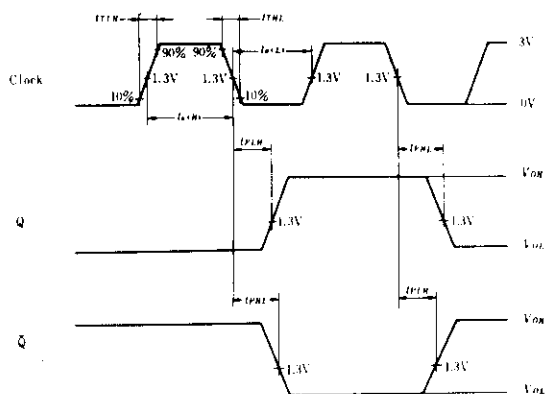
- Notes) 1. Test is put into the each flip-flop.
2. All diodes are 1S2074 (H).
3. C_L includes probe and jig capacitance.

1.2) t_{PHL} (Preset $\rightarrow$ Q), t_{PLH} (Preset $\rightarrow$ Q)

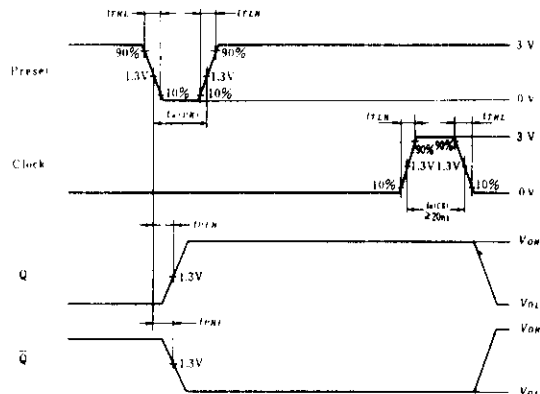


- Notes) 1. Test is put into the each flip-flop.
2. All diodes are 1S2074 (H).
3. C_L includes probe and jig capacitance.

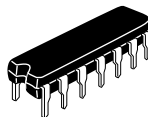
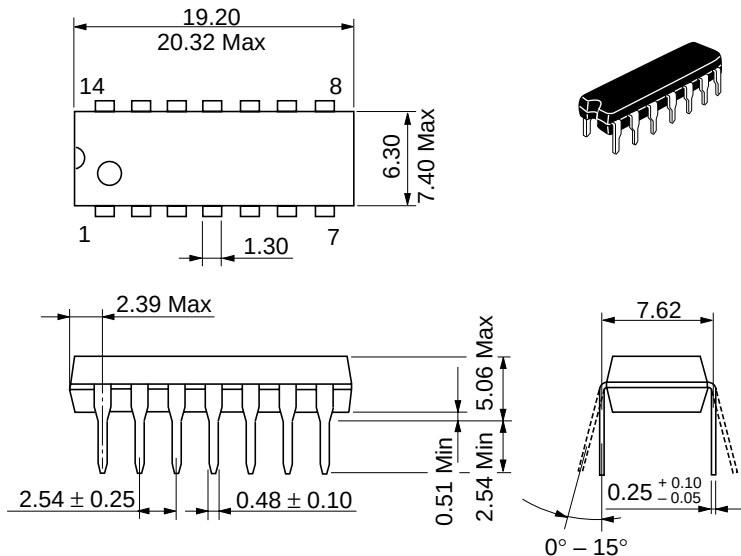
Waveform



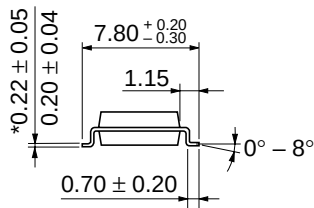
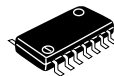
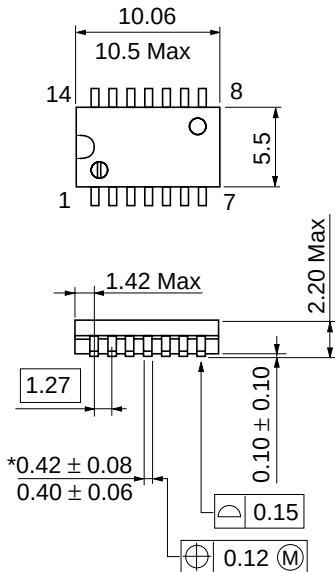
Note) Clock input pulse: $t_{TLH} \leq 15ns$, $t_{THL} \leq 6ns$, $PRR=1MHz$, duty cycle=50% and: for f_{max} , $t_{TLH}=t_{THL} \leq 2.5ns$.



Note) Preset and clock input pulse: $t_{TLH} \leq 15ns$, $t_{THL} \leq 6ns$, $PRR=1MHz$

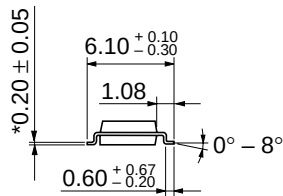
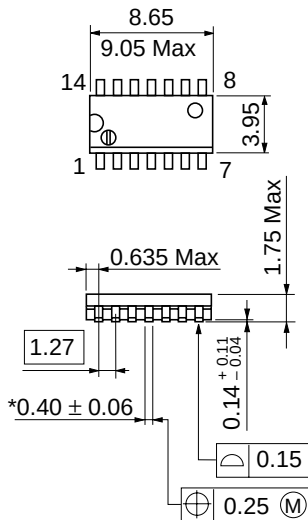


Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g



Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g

*Dimension including the plating thickness
Base material dimension



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g

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