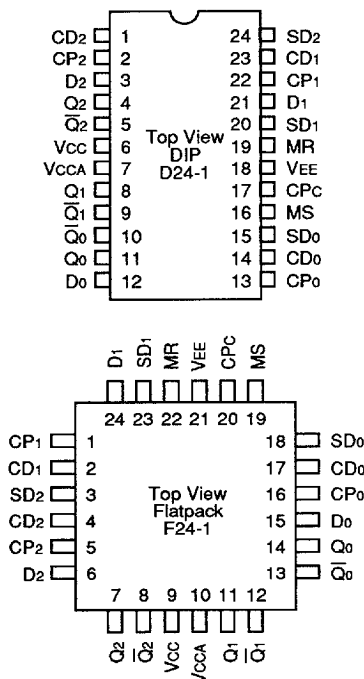


FEATURES

- Max. toggle frequency of 800MHz
- Differential outputs
- IEE min. of -80mA
- ESD protection of 2000V
- Industry standard 100K ECL levels
- Extended supply voltage option:
— VEE = -4.2V to -5.46V
- Voltage and temperature compensation for improved noise immunity
- Internal 75KΩ Input pull-down resistors
- 150% faster than National or Signetics
- 40% lower power than National or Signetics
- Function and pinout compatible with National and Signetics F100K
- Available in Cerdip, CERPAC and PLCC

PIN CONFIGURATIONS



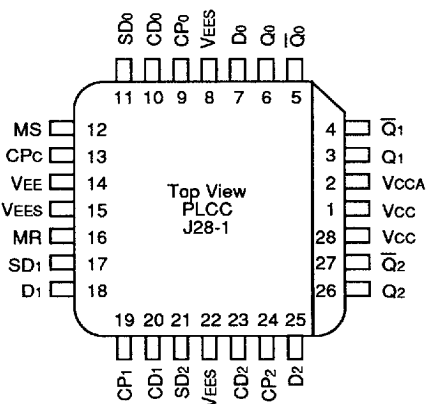
DESCRIPTION

The SY100S331 offers three D-type, edge-triggered master/slave flip-flops with true and complement outputs, designed for use in high-performance ECL systems. Each flip-flop is controlled by a common clock (CPC), as well as its own clock pulse (CPn). The resultant clock signal controlling the flip-flop is the logical OR operation of these two clock signals. Data enters the master when both CPC and CPn are LOW and enters the slave on the rising edge of either CPC or CPn (or both).

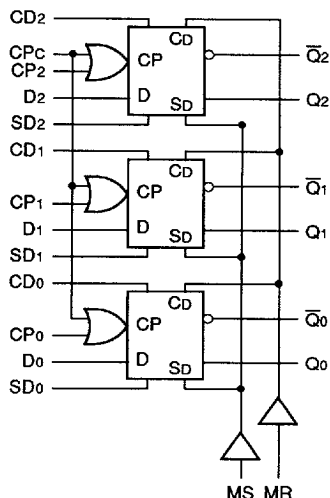
Additional control signals include Master Set (MS) and Master Reset (MR) inputs. Each flip-flop also has its own Direct Set (SDn) and Direct Clear (CDn) signals. The MR, MS, SDn and DCn signals override the clock signals. The inputs on this device have 75KΩ pull-down resistors.

PIN NAMES

Pin	Function
CP0 – CP2	Individual Clock Inputs
CPC	Common Clock Input
D0 – D2	Data Inputs
CD0 – CD2	Individual Direct Clear Inputs
SDn	Individual Direct Set Inputs
MR	Master Reset Input
MS	Master Set Input
Q0 – Q2	Data Outputs
Q0 – Q2	Complementary Data Outputs



BLOCK DIAGRAM



TRUTH TABLES

Asynchronous Operation ⁽¹⁾					
Inputs					Outputs
D _n	CP _n	CP _c	MS SD _n	MR DC _n	Q _n (t+1)
X	X	X	H	L	H
X	X	X	L	H	L
X	X	X	H	H	U

NOTE:

1. H = High Voltage Level, L = Low Voltage Level, X = Don't Care, U = Undefined, t = Time before CP Positive Transition, t+1 = Time after CP Positive Transition, / = Low-to-High Transition

Synchronous Operation ⁽¹⁾					
Inputs					Outputs
D _n	CP _n	CP _c	MS SD _n	MR DC _n	Q _n
L	/	L	L	L	L
H	/	L	L	L	H
L	L	/	L	L	L
H	L	/	L	L	H
X	L	L	L	L	Q _n (t)
X	H	X	L	L	Q _n (t)
X	X	H	L	L	Q _n (t)

NOTE:

1. H = High Voltage Level, L = Low Voltage Level, X = Don't Care, U = Undefined, t = Time before CP Positive Transition, t+1 = Time after CP Positive Transition, / = Low-to-High Transition

DC ELECTRICAL CHARACTERISTICS

VEE = -4.2V to -5.46V unless otherwise specified, VCC = VCCA = GND, TA = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I _{IH}	Input HIGH Current, All Inputs	—	—	200	μA	V _{IN} = V _{IH} (Max.)
I _{EE}	Power Supply Current	-80	-65	-35	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERDIP

$V_{EE} = -4.2V$ to $-5.46V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_A = 0^{\circ}C$ to $+85^{\circ}C$

Symbol	Parameter	$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{max}	Toggle Frequency	800	—	800	—	800	—	MHz	—
tPLH tPHL	Propagation Delay CP _c to Output	300	900	300	900	300	900	ps	—
tPLH tPHL	Propagation Delay CP _n to Output	300	900	300	900	300	900	ps	—
tPLH tPHL	Propagation Delay CD _n , SD _n to Output	300	1000	300	1000	300	1000	ps	—
tPLH tPHL	Propagation Delay MS, MR to Output	300	1100	300	1100	300	1100	ps	—
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	—
t _s	Set-up Time D _n	400	—	400	—	400	—	ps	—
	CD _n , SD _n (Release Time)	500	—	500	—	500	—		
	MS, MR (Release Time)	800	—	800	—	800	—		
t _n	Hold Time D _n	300	—	300	—	300	—	ps	—
t _{pw} (H)	Pulse Width HIGH CP _n , CP _c , DC _n SD _n , MR, MS	800	—	800	—	800	—	ps	—

CERPACK

$V_{EE} = -4.2V$ to $-5.46V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_A = 0^{\circ}C$ to $+85^{\circ}C$

Symbol	Parameter	$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{max}	Toggle Frequency	800	—	800	—	800	—	MHz	—
tPLH tPHL	Propagation Delay CP _c to Output	300	800	300	800	300	800	ps	—
tPLH tPHL	Propagation Delay CP _n to Output	300	800	300	800	300	800	ps	—
tPLH tPHL	Propagation Delay CD _n , SD _n to Output	300	900	300	900	300	900	ps	—
tPLH tPHL	Propagation Delay MS, MR to Output	300	1000	300	1000	300	1000	ps	—
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	—
t _s	Set-up Time D _n	400	—	400	—	400	—	ps	—
	CD _n , SD _n (Release Time)	500	—	500	—	500	—		
	MS, MR (Release Time)	800	—	800	—	800	—		
t _n	Hold Time D _n	300	—	300	—	300	—	ps	—
t _{pw} (H)	Pulse Width HIGH CP _n , CP _c , DC _n SD _n , MR, MS	800	—	800	—	800	—	ps	—

AC ELECTRICAL CHARACTERISTICS (CONT'D.)

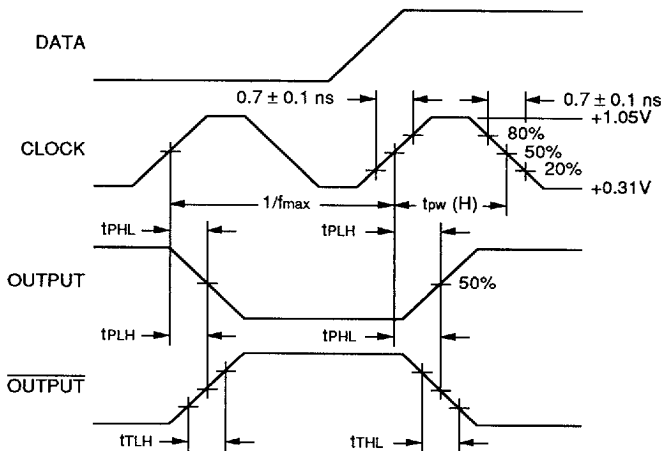
PLCC

VEE = -4.2V to -5.46V unless otherwise specified, VCC = VCCA = GND, TA = 0°C to +85°C

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
fmax	Toggle Frequency	800	—	800	—	800	—	MHz	—
tPLH tPHL	Propagation Delay CP _c to Output	300	700	300	700	300	700	ps	—
tPLH tPHL	Propagation Delay CP _n to Output	300	700	300	700	300	700	ps	—
tPLH tPHL	Propagation Delay CD _n , SD _n to Output	300	800	300	800	300	800	ps	—
tPLH tPHL	Propagation Delay MS, MR to Output	300	900	300	900	300	900	ps	—
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	—
ts	Set-up Time D _n	400	—	400	—	400	—	ps	—
	CD _n , SD _n (Release Time)	500	—	500	—	500	—		
	MS, MR (Release Time)	800	—	800	—	800	—		
tn	Hold Time D _n	300	—	300	—	300	—	ps	—
tpw (H)	Pulse Width HIGH CP _n , CP _c , DC _n SD _n , MR, MS	800	—	800	—	800	—	ps	—

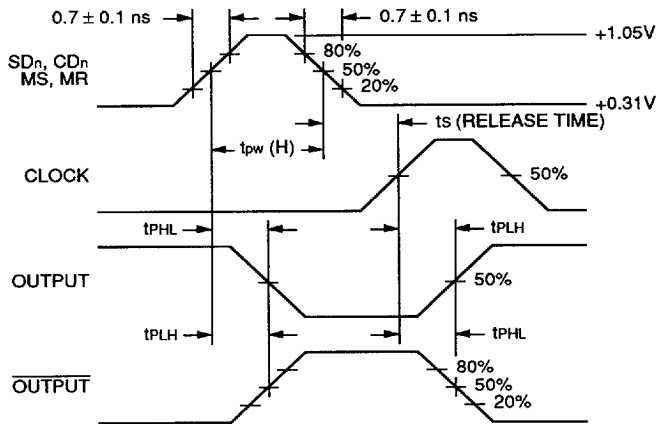
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TIMING DIAGRAMS



Propagation Delay (Clock) and Transition Times

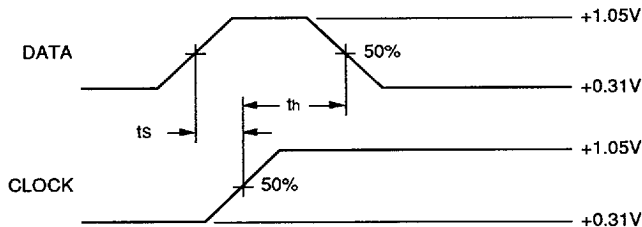
TIMING DIAGRAMS (CONT'D.)



Propagation Delay (Sets and Resets)

NOTE:

SD_n uses complement of DATA and complement of OUTPUT waveforms.



Data Setup and Hold Time

NOTES:

ts is the minimum time before the transition of the clock that information must be present at the data input

th is the minimum time after the transition of the clock that information must remain unchanged at the data input

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S331DC	D24-1	Commercial
SY100S331FC	F24-1	Commercial
SY100S331JC	J28-1	Commercial