Wide Input Voltage, Adjustable Frequency, 3.5 Amp Buck Regulator

FEATURES AND BENEFITS

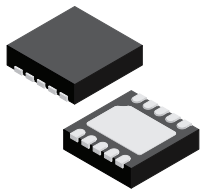
- Automotive AEC-Q100 qualified
- Supply voltage from 3.8 to 36 V
- Output voltage adjustable from 0.8 to 30 V
- Maximized duty cycle for low dropout operation
- Low 30 µA operational quiescent current
- 150 mΩ integrated MOSFET switch
- Programmable switching frequency up to 4 MHz
- Improved EMC with frequency dithering (A8586 and A8586-2) and controlled switch node rise and fall times
- Ceramic capacitor stable
- Internal soft-start
- Overcurrent protection

APPLICATIONS

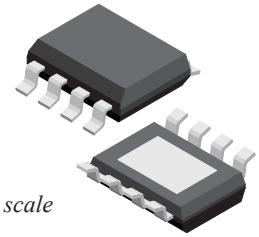
- High-Voltage Power Conversion
- Automotive Systems
- Industrial Power System
- Distributed Power Systems
- Battery-Powered Systems

PACKAGES:

10-Pin DFN with Exposed Thermal Pad (suffix EJ)



8-Pin SOIC with Exposed Thermal Pad (suffix LJ)



Not to scale

DESCRIPTION

The A8586 is a high frequency step-down switching regulator with an integrated high-side power MOSFET. It provides up 3.5 A output current. The A8586 can achieve fast transient response using current-mode control and simple external compensation.

The wide input range of 3.8 to 36 V makes the A8586 suitable for a wide range of step-down applications, including those in an automotive input environment. Battery-driven applications benefit from the low 30 µA operational quiescent current.

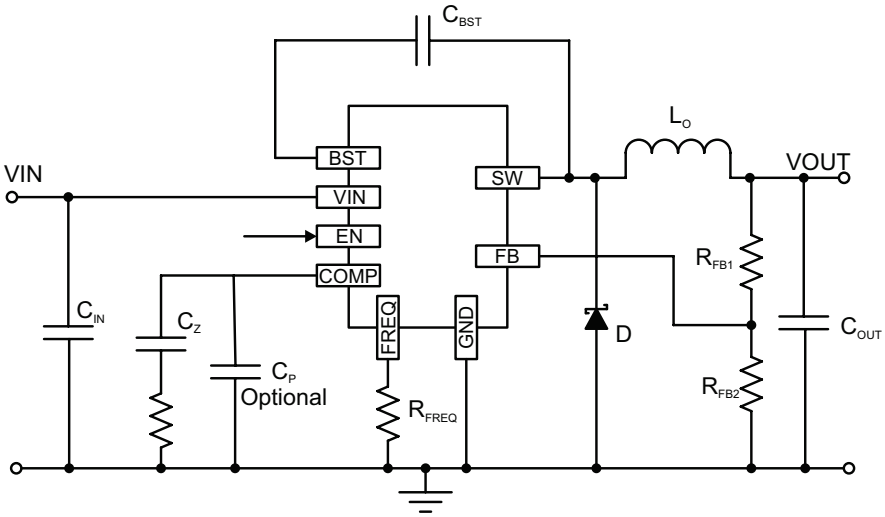
The A8586 maintains high efficiency across a wide load range by the use of pulse-frequency modulation (PFM) as the load reduces. This in turn reduces switching and gate driver losses at light load. A8586-1 and A8586-2 are options that disable the PFM function. A8586-1 also disables the dithering feature. These can be useful when low output ripple and minimum output capacitance is required.

Frequency foldback helps to prevent inductor current runaway during startup and provides enhanced dropout performance. Extensive protection features of the A8586 include pulse-by-pulse current limit, hiccup mode short-circuit protection, open/short freewheeling diode protection, BOOT open/short voltage protection, VIN undervoltage lockout, and thermal shutdown.

The A8586 and A8586-2 are designed to aid in EMC/EMI design by including frequency dithering, soft freewheel diode turn-off, and well controlled switch node slew rates. A 4 MHz oscillator allows the A8586 to switch outside EMI sensitive frequencies bands such as the AM band or ADSL bands.

The A8586 is available in industry-standard DFN-10 or SOIC-8 packages.

Part	Dither Feature	PFM Operation
A8586	Yes	Yes
A8586-1	No	No
A8586-2	Yes	No



A8586 Simplified Schematic

SPECIFICATIONS

SELECTION GUIDE

Part Number	Package	Packing [1]
A8586KLJTR-T	8-pin SOIC with thermal pad	3,000 pieces per 13-inch reel
A8586KEJTR-T	10-pin DFN with thermal pad	1,500 pieces per 7-inch reel
A8586KLJTR-T-1	8-pin SOIC with thermal pad	3,000 pieces per 13-inch reel
A8586KLJTR-T-2	8-pin SOIC with thermal pad	3,000 pieces per 13-inch reel

[1] Contact Allegro for additional packing options.

ABSOLUTE MAXIMUM RATINGS [2]

Characteristic	Symbol	Notes	Rating	Unit
Input Voltage	V_{IN}		−0.3 to 40	V
Switch Node Voltage	V_{SW}		−0.3 to V_{IN} + 0.3	V
		t < 250 ns	−1.5	V
		t < 50 ns	V_{IN} + 3	V
Bootstrap Pin to Switch Node	V_{BST-SW}		−0.3 to 6	V
EN, FREQ			−0.3 to V_{IN} + 0.3	V
All other pins			−0.3 to 6	V
Junction Temperature	T_J		−40 to 150	°C
Storage Temperature Range	T_{stg}		−40 to 150	°C

[2] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

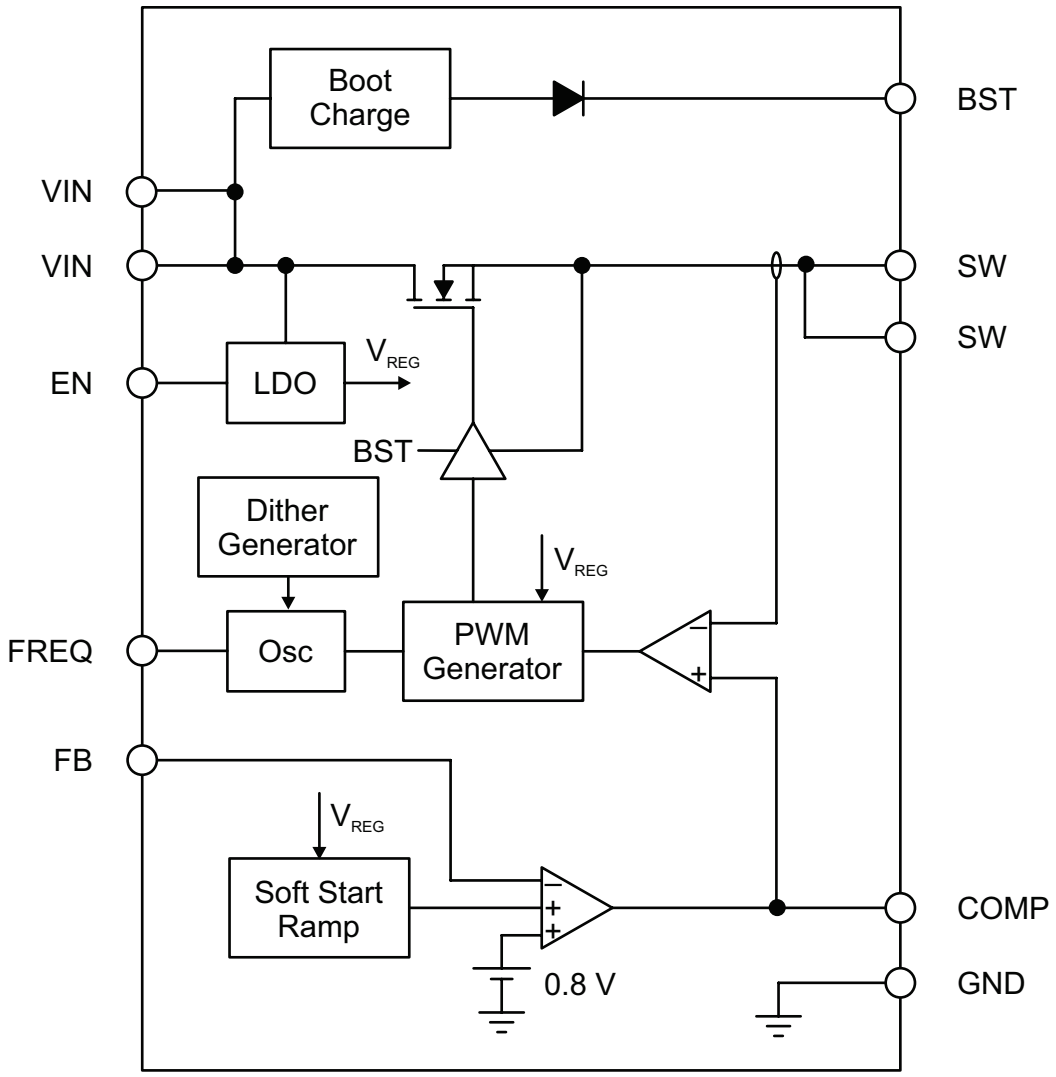
RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Test Conditions	Value	Unit
Input Voltage	V_{IN}		3.8 to 36	V
Junction Temperature	T_J		−40 to 150	°C

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

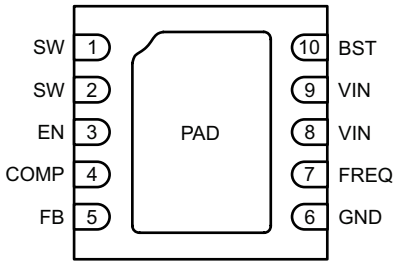
Characteristic	Symbol	Test Conditions [3]	Value	Unit
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	DFN-10 (EJ) package on 4-layer PCB based on JEDEC standard	45	°C/W
		SOIC-8 (LJ) package on 4-layer PCB based on JEDEC standard	35	

[3] Additional thermal information available on the Allegro website.

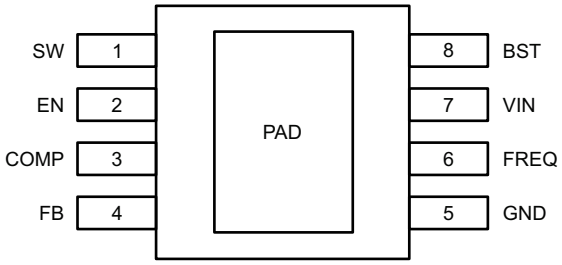


Functional Block Diagram

PINOUT DIAGRAMS AND TERMINAL LIST TABLE



Package EJ Pinouts



Package LJ Pinouts

Terminal List Table

Pin Name	Pin Number		Description
	EJ Package	LJ Package	
SW	1, 2	1	The source of the internal MOSFET. The output inductor (L_O) and cathode of the freewheel diode (D) should be connected to this pin. L_O and D should be placed as close as possible to this pin and connected with relatively wide traces.
EN	3	2	Enable input. This pin is a high-voltage input that turns the regulator on or off: Set this pin high to turn the regulator on or set this pin low to turn the regulator off.
COMP	4	3	Output of the error amplifier and compensation node for the current-mode control loop. Connect a series RC network from this pin to GND for loop compensation. See the Applications section of this datasheet for further details
FB	5	4	Feedback (negative) input to the error amplifier. Connect a resistor divider from the regulator output node, VOUT, to this pin to program the output voltage.
GND	6	5	Ground connection
FREQ	7	6	Frequency setting pin. A resistor, R_{FREQ}, from this pin to GND sets the PWM switching frequency. See Table 1 and Figure 2 to determine the value of R_{FREQ}.
VIN	8, 9	7	Power input for the control circuits and the drain of the internal high-side N-channel MOSFET. Connect this pin to a power supply of 3.8 to 36 V. A high quality ceramic capacitor should be placed very close to this pin and GND
BST	10	8	Bootstrap capacitor connection. Connect a 100 nF capacitor from this pin to the SW pin. The voltage on this capacitor drives the internal MOSFET via the high side gate driver. A series BOOT resistor is not recommended.

ELECTRICAL CHARACTERISTICS [1]: Valid for V_{IN} = 12 V, V_{EN} = 2.5 V, V_{COMP} = 1.4 V, –40°C ≤ T_J ≤ 125°C, typical values at T_J = 25°C, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL SPECIFICATIONS						
Operating Input Voltage	V_{IN}	V_{EN} ≥ 2.5 V	3.8	12	36	V
VIN UVLO Start	$V_{IN(START)}$	V_{IN} rising	2.6	3.0	3.4	V
VIN UVLO Hysteresis	$V_{IN(HYS)}$		–	0.4	–	V
Supply Quiescent Current [1]	I_Q	No load, V_{FB} = 0.9 V	–	27	36	μA
	$I_{Q(SLEEP)}$	V_{EN} = 0 V	–	11	18	μA
PWM SWITCHING FREQUENCY						
Switching Frequency	f_{SW}	R_{FSET} = 45 kΩ	1.6	2.0	2.4	MHz
THERMAL PROTECTION						
Thermal Shutdown Threshold [2]	T_{TSD}	T_J rising	–	170	–	°C
Thermal Shutdown Hysteresis [2]	T_{HYS}		–	20	–	°C
PULSE-WIDTH MODULATION (PWM)						
Minimum On-Time [2]	$t_{ON(MIN)}$		–	80	160	ns
Minimum Off-Time [2]	$t_{OFF(MIN)}$		–	100	–	ns
INTERNAL MOSFET						
MOSFET On Resistance	$R_{DS(on)}$	$V_{BOOT-SW}$ = 5 V	–	150	–	mΩ
MOSFET Leakage	$I_{FET(LKG)}$	V_{EN} = 0 V, V_{IN} = 12 V, V_{SW} = 0 V, T_J = 25°C	–	0.1	1	μA
ERROR AMPLIFIER						
Feedback Voltage	V_{FB}	4.5 V ≤ V_{IN} ≤ 36 V, T_J = 25°C	0.786	0.792	0.803	V
		4.5 V ≤ V_{IN} ≤ 36 V, –40°C ≤ T_J ≤ 125°C	0.773	–	0.812	V
Error Amp Voltage Gain [2]	A_{VOL}		–	1000	–	V/V
Error Amp Transconductance [2]	g_m	I_{COMP} = ±3 μA	35	60	95	μA/V
Error Amp Min. Source Current	$I_{EA(SOURCE)}$	V_{FB} = 0.7 V	–	–5	–	μA
Error Amp Min. Sink Current	$I_{EA(SINK)}$	V_{FB} = 0.9 V	–	5	–	μA
Low I_Q Peak Current Threshold	$I_{PEAK(LO_IQ)}$		–	800	–	mA
SOFT-START						
SS Ramp Time [2]	t_{SS}	0 V < V_{FB} < 0.8 V	–	1.5	–	ms
CURRENT PROTECTION						
Current Limit	I_{LIM}		4.0	5.5	–	A
COMP to Current Sense Transductance [2]	G_{CS}		–	9	–	A/V
Slope Compensation	$S_{E(2MHz)}$	Measured at f_{SW} = 2 MHz	2.2	3.1	4.0	A/μs
LOGIC ENABLE						
EN Threshold Rising	$V_{EN(H)}$	V_{EN} rising	1.2	1.5	1.85	V
EN Threshold Falling	$V_{EN(L)}$	V_{EN} falling	1.0	1.2	1.4	V
EN Hysteresis	$V_{EN(HYS)}$		–	300	–	mV

1 For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
2 Ensured by design and characterization, not production tested.

FUNCTIONAL DESCRIPTION

Overview

The A8586 is a PWM buck regulator that incorporates all the control and protection circuitry necessary to satisfy a wide range of low-voltage applications. The A8586 employs current-mode control to provide fast transient response, simple compensation, and excellent stability.

The features of the A8586 include a ±3% reference, an adjustable switching frequency, a transconductance error amplifier, an enable input, integrated power MOSFET, fixed soft-start time, and low-current sleep mode.

The protection features of the A8586 include undervoltage lockout (UVLO), cycle-by-cycle overcurrent protection (OCP), hiccup mode short-circuit protection (HIC), overvoltage protection (OVP), and thermal shutdown (TSD).

PWM Control

A high-speed PWM comparator, capable of pulse widths less than 100 ns, is included in the A8586. The inverting input of the comparator is connected to the output of the error amplifier. The non-inverting input is connected to the current sense signal.

At the beginning of each PWM cycle, the PWM_CLK signal sets the PWM flip-flop and the high-side MOSFET is turned on. When the current sense signal rises above the error amplifier voltage, the comparator resets the PWM flip-flop and the high-side MOSFET is turned off. It remains off for at least 100 ns before the next cycle can be initiated.

Low-I_Q Pulse-Frequency Modulation (PFM) Mode (A8586 only)

At light loads, the PFM comparator, which is connected to the FB pin, modulates the frequency of the SW node to regulate the output voltage with very high efficiency.

The reference for the PFM comparator is calibrated approximately 1% above the PWM regulation point. When the voltage at the internal FB point rises above the PFM comparator threshold and peak inductor current falls below $I_{PEAK(LO_IQ)}$ (800 mA) minus slope compensation, the device will enter PFM coast mode, tri-stating the SW node and drawing extremely low current from VIN. When voltage at the FB point falls below the PFM comparator threshold, the device will fully power-up after approximately a 2.5 µs delay and the high-side MOSFET is repeatedly turned on, operating at the PWM switching frequency until the voltage at the FB pin rises above the PFM comparator threshold. V_{OUT} will rise at a rate determined by—and have a voltage ripple dependent on—the input voltage, output voltage, inductor value, output capacitance, and load. In addition, the transition point from PWM to PFM mode is defined by the input voltage, output voltage, slope compensation, and inductor value.

Error Amplifier

The primary function of the transconductance error amplifier is to regulate the A8586 output voltage. The error amplifier appears as a device with three inputs: two positive and one negative. The negative input is simply connected to the FB pin and is used to sense the feedback voltage for regulation. The two positive inputs are connected to the internal soft-start and reference voltages. The error amplifier performs an analog OR selection between them; it regulates to either the soft-start voltage or the A8586 internal reference (V_{REF}), whichever is lower.

To stabilize the regulator, a series RC compensation network (R_Z C_Z) must be connected from the error amplifier output (COMP pin) to GND as shown in the typical application schematic. In most applications, an additional, low-value capacitor (C_P) should be connected in parallel with the R_Z C_Z compensation network to roll-off the loop gain at higher frequencies. However, if the C_P capacitor is too large, the phase margin of the regulator may be reduced.

During operation, the minimum COMP voltage is clamped to 750 mV and its maximum is clamped to 1.5 V. COMP is internally pulled down to GND during fault conditions.

Slope Compensation

The A8586 family incorporates internal slope compensation (S_E) to allow PWM duty cycles above 50% for a wide range of input/output voltages and inductor values. The slope compensation signal is added to the sum of the current sense amplifier output and the PWM ramp offset. The amount of slope compensation scales with the maximum on-time ($1/f_{SW} - t_{OFF(MIN)}$) centered around 3.1 A/µs at 2 MHz. The value of the output inductor should be chosen such that S_E is between 0.5× and 1× the falling slope of the inductor current (S_F).

Internal Regulator

An internal series-pass regulator (LDO) generates around 2.9 V for most of the internal circuits of the A8586. The power for this LDO is derived from V_{IN}. The LDO is in full regulation once V_{IN} is greater than 3.0 V.

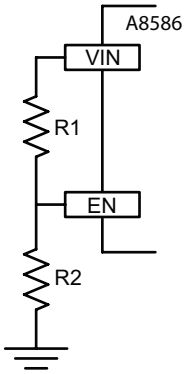
Enable Control

The enable (EN) input provides enabling/disabling the A8586 with system control or enabling/disabling the A8586 automatically. The EN pin is rated to 40 V, so this EN pin may be connected directly to VIN if there is no suitable logic signal available to wake up the regulator.

When EN is being used as a system controlled enabling/disabling logic input and EN is kept high, the A8586 turns on and—provided there are no fault conditions—V_{OUT} will ramp to its final voltage in the soft-start time. When the EN is low, the A8586 will enter shutdown mode and draw less than 20 µA from the input.

When EN transitions low, the device waits approximately 150 µs before shutting down. This delay provides plenty of filtering to prevent the device from prematurely entering Sleep mode because of any small glitches that might couple onto the PCB trace or EN pin.

The enable input can also be used as a programmable UVLO. Connecting a resistor from VIN to enable and a second resistor from enable to ground implements this feature.



$$V_{IN(START)} = \frac{R1 + R2}{R2} V_{EN(H)} \quad (1)$$

$$V_{IN(STOP)} = \frac{R1 + R2}{R2} V_{EN(L)} \quad (2)$$

While there is an internal 1 µA current source that pulls EN up if enable is not used, it is recommended to connect it to VIN so the A8586 is automatically enabled once VIN exceeds VIN_{START}.

Undervoltage Lockout (UVLO)

An undervoltage lockout (UVLO) comparator monitors the voltage at the VIN pin and keeps the regulator disabled if the voltage is below the lockout threshold ($V_{IN(START)}$). The UVLO comparator incorporates enough hysteresis ($V_{IN(HYS)}$) to prevent on/off cycling of the regulator due to IR drops in the VIN path during heavy loading or during startup.

Low-Dropout Operation

The A8586 is designed to operate with one quarter the switching frequency when an off-time of less than $t_{OFF(MIN)}$ is demanded.

Internal Soft-Start

Inrush current to the regulator is controlled by the soft-start function. When the A8586 is enabled, after all faults are cleared, the soft-start will ramp upward from 0 to 0.8 V. The error amplifier output slews upward and, shortly thereafter, PWM switching will begin.

After the A8586 starts switching, the error amplifier will regulate the voltage at the FB pin to the internal soft-start voltage. After switching starts, the regulator output voltage will rise from 0 V to the set point determined by the feedback resistor divider (R_{FB1} and R_{FB2}). When the voltage of the internal soft-start reaches 0.8 V, the error amplifier will change mode and begin regulating to the A8586 internal reference, 792 mV.

To keep the inductor current under control, the A8586 operates with one quarter the switching frequency while V_{FB} remains below 200 mV, and half the switching frequency when V_{FB} is between 200 and 400 mV. The A8586 operates at the full switching frequency when V_{FB} is greater than 400 mV.

Pre-Biased Startup

If the output of the regulator is pre-biased to some voltage, the A8586 modifies the normal startup routine to prevent discharging the output capacitors. As described previously, the error amplifier usually becomes active when the soft-start voltage starts to ramp. If the output is pre-biased, the internal FB voltage is at some non-zero voltage. The COMP pin remains low and SW is tri-stated until the soft-start voltage rises above V_{FB}.

Thermal Shutdown

The A8586 protects itself from overheating by means of an internal thermal monitoring circuit. If the junction temperature exceeds the thermal shutdown threshold (T_{TSD}, 170°C typical), the voltages at the soft-start and COMP pins will be pulled to GND and the high-side MOSFET will be turned off. The A8586 will automatically restart when the junction temperature decreases more than the thermal shutdown hysteresis (T_{HYS}, 20°C typical).

MOSFET Driver and Bootstrap Capacitor

The position of the internal N-channel MOSFET requires special consideration when driving it. The source of this MOSFET can be either at close to VIN or close to GND. For that reason, a floating gate charge driver is required. This driver requires a voltage greater than V_{IN} to ensure the MOSFET can be turned on.

A simple charge pump—consisting of an internal charge circuit, an external capacitor (BST capacitor), and the freewheeling diode—is required to power the high side gate driver. The internal charge circuit is power by V_{IN}. When the SW node is sufficiently below V_{IN}, the charge circuit will charge the BST capacitor to around 5 V with respect to the SW node. This BST voltage is used to turn the MOSFET on. As SW node rises, the BST capacitor will maintain the BST pin at 5 V above SW, thereby ensuring sufficient voltage to keep the MOSFET on.

Also, the BST charge circuit incorporates its own UVLO of 1.8 V rising and 0.4 V hysteresis.

Current Comparator and Current Limit

A high-bandwidth current sense amplifier monitors the current in the high-side MOSFET. The current signal is supplied to the PWM comparator and the cycle-by-cycle current limiter.

The cycle-by-cycle maximum current of the internal power MOSFET is internally limited.

Overcurrent Protection (OCP) and Hiccup Mode

An OCP counter and hiccup mode circuit protect the buck regulator when the output of the regulator is shorted to ground or when the load is too high. When the soft-start ramp is active ($t < t_{SS}$), the OCP hiccup counter is disabled. Two conditions must be met for the OCP counter to be enabled and begin counting:

- $t > t_{SS}$, and
- V_{COMP} clamped at its maximum voltage (OCL = 1)

As long as these two conditions are met, the OCP counter remains enabled and counts pulses from the overcurrent comparator. If the COMP voltage decreases (OCL = 0), the OCP counter is cleared. If the OCP counter reaches the OCPLIM counts (120), a hiccup latch is set and the COMP pin is quickly pulled down by a relatively low resistance (4 kΩ). Switching is halted for 6 ms to provide time for the IC to cool down. After the hiccup off-time expires (6 ms), the soft-start ramp starts, marking the beginning of a new, normal soft-start cycle as described earlier. When the soft-start voltage crosses the effective output voltage, the error amplifier forces the voltage at the COMP pin to quickly slew upward and PWM switching resumes. If the short circuit at the regulator output remains, another hiccup cycle occurs. Hiccups repeat until the short circuit is removed or the converter is disabled. If the short circuit has been removed, the device soft-starts normally and the output voltage automatically recovers to the target level.

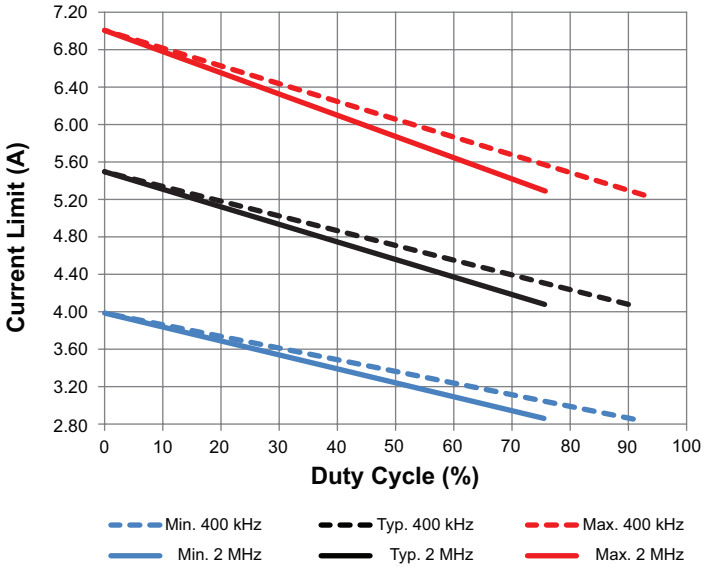


Figure 1: Current Limit vs. Duty Cycle

BOOT Capacitor Protection

The A8586 monitors the voltage across the BOOT capacitor to detect if the capacitor is missing or short-circuited. If the BOOT capacitor is missing, the regulator enters hiccup mode after 7 PWM cycles. If the BOOT capacitor is shorted, the regulator enters hiccup mode after 120 PWM cycles. For a BOOT fault, hiccup mode operates virtually the same as described previously for an output short circuit fault (OCP), having a hiccup off time of 6 ms followed by a soft start retry with repeated attempts until the fault clears. However, OCP is the only fault that is ignored during the soft start ramp time (t_{SS}). BOOT faults are a non-latched condition, so the device automatically recovers when the fault is corrected.

Freewheeling Diode Protection

If the freewheeling diode is missing or damaged (open), the SW pin is subject to unusually high negative voltages. This negative voltage may cause the device to malfunction and could lead to damage. The A8586 includes protection circuitry to detect when the freewheeling diode is missing. If the SW pin is below −1.25 V typically, for more than 50 ns typically, the device enters hiccup mode after detecting 1 missing diode fault. Also, if the freewheeling diode is shorted, the device experiences extremely high currents through the high-side MOSFET. If this occurs, the device enters hiccup mode after detecting 1 shorted diode fault.

Overvoltage Protection (OVP)

The A8586 provides an always-on overvoltage protection that monitors V_{OUT}, to protect against V_{OUT} rising up at light loads due to high side switch leakage. In this case, the high-side switch is forced off and the low-side switch continues to operate and can correct the OVP condition provided only a few milliamperes of pull-down current are required. When the condition causing the overvoltage is corrected, the regulator automatically recovers.

Pin-to-Ground and Pin-to-Pin Short Protections

The A8586 is designed to satisfy the most demanding automotive applications. For example, the device is carefully designed fundamentally to withstand a short circuit to ground at each pin without suffering damage. In addition, care was taken when defining the device pin-out to optimize protection against adjacent pin-to-pin short circuits. For example, logic pins and high-voltage pins are separated as much as possible. Inevitably, some low-voltage pins had to be located adjacent to high-voltage pins, but in these instances the low-voltage pins are designed to withstand increased voltages, with clamps and/or series input resistance, to prevent damage to the device.

Startup and Shutdown

If both V_{IN} and V_{EN} are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuits.

When the internal soft-start block is enabled, it first holds its SS output low to ensure the remaining circuits are ready and then slowly ramps up.

Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, power MOSFET is turned off first to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down.

Programmable Oscillator

A resistor (R_{FREQ}) from FREQ to ground sets the operation frequency of the A8586. The Applications Information section details the selection of this resistor.

Frequency Dithering (A8586, A8586-2)

The A8586 and A8586-2 include a dithering function, which changes the switching frequency within a certain frequency range. By shifting the switching frequency of the regulator in a triangle fashion around the programmed switching frequency, the overall system noise magnitude can be greatly reduced.

The dithering sweep is internally set at ±8%. The switching frequency will ramp from a low of 0.92 times the programmed frequency to a high of 1.08 times the programmed frequency. The rate or modulation at which the frequency sweeps is governed by an internal 12 kHz triangle pattern.

APPLICATIONS INFORMATION

Setting the Switching Frequency

The switching frequency (f_{SW}) of a regulator using the A8586 can be set using a resistor at the FREQ pin (R_{FREQ}). The recommended R_{FREQ} value for various switching frequencies can be obtained from either Table 1 or Figure 2 below:

Table 1: R_{FREQ} vs. f_{SW}

f_{SW} (MHz)	R_{FREQ} (kΩ)
4.0	15.4
3.5	20.0
3.0	26.1
2.5	34.0
2.0	45.3
1.5	68.1
1.0	105
0.8	140
0.5	232
0.3	402
0.2	619

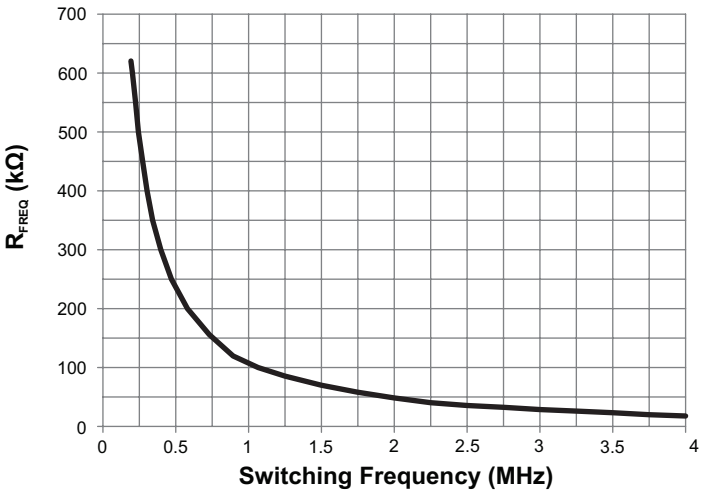


Figure 2: R_{FREQ} vs. f_{SW}

While the A8586 can switch at frequencies up to 4 MHz, care must be taken when operating above 2 MHz. The minimum controllable on-time for the A8586 is around 80 ns. This means that at higher frequencies, high input, and low output voltages, pulse skipping may be seen.

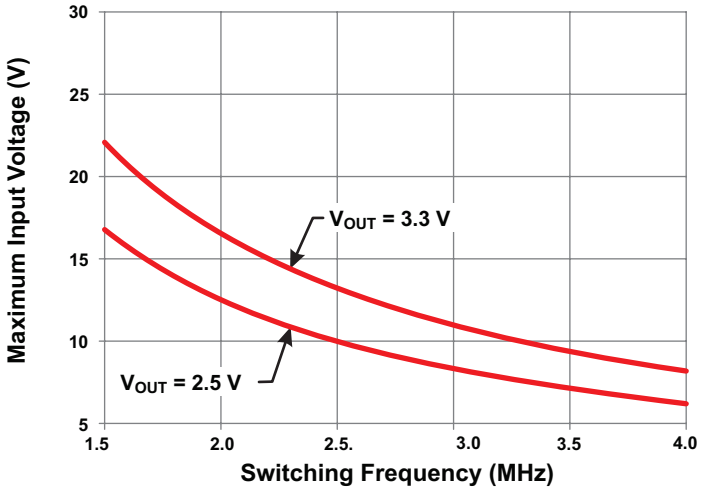


Figure 3: Recommended Switching Frequency vs. Maximum Input Voltage

Setting the Output Voltage

Many output voltages can be programmed by the selection of the right resistor pair, R_{FB1} and R_{FB2}. These resistors form a voltage divider between VOUT and GND with FB pin as the center. The voltage divider divides the output voltage down to the feedback voltage.

$$R_{FB1} = \frac{V_{OUT} - V_{FB}}{V_{FB}} \times R_{FB2} \qquad (3)$$

Table 2 below shows some typical resistor values selected from the E48 series for popular output voltages, using R_{FB2} = 40.2 kΩ. More accurate output voltage set points can be achieved by using a parallel combination for R_{FB1}.

Table 2: R_{FB1} vs. V_{OUT}, R_{FB2} = 40.2 kΩ

V_{OUT} (V)	R_{FB1} (kΩ)
1	10
1.2	20.5
1.5	34.8
1.8	51.1
2	59
2.5	86.6
2.7	95.3
3.3	127
5	215
12	562

Inductor

As with any buck converter, an inductor is required to supply constant current to the output load while being driven by the switched input voltage. Many factors determine the selection of this inductor, such as switching frequency, output/input voltage ratio, transient response, and ripple current. A larger value inductor will result in less ripple current that will result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current.

A good rule for determining the inductance to use is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum output current (I_{OUTMAX}). Also, make sure that the peak inductor current during normal operation is below the maximum switch current limit. The inductance value can be calculated by:

$$L_O = \frac{V_{OUT}}{f_{SW} \times \Delta I_L}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \qquad (4)$$

where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_{SW} is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current = $0.3 \times I_{OUTMAX}$.

A second constraint on inductor value would be loop stability at duty cycles greater than 50%. The A8586 uses current-mode control and includes internal slope compensation (S_E). Based on the S_E value, recommended inductance for stability would be:

$$L_O \geq \frac{V_{OUT}}{S_E}\left(1 - 0.18 \times \frac{V_{IN(MIN)}}{V_{OUT}}\right) \qquad (5)$$

Slope compensation (S_E) will vary with switching frequency. S_E can be calculated using equation 6.

$$S_E = S_{E(2MHz)} \times \left(\frac{\frac{1}{2\ MHz} - 100\ ns}{\frac{1}{f_{SW}} - 100\ ns}\right) \qquad (6)$$

Choose an inductor that will not saturate under the maximum inductor peak current, which is the current limit of the A8586, over the full temperature range.

Also, ensure that the peak current at I_{OUTMAX} does not exceed the current limit. The peak inductor current can be calculated by:

$$I_{LPK} = I_{OUTMAX} + \frac{V_{OUT}}{2 \times f_{SW} \times L_O}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \qquad (7)$$

Freewheeling Diode

The freewheeling diode allows the current in the inductor to flow to the load when the high-side switch is off. To reduce losses due to the diode forward voltage and recovery times, use a Schottky diode.

Choose a diode with a maximum reverse voltage rating greater than the maximum input voltage and a current rating greater than the maximum load current.

Input Capacitor

Three factors should be considered when choosing the input capacitors. First, they must be chosen to support the maximum expected input voltage with adequate design margin. Second, their rms current rating must be higher than the expected rms input current to the regulator. Third, they must have enough capacitance and a low enough ESR to limit the input voltage dv/dt to something much less than the hysteresis of the VIN pin UVLO circuitry (350 mV (typ)) at maximum loading and minimum input voltage.

The input capacitor(s) must limit the voltage deviations at the VIN pin to something significantly less than the A8586 VIN pin UVLO hysteresis during maximum load and minimum input voltage. The minimum input capacitance can be calculated as follows:

$$C_{IN} > \frac{I_{OUT}}{0.85 \times f_{SW} \times \Delta V_{IN}} \times \frac{V_{OUT}}{V_{IN}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \qquad (8)$$

where ΔV_{IN} is chosen to be much less than the hysteresis of the VIN pin, UVLO comparator ($\Delta V_{IN} \leq 100$ mV is recommended) and f_{SW} is the nominal PWM switching frequency.

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current.

Output Capacitor

The output capacitors filter the output voltage to provide an acceptable level of ripple voltage and they store energy to help maintain voltage regulation during a load transient. The voltage rating of the output capacitors must support the output voltage with sufficient design margin.

The output voltage ripple (ΔV_{OUT}) is a function of the output capacitor parameters: C_{OUT}, ESR, and ESL:

$$\Delta V_{OUT} = \Delta I_L \times ESR + \frac{V_{IN} - V_{OUT}}{L_O} \times ESL + \frac{\Delta I_L}{8 f_{SW} C_{OUT}} \quad (9)$$

where L_O is the inductor value, ESR is the equivalent series resistance of the output capacitor, and ESL is its equivalent series inductance.

The type of output capacitors will determine which terms of equation 9 are dominant. For ceramic output capacitors the ESR and ESL are virtually zero, so the output voltage ripple will be dominated by the third term of equation 10:

$$\Delta V_{OUT} = \frac{\Delta I_L}{8 f_{SW} C_{OUT}} \quad (9)$$

To reduce the voltage ripple of a design using ceramic output capacitors, simply increase the total capacitance, reduce the inductor current ripple (that is, increase the inductor value), or increase the switching frequency.

For electrolytic output capacitors, the value of capacitance will be relatively high, so the third term in equation 9 will be very small. The output voltage ripple will be determined primarily by the first two terms of equation 9.

$$\Delta V_{OUT} = \Delta I_L \times ESR + \frac{V_{IN} - V_{OUT}}{L_O} \times ESL \quad (11)$$

To reduce the voltage ripple of a design using electrolytic output capacitors, simply decrease the equivalent ESR and ESL by using a high(er) quality capacitor, add more capacitors in parallel, or reduce the inductor current ripple (that is, increase the inductor value).

The ESR of some electrolytic capacitors can be quite high, therefore choose a quality capacitor that clearly documents the ESR, or the total impedance, in the datasheet. Also, the ESR of electrolytic capacitors usually increases significantly at cold temperatures, by as much as 10×, which increases the output voltage ripple and, in most cases, significantly reduces the stability of the system.

The transient response of the regulator depends on the number and type of output capacitors. In general, minimizing the ESR of the output capacitance will result in a better transient response. The ESR can be minimized by simply adding more capacitors in parallel or by using higher quality capacitors. At the instant of a fast load transient (di/dt), the output voltage will change by the amount.

$$\Delta V_{OUT} = \Delta I_{OUT} \times ESR + \frac{di}{dt} \times ESL \quad (12)$$

After the load transient occurs, the output voltage will deviate from its nominal value for a short time. This time will depend on the system bandwidth, the output inductor value, and output capacitance. Eventually, the error amplifier will bring the output voltage back to its nominal value.

The speed at which the error amplifier will bring the output voltage back to its set point will depend mainly on the closed-loop bandwidth of the system. A higher bandwidth usually results in a shorter time to return to the nominal voltage. However, a higher bandwidth system may be more difficult to obtain acceptable gain and phase margins. Selection of the compensation components (R_Z, C_Z, C_P) are discussed in more detail in the Compensation Components section of this datasheet.

Low-I_Q PFM Output Voltage Ripple Calculation (A8586 Only)

After choosing an output inductor and output capacitor(s), it is important to calculate the output voltage ripple ($\Delta V_{OUT(PFM)}$) during Low-I_Q PFM mode. With ceramic output capacitors, the output voltage ripple in PWM mode is usually negligible, but that is not the case during Low-I_Q PFM mode.

The PFM mode comparator requires about 10 mV or greater of voltage ripple on the VOUT pin and generates groups of pulses to meet this requirement. However, if a single pulse results in a voltage ripple greater than 10 mV, then the voltage ripple would be dictated by that single pulse. To calculate the voltage ripple from that single pulse, first the peak inductor current must be calculated with slope compensation accounted for. The $I_{PEAK(LO_IQ)}$ specification does not include slope compensation; therefore, the peak inductor current operating point is calculated as follows:

$$I_{PEAK_L} = \frac{I_{PEAK(LO_IQ)}}{1 + \frac{S_E \times L_O}{V_{IN} - V_{OUT}}} \quad (13)$$

Then, calculate the MOSFET on-time ($t_{ON(Q)}$) and freewheeling diode on-time ($t_{ON(D)}$) (Figure 3). The on-time is defined as the time it takes for the inductor current to reach I_{PEAK_L}:

$$t_{ON(Q)} = \frac{I_{PEAK_L} \times L_O}{V_{IN} - V_{OUT} - I_{PEAK_L} \times (R_{DS(ON)HS} + L_{O(DCR)})} \quad (14)$$

where $R_{DS(on)}$ is the on-resistance of the internal high-side MOSFET (150 mΩ typical) and $L_{O(DCR)}$ is the DC resistance of the

output inductor (L_O). During this rising time interval, the length of time for the inductor current to rise from 0 A to I_{OUT} is:

$$t_1 = \frac{I_{OUT} \times L_O}{V_{IN} - V_{OUT} - I_{PEAK_L} \times (R_{DS(ON)HS} + L_{O(DCR)})} \quad (15)$$

The freewheeling diode on-time is defined as the time it takes for the inductor current to decay from I_{PEAK_L} to 0 A:

$$t_{ON(D)} = \frac{I_{PEAK_L} \times L_O}{V_{OUT} + V_F} \quad (16)$$

During this falling time interval, the length of time for the inductor current to fall from I_{OUT} to 0 A is:

$$t_2 = \frac{I_{OUT} \times L_O}{V_{OUT} + V_F} \quad (17)$$

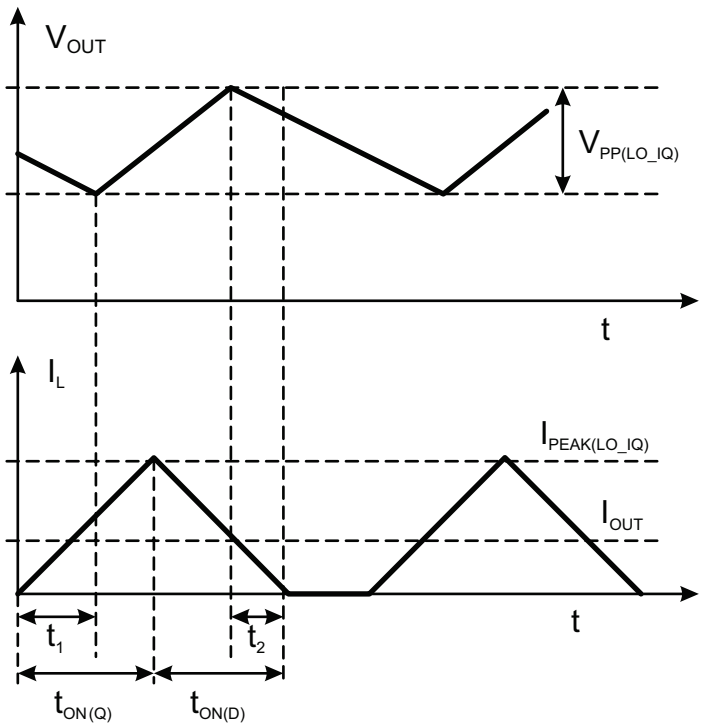


Figure 4: Calculating the Output Ripple Voltage in PFM Mode (A8586 Only)

Given the peak inductor current (I_{PEAK_L}) and the rise and fall times ($t_{ON(Q)}$ and $t_{ON(D)}$) for the inductor current, the output voltage ripple can be calculated for a signal pulse as follows:

$$V_{PP(LO_IQ)} = \frac{I_{PEAK_L} - I_{OUT}}{2 \times C_{OUT}} (t_{ON(Q)} + t_{ON(D)} - t_1 - t_2) \quad (18)$$

If $V_{PP(LO_IQ)}$ is greater than the ~10 mV ripple that the PFM comparator requires, then the output capacitance or inductor can be adjusted to reduce the PFM mode voltage ripple. In PFM mode, decreasing the inductor value reduces the PFM ripple, but may negatively impact the PWM voltage ripple, maximum load current in PWM mode, or change the mode of operation from CCM to DCM.

If $V_{PP(LO_IQ)}$ is less than the ~10 mV requirement, the A8586 operates with multiple pulses at the PWM frequency to meet the ripple requirement. The fixed frequency operation may result in DCM or CCM operation during the multiple pulses.

Compensation Components

A8586 employs current-mode control for easy compensation and fast transient response. The system stability and transient response are controlled through the COMP pin. COMP pin is the output of the internal transconductance error amplifier. A series capacitor-resistor combination sets a pole-zero pair to control the characteristics of the control system. The DC voltage gain, A_{VDC}, of the feedback loop is given by:

$$A_{VDC} = \frac{V_{OUT}}{I_{OUT}} \times G_{CS} \times A_{VOL} \times \frac{V_{FB}}{V_{OUT}} \quad (19)$$

where A_{VOL} is the error amplifier voltage gain, 1000 V/V and G_{CS} is the current sense transconductance, 9 A/V.

The system has two noteworthy poles. One is due to the compensation capacitor (C_Z) and the error amplifier output resistor. The other is due to the output capacitor and the load resistor. These poles are located at:

$$f_{P1} = \frac{g_m}{2\pi \times C_Z \times A_{VOL}} \quad (20)$$

$$f_{P2} = \frac{I_{OUT}}{2\pi \times C_{OUT} \times V_{OUT}} \quad (21)$$

where g_m is the error amplifier transconductance, 60 µA/V.

The system has one noteworthy zero. This is due to the compensation capacitor (C_Z) and the compensation resistor (R_Z). This zero is located at:

$$f_Z = \frac{1}{2\pi \times C_Z \times R_Z} \quad (22)$$

The system may have another zero, if the output capacitor has a large capacitance and/or a high ESR value. The zero, due to the ESR and capacitance of the output capacitor, is located at:

$$f_Z = \frac{1}{2\pi \times C_{OUT} \times ESR} \quad (23)$$

In this case (as shown in the simplified schematic on page 1), a third pole set by the optional compensation capacitor (C_P) and the compensation resistor (R_Z) is used to compensate the effect of the ESR zero on the loop gain. This pole is located at:

$$f_{P3} = \frac{1}{2\pi \times C_P \times R_Z} \quad (24)$$

The goal of compensation design is to shape the converter transfer function to get a desired loop gain. The system crossover frequency where the feedback loop has unity gain is important. Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies could cause the system to be unstable. A good rule of thumb is to set the crossover frequency to approximately one tenth of the switching frequency. Table 3 lists typical values of compensation components for some standard output voltages with various output ceramic capacitors and inductors. The values of the compensation components have been optimized for fast transient responses and good stability.

Table 3: Compensation Values for Typical Output Voltage/ Capacitor Combinations with f_{SW} = 500 kHz

V_{OUT} (V)	L_O (µH)	C_{OUT} (µF)	R_Z (kΩ)	C_Z (pF)	C_P
1.8	4.7	47	105	100	None
2.5	4.7 - 6.8	22	54.9	220	None
3.3	6.8 -10	22	68.1	220	None
5	15 - 22	22	100	150	None
12	22 - 33	22	147	150	None

To optimize the compensation components for conditions not listed in Table 3, the following procedure can be used.

1. Choose the compensation resistor (R_Z) to set the desired crossover frequency (f_C). Determine the R_Z value by the following equation:

$$R_Z = \frac{2\pi \times C_{OUT} \times f_C}{g_m \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}} \quad (25)$$

2. Choose the compensation capacitor (C_Z) to achieve the desired phase margin. For applications with typical inductor values, setting the compensation zero (f_{Z1}) below one fourth of the crossover frequency provides sufficient phase margin. Determine the C_Z value by the following equation:

$$C_Z > \frac{4}{2\pi \times R_Z \times f_C} \quad (26)$$

3. Determine if the second compensation capacitor (C_P) is required. It is required if the ESR zero of the output capacitor is located at less than half of the switching frequency or the following relationship is valid:

$$\frac{1}{2\pi \times C_{OUT} \times ESR} < \frac{f_{SW}}{2} \quad (27)$$

If this is the case, then add the second compensation capacitor (C_P) to set the pole f_{P3} at the location of the ESR zero. Determine the C_P value by the equation:

$$C_P = \frac{C_{OUT} \times ESR}{R_Z} \quad (28)$$

PCB COMPONENT PLACEMENT AND ROUTING

A good PCB layout is critical if the A8586 is to provide clean, stable output voltages. Follow these guidelines to ensure a good PCB layout. Figure 5 shows a typical A8586-based schematic with the critical power paths/loops. Figure 6 shows an example PCB component placement and routing with the same critical power paths/loops as shown in the schematic.

1. By far, the highest di/dt in the asynchronous buck regulator occurs at the instant the high-side MOSFET turns on, and the ceramic input capacitors through the high-side MOSFET and into the asynchronous diode to ground must be minimized. Ideally these components are all connected using only the top metal layer (that is, do not use vias to other power/signal layers).
2. When the high-side MOSFET is on, current flows from the input supply and capacitors, through the high-side MOSFET, into the load via the output inductor, and back to ground. This loop should be minimized and have relatively wide traces.
3. When the high-side MOSFET is off, free-wheeling current flows from ground, through the asynchronous diode, into the load via the output inductor, and back to ground. This loop should be minimized and have relatively wide traces.
4. The voltage on the SW node transitions from 0 V to VIN very quickly and is the root cause of many noise issues. It is best to place the asynchronous diode and output inductor close to the A8586 to minimize the size of the SW polygon. Also, keep low level analog signals (like FB and COMP) away from the SW polygon.
5. Place the feedback resistor divider (R6 and R4) very close to the FB pin. Ground this resistor divider as close as possible to the A8586.
6. To have the highest output voltage accuracy, the output voltage sense trace (from VOUT to R6) should be connected as close as possible to the load.
7. Place the compensation components (R5, C6, and C7) as close as possible to the COMP pin. Place vias to the GND plane as close as possible to these components.
8. Place the bootstrap capacitor (C5) near the BST pin and keep the routing from this capacitor to the SW polygon as short as possible.
9. When connecting the input and output ceramic capacitors, use multiple vias to GND and place the vias as close as possible to the pads of the components.
10. To minimize PCB losses and improve system efficiency, the input and output traces should be as wide as possible and be duplicated on multiple layers, if possible.
11. The thermal pad under the A8586 must connect to the GND plane using multiple vias. More vias will ensure the lowest junction temperature and highest efficiency.
12. EMI/EMC issues are always a concern. Allegro recommends having component locations for an RC snubber from SW to ground. The resistor should be 1206 size and connected to ground plane to aid thermal dissipation.

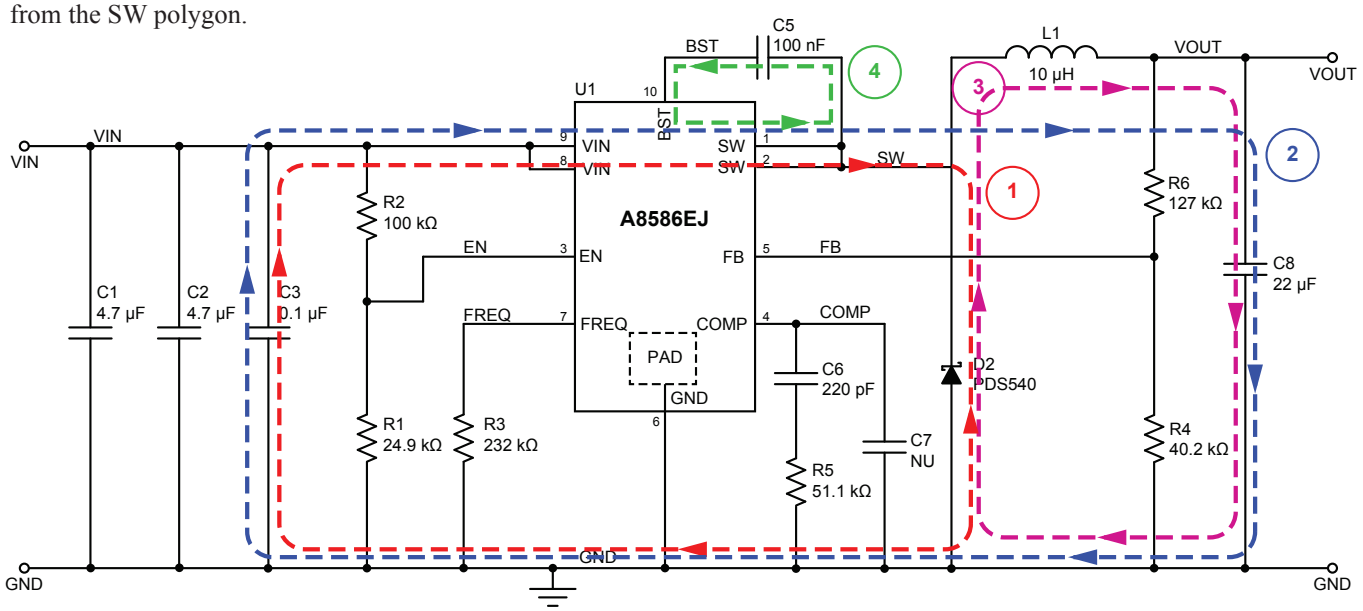


Figure 5: Typical Buck Converter with Critical Paths/Loops Shown

LOOP 1 (RED)

At the instant the internal MOSFET turns on, Schottky diode D2, which is very capacitive, must be very quickly shut off (only 5 to 15 ns of charging time). This spike of charging current must come from the local input ceramic capacitor, C3. This spike of current is quite large and will be an EMI/EMC issue if loop 1 (red) is not minimized. Therefore, the input capacitor C3 and Schottky diode D1 must be placed be on the same (top) layer, be located near each other, and be grounded at virtually the same point on the PCB.

LOOP 2 (MAGENTA)

When the internal MOSFET is off, free-wheeling inductor current must flow from ground through diode D2 (SW will be at –Vf), into the output inductor, out to the load and return via ground. While the MOSFET is off, the voltage on the output capacitors decreases. The output capacitors and Schottky diode D2 should be placed on the same (top) layer, be located near each other, and be sharing a good, low inductance ground connection.

LOOP 3 (BLUE)

When the MOSFET is on, current will flow from the input supply and input capacitors through the output inductor and into the load and the output capacitors. At this time the voltage on the output capacitors increases.

LOOP 4 (GREEN)

When the MOSFET is turned on, gate current is sourced from the boot capacitor C5. This current can have significant di/dt levels. The loop created by the A8586 BST pin, C5 and A8586 SW pin should be minimized.

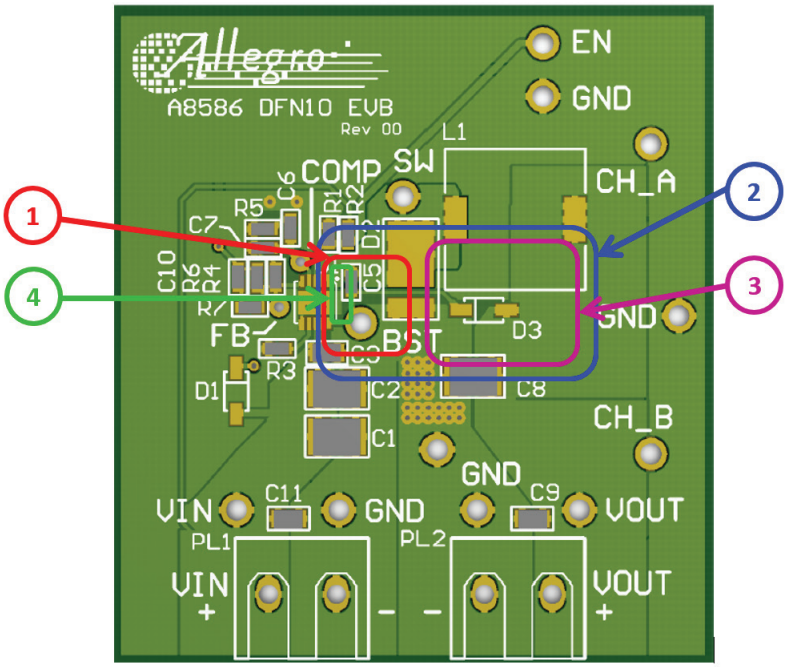


Figure 6: Example PCB Component Placement and Routing

PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference DWG 2860)
Dimensions in millimeters – NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown

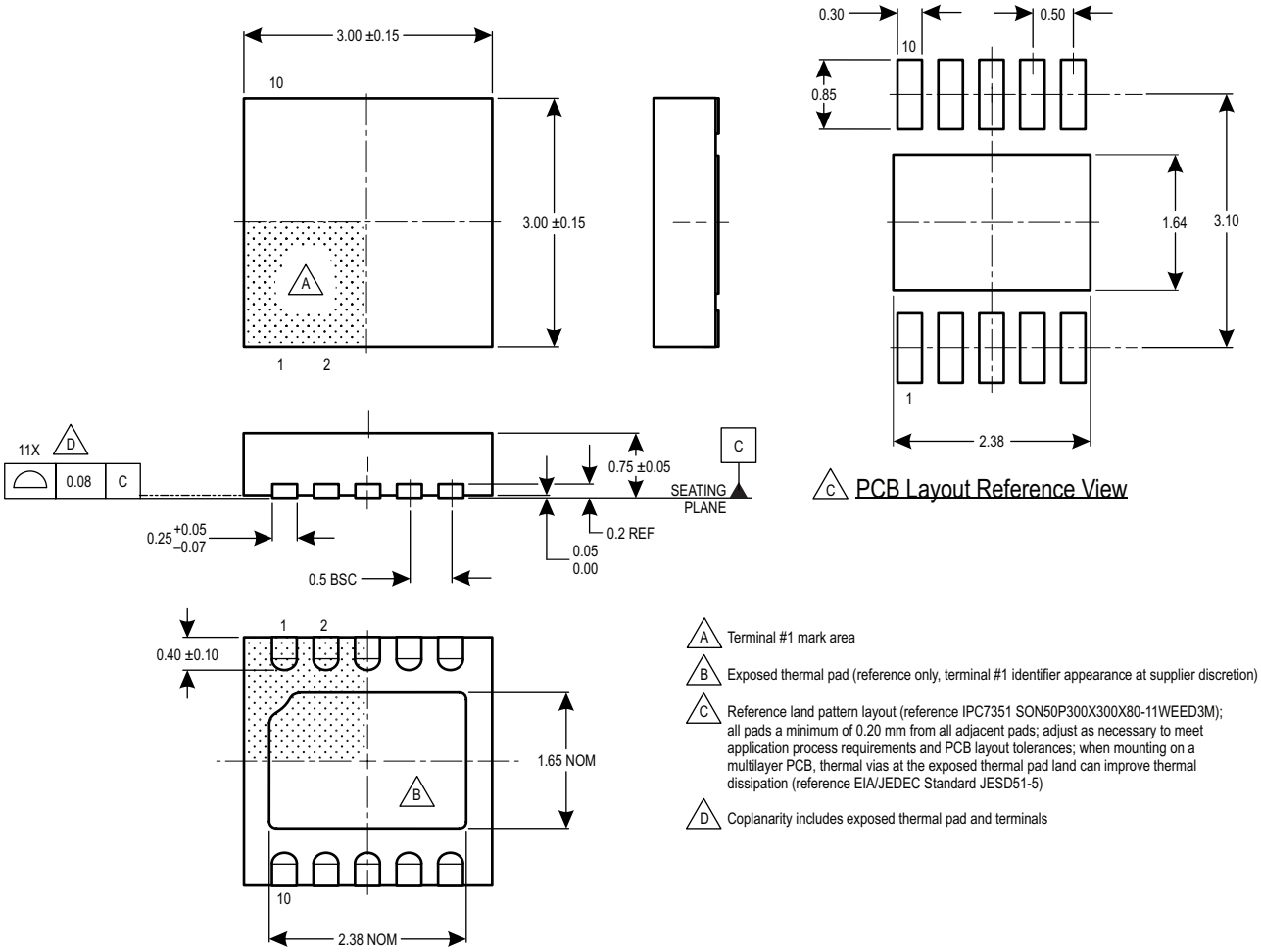


Figure 7: Package EJ, 10-Pin DFN with Exposed Thermal Pad

For Reference Only – Not for Tooling Use

(Reference DWG-2869)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

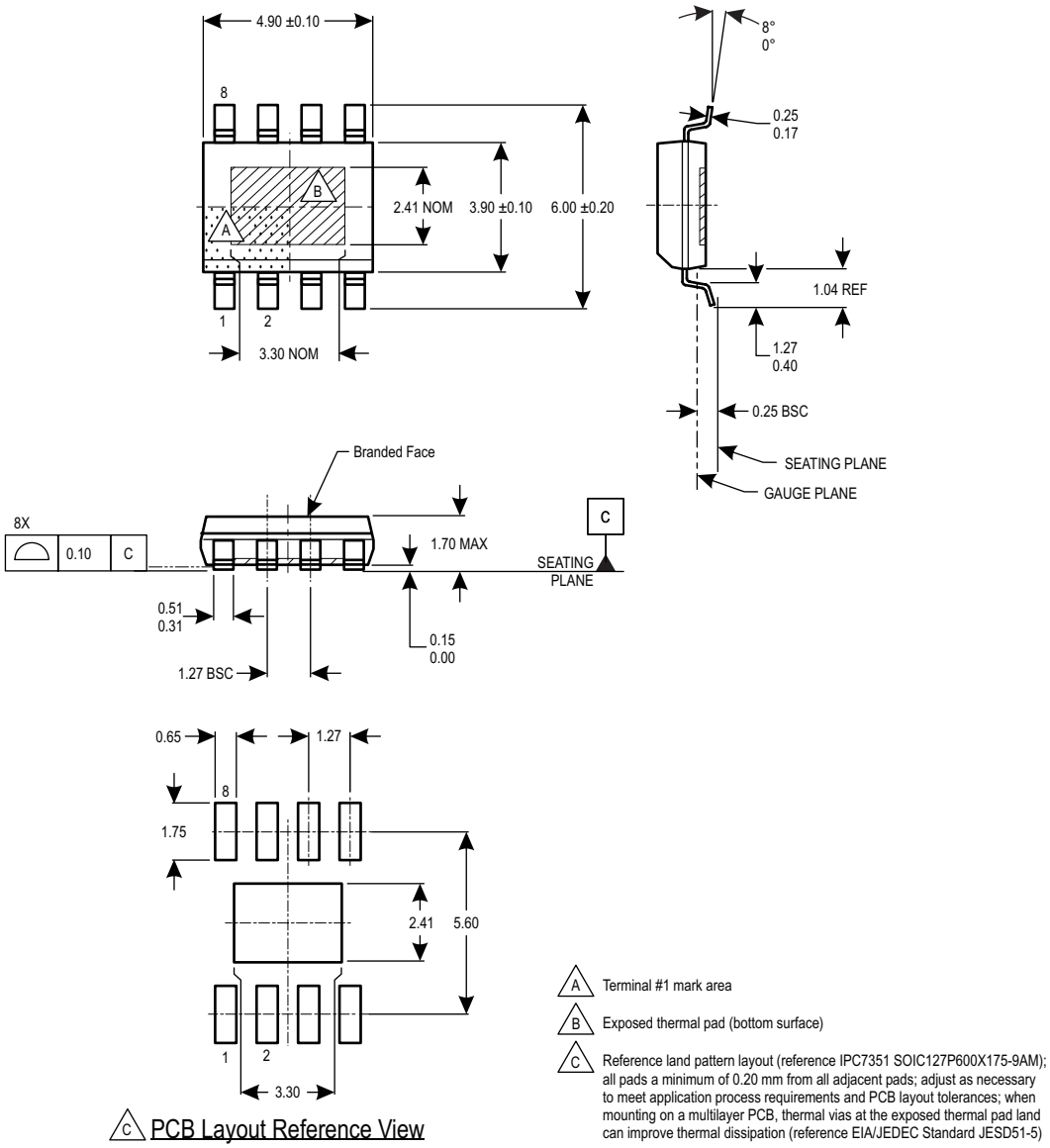


Figure 8: Package LJ, 8-Pin SOIC with Exposed Thermal Pad

Revision History

Number	Date	Description
–	December 2, 2014	Initial release.
1	March 29, 2016	Updated Selection Guide table (page 2); minor editorial changes.
2	August 19, 2016	Added PCB Component Placement and Routing section (pages 15-16).
3	October 4, 2016	Removed “Operating at Low Input Voltages” section (page 8 and 14).
4	January 17, 2017	Corrected EJ package outline drawing (page 17). Updated bootstrap capacitor value (pages 4 and 15).

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