Advance Information

Am79C980

Integrated Multiport Repeater (IMR)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- CMOS device features high integration and low power with a single +5 V supply
- Repeater functions conform to IEEE 802.3c Repeater Unit specifications
- Eight integral 10BASE-T transceivers utilize the required pre-distortion transmission technique
- Attachment Unit Interface (AUI) port allows connectivity with 10BASE-5 (Ethernet) and 10BASE-2 (Cheapernet) networks
- Expandable to increase number of repeater ports
- All ports can be separately isolated (partitioned) in response to excessive collision conditions or fault conditions
- Network management and optional features are accessible through a dedicated serial management port
- Twisted Pair Link Test capability conforming to the 10BASE-T standard. The receive Link Test Function can be optionally disabled through the management port to facilitate interoperability with devices that don't implement the Link Test Function
- Programmable option of Automatic Polarity Detection and Reversal enables the network to function even with polarity reversals due to wiring errors
- Full re-timing and re-conditioning of all repeater signals

GENERAL DESCRIPTION

The Integrated Multiport Repeater (IMR) is a VLSI integrated circuit that provides a system level solution to designing a 10BASE-T Repeater. The device integrates the Repeater functions specified by section 9 of the IEEE 802.3 standard and Twisted Pair Transceiver functions conforming to the 10BASE-T standard (draft 10). The Am79C980 provides eight integral Twisted Pair Medium Attachment Units (MAUs) and an Attachment Unit Interface (AUI) port in an 84-pin Plastic Leaded Chip Carrier (PLCC).

A network based on the 10BASE-T standard uses unshielded twisted pair cables, therefore providing an economical solution to networking by allowing the use of existing telephone wiring.

The total number of ports per repeater unit can be increased by connecting multiple IMR devices through their expansion ports, hence minimizing the total cost per node. Furthermore, a general purpose Attachment Unit Interface (AUI) provides connection capability to 10BASE-5 (Ethernet) and 10BASE-2 (Cheapernet) networks. Network management and test functions are provided through TTL compatible I/O pins.

The device is fabricated in CMOS technology and requires a single +5 V supply.

RELATED AMD PRODUCTS

Part No.	Description
Am79C900	Integrated Local Area Communications Controller (ILACC)
Am7990	Local Area Network Controller for Ethernet (LANCE)
Am7992B	Serial Interface Adapter (SIA)
Am79C98	Twisted Pair Ethernet Transceiver (TPEX)
Am7996	IEEE 802.3/Ethernet/Cheapernet Transceiver

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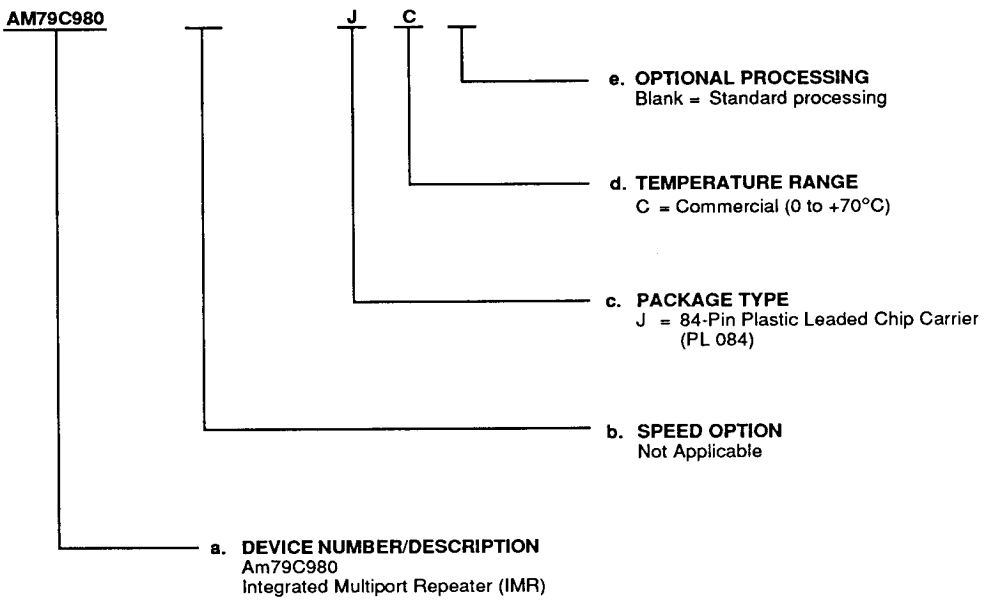
ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

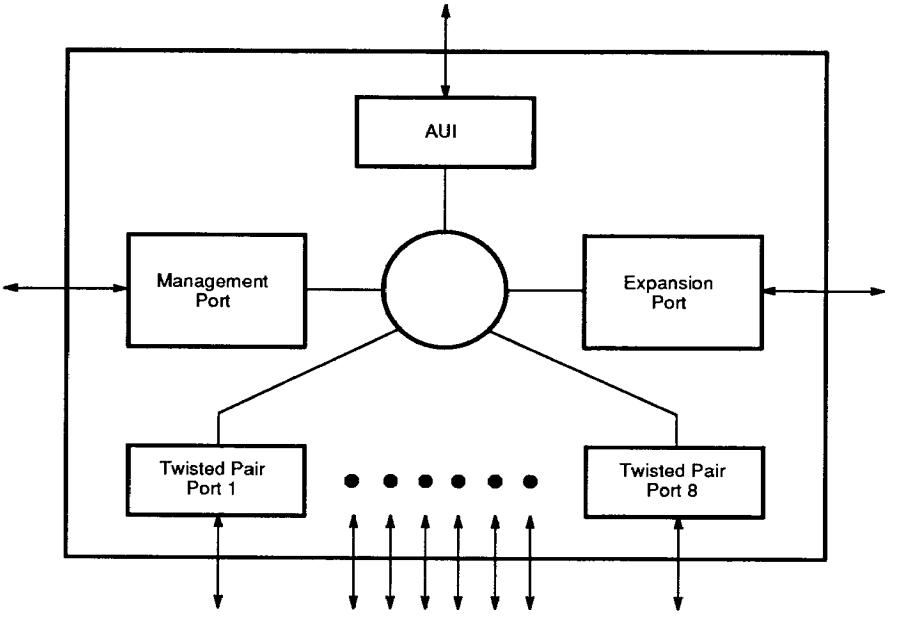


Valid Combinations	
AM79C980	JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

LOGIC DIAGRAM



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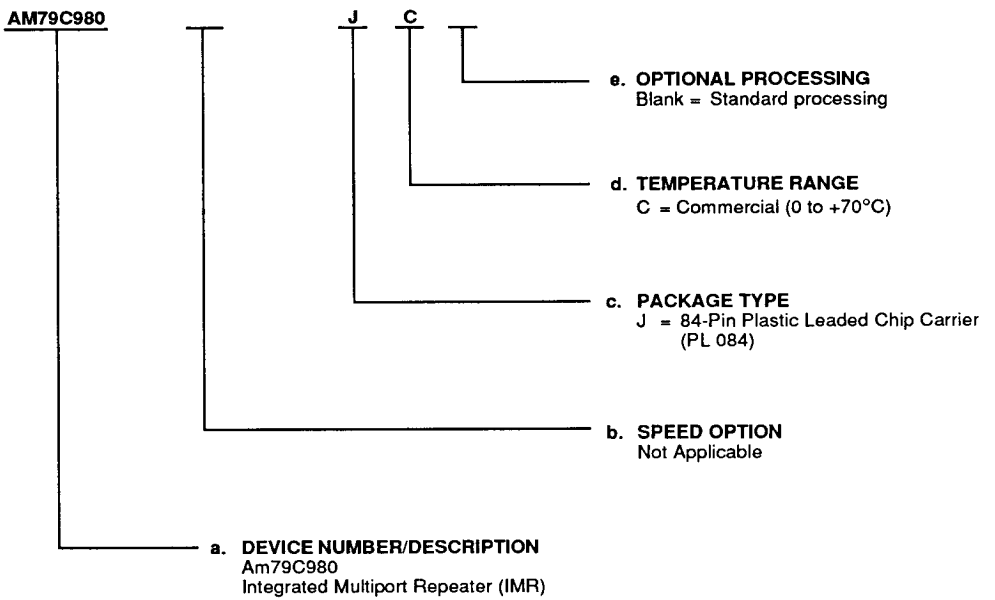

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PIN DESCRIPTION

TXD+, TXD–
Transmit Data

Output

10BASE-T port differential drivers (8 ports)

TXP+, TXP–
Transmit Pre-distort

Output

10BASE-T transmit waveform pre-distortion control differential outputs (8 ports)

RXD+, RXD–
Receive Data

Input

10BASE-T port differential receive inputs (8 ports)

DO+, DO–
Data Out

Output

AUI port differential driver

DI+, DI–
Data In

Input

AUI port differential receiver

CI+, CI–
Control In

Input

AUI port differential receiver

X_1
Crystal 1

Crystal Connection

The internal clock generator uses a 20 MHz crystal attached to pins X_1 and X_2. Alternatively, an external 20 MHz TTL clock signal can be used to drive this pin.

X_2
Crystal 2

Crystal Connection

The internal clock generator uses a 20 MHz crystal attached to pins X_1 and X_2. If an external clock source is used, this pin should be left unconnected.

$\overline{REQ}$
Request

Output, Active LOW

This pin is driven LOW when the IMR is active. An active IMR is defined as an IMR which has one or more ports receiving or colliding and/or in the state where it is still transmitting data from the internal FIFO. The assertion of this signal signifies that the IMR is requesting the use of the DAT and JAM lines for the transfer of repeated data and collision status to other IMRs.

$\overline{ACK}$
Acknowledge

Input, Active LOW

When this input is asserted, it signals to the requesting IMR that it may control the DAT and JAM pins. If the IMR is not requesting control of the DAT line ($\overline{REQ}$ pin HIGH), then the assertion of the $\overline{ACK}$ signal indicates the presence of valid collision status on the JAM or valid data on the DAT line.

$\overline{COL}$
Expansion Collision

Input, Active LOW

When this input is asserted by an external arbiter, it signifies that more than one IMR is active and that each IMR should generate Collision Jam Sequence independently.

DAT
Data

Input/Output

When there is a single IMR active (in a multiple IMR design), the IMR with both $\overline{REQ}$ and $\overline{ACK}$ pins asserted drives the DAT line with NRZ data. The pin is an input when only the $\overline{ACK}$ signal is asserted, and is in a high impedance state if neither $\overline{REQ}$ or $\overline{ACK}$ is asserted.

JAM
Jam

Input/Output

This pin is an output on the single active IMR ($\overline{REQ}$ and $\overline{ACK}$ both asserted). The active IMR drives the JAM pin HIGH to indicate that it is in a Collision state. The pin is an input when only the $\overline{ACK}$ signal is asserted, and is in a high impedance state if neither $\overline{REQ}$ or $\overline{ACK}$ is asserted.

CRS
Carrier Sense

Output

The states of the internal carrier sense signals for the AUI port and the eight twisted pair ports is serially output on this pin continuously. The output serial bit stream is synchronized to the X_1 clock.

STR
Store

Output

This pin goes HIGH for two X_1 clock cycle times after the nine carrier sense bits are output on the CRS pin. Note that the carrier sense signals arriving from each port are latched internally, so that an active transition is remembered between samples. The accuracy of the carrier sense signals produced in this manner is 10 bit times (one microsecond).

SI
Serial In
Input

Test/Management serial input port.

SO
Serial Out
Output

Test/Management serial output port.

SCK
Serial Clock
Input

Serial input data is clocked in on the rising edge of the signal on this pin.

TEST
Test Pin
Input, Active HIGH

This pin should be tied LOW for normal operation. If this pin is driven HIGH, then the IMR is configured to be programmed for Loopback Mode.

$\overline{RST}$
Reset
Input, Active LOW

Driving this pin LOW resets the internal logic of the IMR.

AV_{DD}
Analog Power
Power Pin

These pins supply the +5 V to the analog portions of the IMR.

AV_{SS}
Analog Ground
Ground Pin

These pins are the 0 V reference for the analog portions of the IMR.

DV_{DD}
Digital Power
Power Pin

These pins supply the +5 V to the logic portions of the IMR.

DV_{SS}
Digital Ground
Ground Pin

These pins are the 0 V reference for the logic portions of the IMR.