UCC2732x-Q1 Single 9-A High-Speed Low-Side MOSFET Driver With Enable

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C6
- Industry-Standard Pinout With Addition of Enable Function
- High Peak-Current Drive Capability of ±9 A at the Miller Plateau Region Using TrueDrive™ Technology
- Efficient Constant-Current Sourcing Using a Unique Bipolar and CMOS Output Stage
- TTL and CMOS-Compatible Inputs Independent of Supply Voltage
- 20-ns Typical Rise and 15-ns Typical Fall Times With 10-nF Load
- Typical Propagation Delay Times of 25 ns With Input Falling and 35 ns With Input Rising
- 4-V to 15-V Supply Voltage
- Available in Thermally Enhanced MSOP PowerPAD™ Package
- TrueDrive Output Architecture Using Bipolar and CMOS Transistors in Parallel

2 Applications

- Switch-Mode Power Supplies
- DC-DC Converters
- Motor Controllers
- Line Drivers
- Class-D Switching Amplifiers
- Pulse Transformer Driver

3 Description

The UCC2732x-Q1 family of high-speed drivers delivers 9 A of peak drive current in an industry-standard pinout. These drivers can drive large MOSFETs for systems requiring extreme Miller current due to high dV/dt transitions. This eliminates additional external circuits and can replace multiple components to reduce space, design complexity, and assembly cost. Two standard logic options are offered, inverting (UCC27321-Q1) and noninverting (UCC27322-Q1).

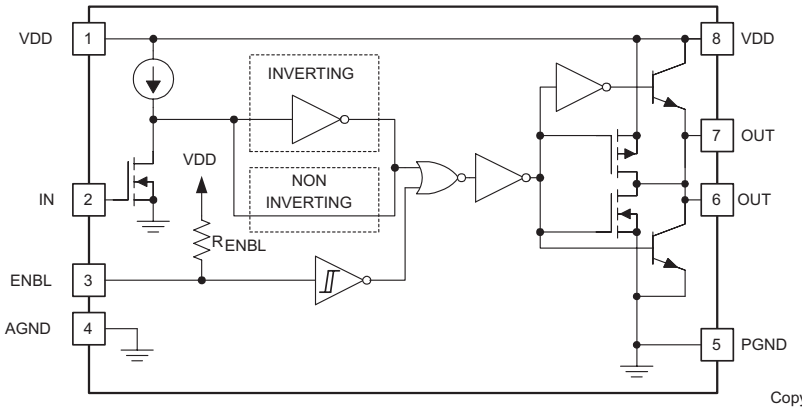
Using a design that minimizes shoot-through current, the outputs of these devices can provide high gate drive current where it is most needed at the Miller plateau region during the MOSFET switching transition. A unique hybrid-output stage paralleling bipolar and MOSFET transistors (TrueDrive) allows efficient current delivery at low supply voltages. With this drive architecture, UCC2732x-Q1 can be used in industry standard 6-A, 9-A, and many 12-A driver applications. Latch-up and ESD protection circuits are also included. Finally, the UCC2732x-Q1 provides an enable (ENBL) function to better control the operation of the driver applications. ENBL is implemented on pin 3, which was previously left unused in the industry-standard pinout. It is internally pulled up to VDD for active-high logic and can be left open for standard operation.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC27321-Q1, UCC27322-Q1	SOIC (8)	6.00 mm × 4.90 mm
UCC27322-Q1	MSOP-PowerPAD (8)	4.90 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



INPUT/OUTPUT TABLE

	ENBL	IN	OUT
INVERTING UCC27321-Q1	0	0	0
	0	1	0
	1	0	1
	1	1	0
NON INVERTING UCC27322-Q1	0	0	0
	0	1	0
	1	0	0
	1	1	1

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (January 2012) to Revision D — **Page**

- Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed UCC3732x to UCC2732x-Q1 throughout document ... 1
- Deleted *Ordering Information* table; see POA added at the end of the data sheet ... 1
- Changed table descriptions for AGND and PGND ... 3
- Updated values in the *Thermal Information* table to align with JEDEC standards ... 4
- Changed x-axis values from 1, 10, 100 to 0.1, 1, 10 in Rise Time vs Load Capacitance graph ... 7
- Deleted note reference [1] ... 12

Changes from Revision B (January 2011) to Revision C — **Page**

- Changed enable impedance maximum from 135 kΩ to 145 kΩ ... 5

5 Description (Continued)

In addition to 8-pin SOIC (D) package offerings, the UCC2732x-Q1 also comes in the thermally enhanced but tiny 8-pin MSOP-PowerPAD (DGN) package. The PowerPAD package drastically lowers the thermal resistance to extend the temperature operation range and improve long-term reliability.

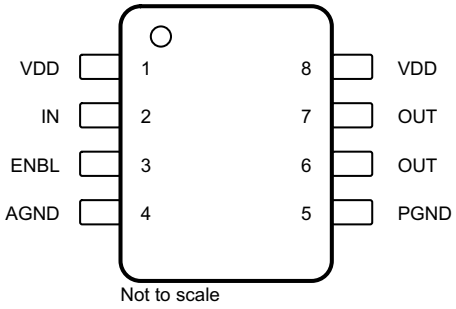
6 Device Comparison Table

Table 1. Related Products

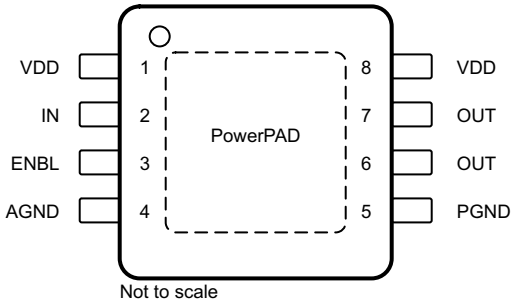
PRODUCT	DESCRIPTION	PACKAGE
UCC2742x-Q1	Dual 4-A low-side drivers with enable	MSOP-8 PowerPAD, SOIC-8, PDIP-8
TPS2811-Q1	Dual 2-A low-side drivers with internal regulator	TSSOP-8, SOIC-8, PDIP-8
TPS2819-Q1	Single 2-A low-side driver with internal regulator	5-pin SOT-23
TPS2829-Q1	Single 2-A low-side driver	5-pin SOT-23

7 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



DGN Package
8-Pin MSOP with PowerPAD
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
AGND	4	GND	The AGND and the PGND must be connected by a single thick trace directly under the device. There must be a low ESR, low ESL capacitor of 0.1 µF between VDD (pin 1) and AGND. The power MOSFETs must be placed on the PGND side of the device while the control circuit must be on the AGND side of the device. The control circuit ground must be common with the AGND while the PGND must be common with the source of the power FETs.
ENBL	3	I	Enable input for the driver with logic-compatible threshold and hysteresis. The driver output can be enabled and disabled with this pin. It is internally pulled up to VDD with a pullup resistor for active-high operation. The output state when the device is disabled is low, regardless of the input state.
IN	2	I	Input signal of the driver, which has logic-compatible threshold and hysteresis. For UCC27321-Q1, IN is inverting, and for UCC37322-Q1, IN is noninverting.
OUT	6, 7	O	Driver outputs that must be connected together externally. The output stage is capable of providing 9-A peak drive current to the gate of a power MOSFET.
PGND	5	GND	Common ground for output stage. This ground must be connected very close to the source of the power MOSFET which the driver is driving. Grounds are separated to minimize ringing effects due to output switching di/dt, which can affect the input threshold. There must be a low ESR, low ESL capacitor of 0.1 µF between VDD (pin 8) and PGND.
VDD	1, 8	PWR	Supply voltage and the power input connections for this device. These pins must be connected together externally.
PowerPAD	Pad	GND	PowerPAD on DGN package only. The PowerPAD thermal pad is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate, which is the ground of the device.

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Supply voltage		–0.3	16	V
Output current	OUT		0.6	A
Input voltage	IN, ENBL	–5	6 or V_{DD} + 0.3	V
Power dissipation at T_A = 25°C	D package		650	mW
	DGN package		3	W
Operating junction temperature, T_J		–55	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND. Currents are positive into and negative out of the specified terminal.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	2000	V
		Charged-device model (CDM), per AEC Q100-011	1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage	VDD	4.5	15	V

8.4 Thermal Information

THERMAL METRIC(1)(2)(3)		UCC2732x-Q1	UCC27322-Q1	UNIT
		D (SOIC)	DGN (MSOP-PowerPAD)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	113	58.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.7	45.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	53.2	34.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	52.7	34	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	11.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) In general, the system designer must attempt to use larger traces on the PCB where possible to spread the heat away from the device more effectively. For information on the PowerPAD package, see *PowerPad™ Thermally Enhanced Package* and *PowerPad™ Made Easy*.
(3) The PowerPAD thermal pad is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate, which is the ground of the device.

8.5 Electrical Characteristics

V_{DD} = 4.5 V to 15 V, T_J = T_A = –40°C to 125°C (unless otherwise noted)

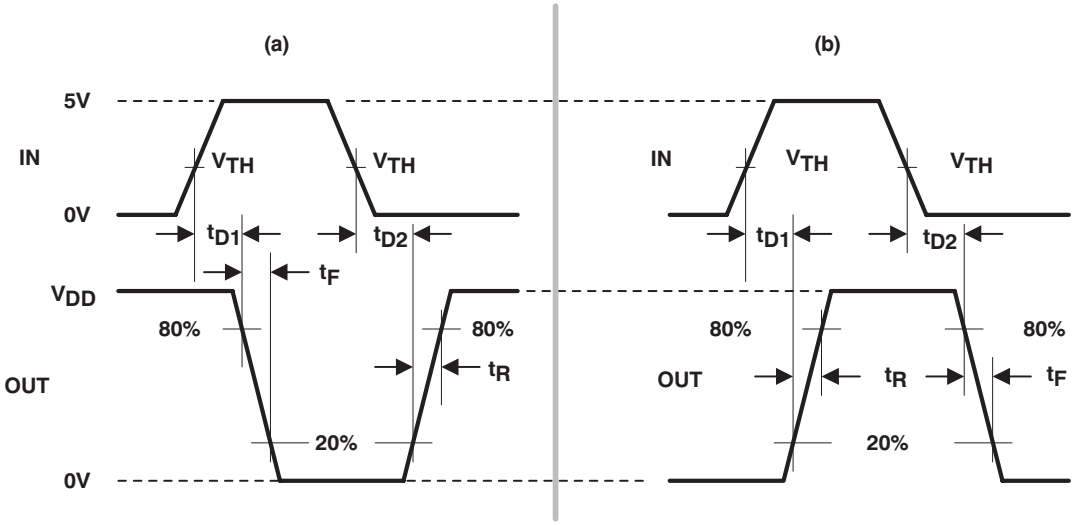
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DD}	Static operating current	UCC27321-Q1	IN = Low, ENBL = Low, V_{DD} = 15 V		150	225	µA
					440	650	
			IN = High, ENBL = Low, V_{DD} = 15 V		370	550	
					370	550	
		UCC27322-Q1	IN = Low, ENBL = High, V_{DD} = 15 V		150	225	
					450	650	
			IN = High, ENBL = High, V_{DD} = 15 V		75	125	
					675	1000	
INPUT (IN)							
V_{IH}	Logic 1 input threshold			2			V
V_{IL}	Logic 0 input threshold					1	V
	Input current	0 V ≤ V_{IN} ≤ V_{DD}		–10	0	10	µA
	Latch-up protection(1)			500			mA
OUTPUT (OUT)							
	Peak output current(1)(2)	V_{DD} = 14 V			9		A
V_{OH}	High-level output voltage	V_{OH} = V_{DD} – V_{OUT}, I_{OUT} = –10 mA			150	300	mV
V_{OL}	Low-level output voltage	I_{OUT} = 10 mA			11	25	mV
	Output resistance high(3)	I_{OUT} = –10 mA, V_{DD} = 14 V			15	25	Ω
	Output resistance low(3)	I_{OUT} = 10 mA, V_{DD} = 14 V			1.1	2.5	Ω
	Latch-up protection(1)			500			mA
ENABLE (ENBL)							
V_{EN_H}	Enable rising threshold voltage	Low-to-high transitions		1.5	2.2	2.7	V
V_{EN_L}	Enable falling threshold voltage	High-to-low transition		1.1	1.65	2	V
	Hysteresis			0.18	0.55	0.9	V
$R_{(ENBL)}$	Enable impedance	V_{DD} = 14 V, ENBL = Low		75	100	145	kΩ
t_{D3}	Propagation delay time	C_{LOAD} = 10 nF (see Figure 2)			60	95	ns
t_{D4}	Propagation delay time	C_{LOAD} = 10 nF (see Figure 2)			60	95	ns

(1) Specified by design
(2) The pullup and pulldown circuits of the driver are bipolar and MOSFET transistors in parallel. The pulsed output current rating is the combined current from the bipolar and MOSFET transistors.
(3) The pullup and pulldown circuits of the driver are bipolar and MOSFET transistors in parallel. The output resistance is the $R_{DS(ON)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

8.6 Switching Characteristics

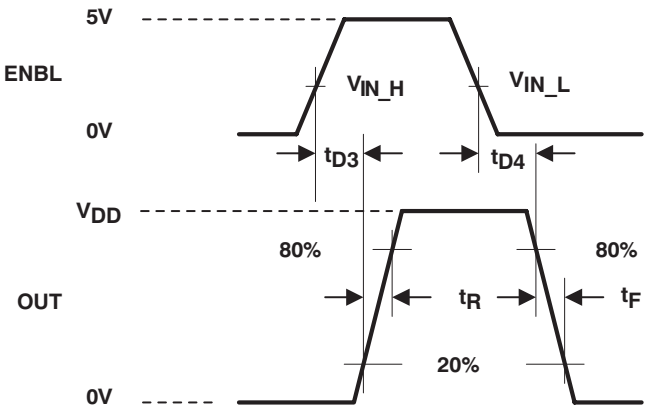
V_{DD} = 4.5 V to 15 V, T_J = T_A = –40°C to 125°C (unless otherwise noted) (see Figure 1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R	Rise time (OUT)	C_{LOAD} = 10 nF		20	75	ns
t_F	Fall time (OUT)	C_{LOAD} = 10 nF		20	35	ns
t_{D1}	Delay time, IN rising (IN to OUT)	C_{LOAD} = 10 nF		25	75	ns
t_{D2}	Delay time, IN falling (IN to OUT)	C_{LOAD} = 10 nF		35	75	ns



The 20% and 80% thresholds depict the dynamics of the bipolar output devices that dominate the power MOSFET transition through the Miller regions of operation.

Figure 1. Switching Waveforms for Inverting Driver (a) and Noninverting Driver (b)



The 20% and 80% thresholds depict the dynamics of the bipolar output devices that dominate the power MOSFET transition through the Miller regions of operation.

Figure 2. Switching Waveforms for Enable to Output

8.7 Typical Characteristics

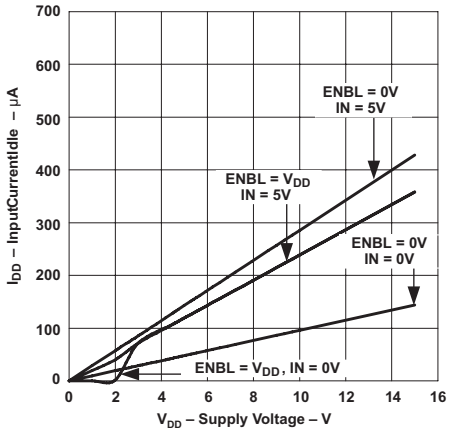


Figure 3. Input Current Idle vs Supply Voltage (UCC27321-Q1)

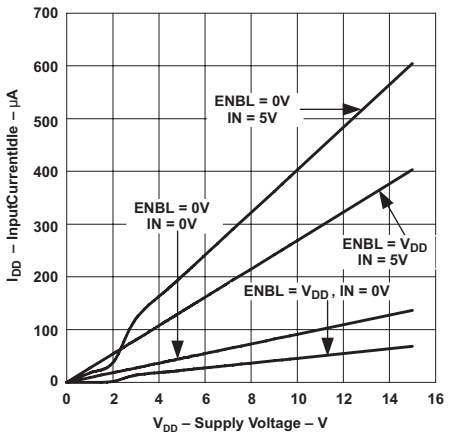


Figure 4. Input Current Idle vs Supply Voltage (UCC27322-Q1)

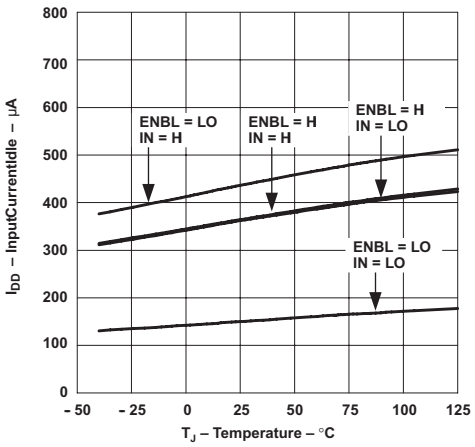


Figure 5. Input Current Idle vs Temperature (UCC27321-Q1)

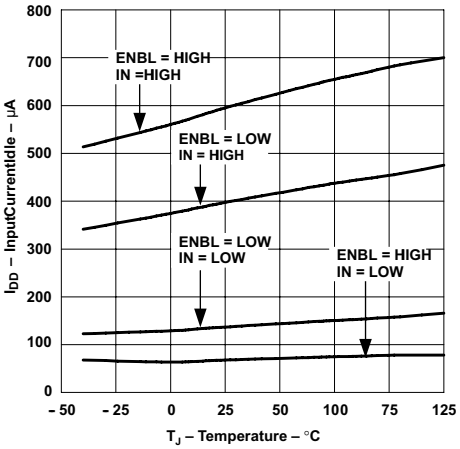


Figure 6. Input Current Idle vs Temperature (UCC27322-Q1)

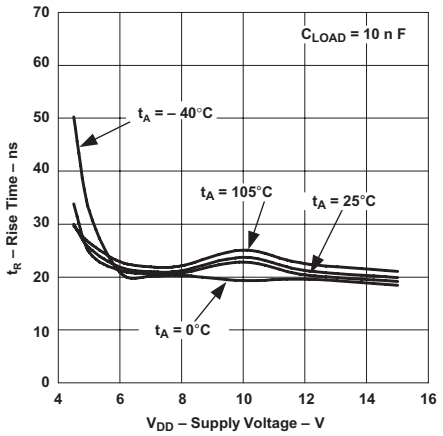


Figure 7. Rise Time vs Supply Voltage

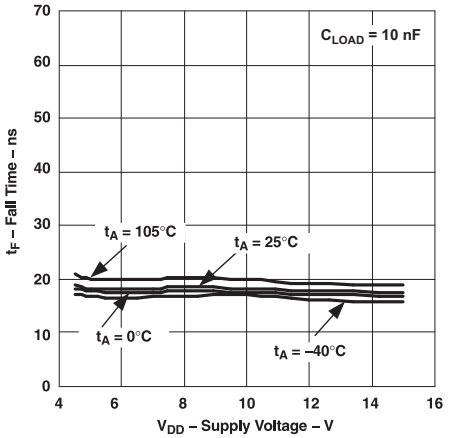


Figure 8. Fall Time vs Supply Voltage

Typical Characteristics (continued)

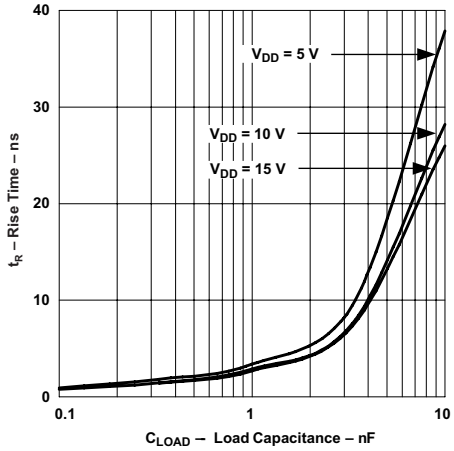


Figure 9. Rise Time vs Load Capacitance

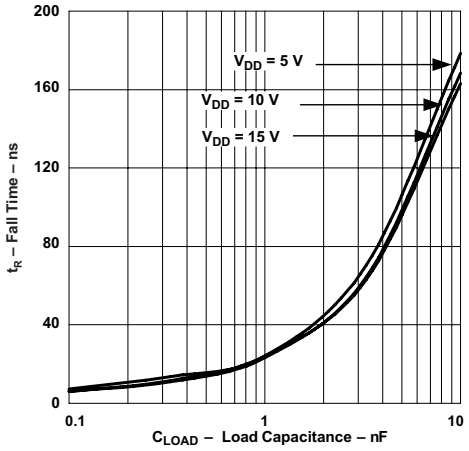


Figure 10. Fall Time vs Output Capacitance

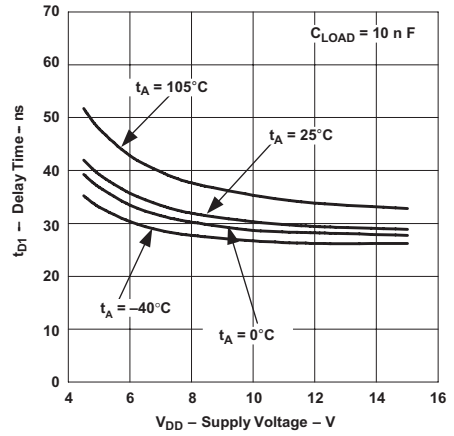


Figure 11. t_{D1} Delay Time vs Supply Voltage

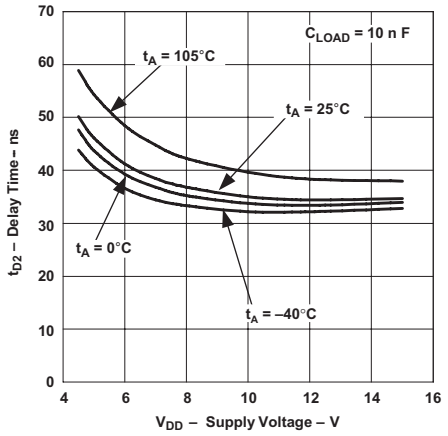


Figure 12. t_{D2} Delay Time vs Supply Voltage

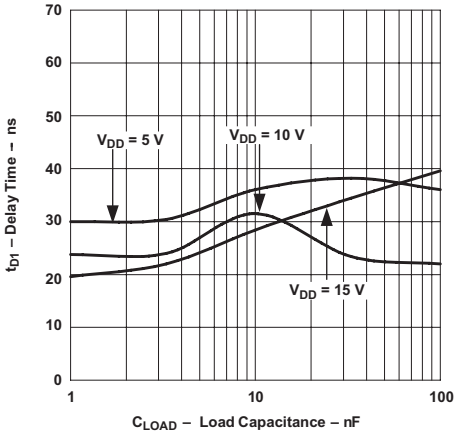


Figure 13. t_{D1} Delay Time vs Load Capacitance

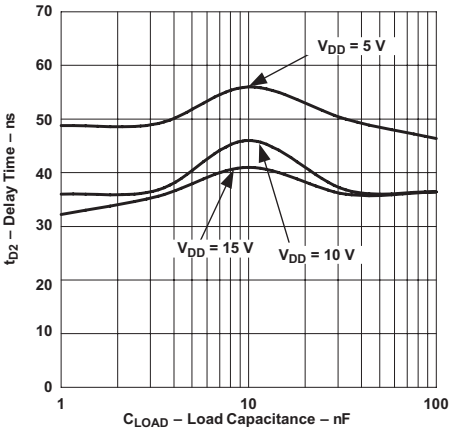


Figure 14. t_{D2} Delay Time vs Load Capacitance

Typical Characteristics (continued)

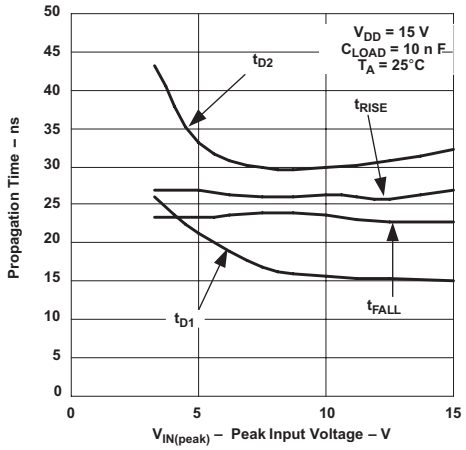


Figure 15. Propagation Times vs Peak Input Voltage

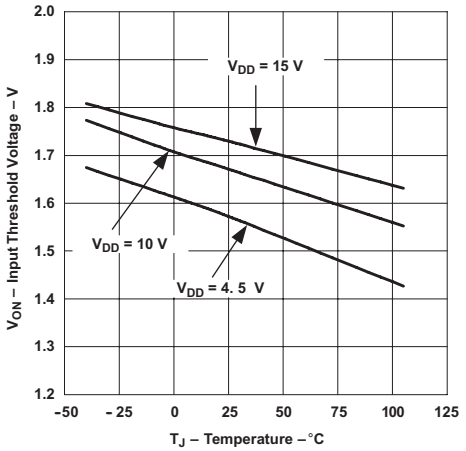


Figure 16. Input Threshold vs Temperature

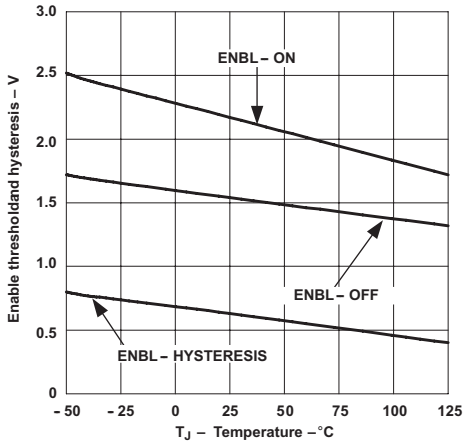


Figure 17. Enable Threshold and Hysteresis vs Temperature

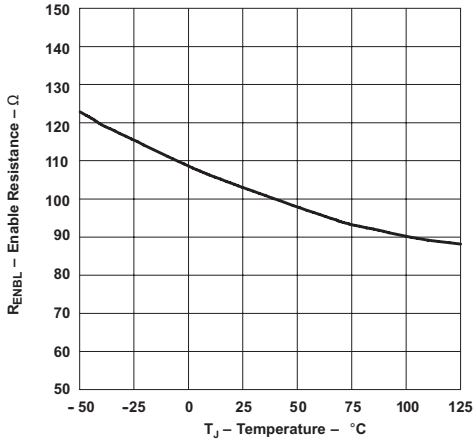


Figure 18. Enable Resistance vs Temperature

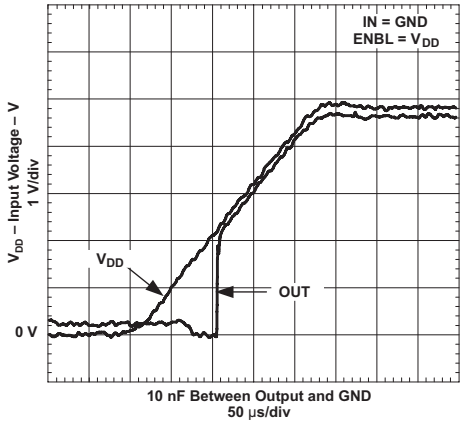


Figure 19. Output Behavior vs V_{DD} (UCC27321-Q1)

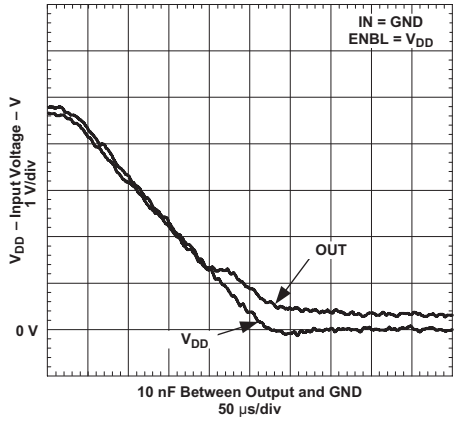


Figure 20. Output Behavior vs V_{DD} (UCC27321-Q1)

Typical Characteristics (continued)

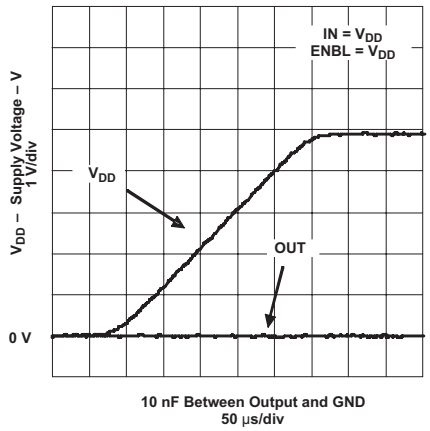


Figure 21. Output Behavior vs V_{DD} (Inverting)

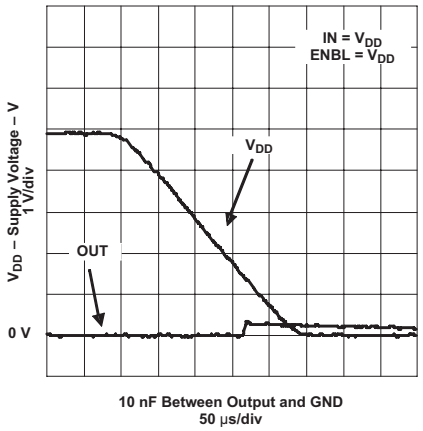


Figure 22. Output Behavior vs V_{DD} (Inverting)

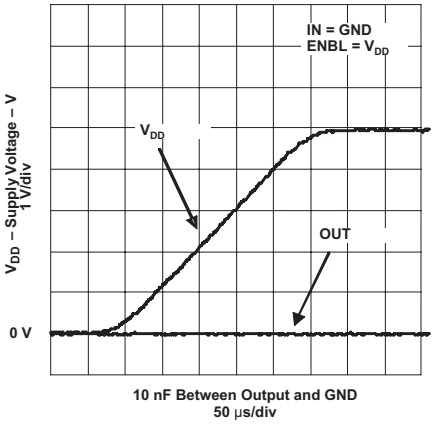


Figure 23. Output Behavior vs V_{DD} (Noninverting)

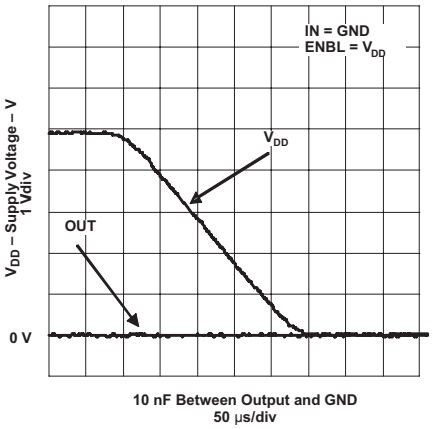


Figure 24. Output Behavior vs V_{DD} (Noninverting)

9 Detailed Description

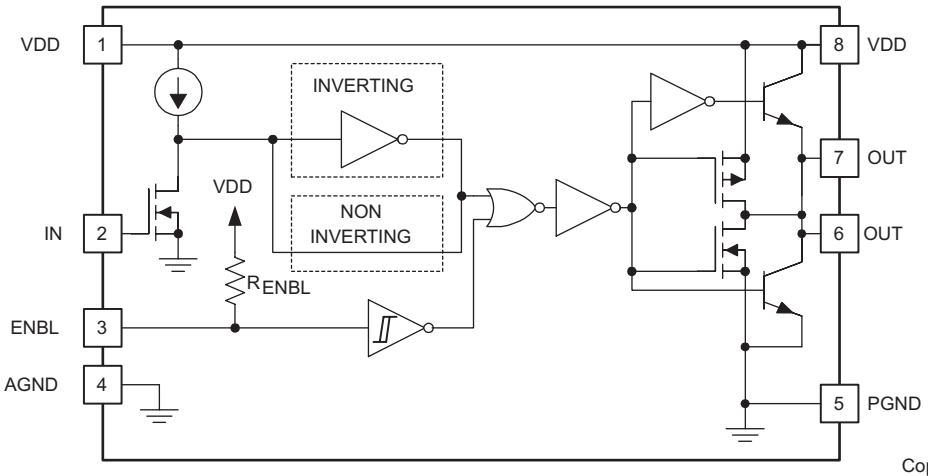
9.1 Overview

The UCC27321-Q1 and UCC27322-Q1 drivers serve as an interface between low-power controllers (discrete controllers, DSPs, MCUs, or microprocessors) and power MOSFETs. High-frequency power supplies often require high-speed, high-current drivers such as the UCC2732x-Q1 family. A leading application provides a high-power buffer stage between the PWM output of the control device and the gates of the primary power MOSFET or IGBT switching devices. In other cases, the device drives the power device gates through a drive transformer. Synchronous rectification supplies also have the need to drive multiple devices simultaneously, which can present an extremely large load to the control circuitry.

The inverting driver (UCC27321-Q1) is useful for generating inverted gate-drive signals from controllers that have outputs of the opposite polarity. For example, this driver can provide a gate signal for ground-referenced, N-channel synchronous rectifier MOSFETs in buck derived converters. This driver can also be used for generating a gate-drive signal for a P-channel MOSFET from a controller that is designed for N-channel applications.

MOSFET gate drivers are generally used when it is not feasible to have the primary PWM regulator device directly drive the switching devices for one or more reasons. The PWM device may not have the brute drive capability required for the intended switching MOSFET, limiting the switching performance in the application. In other cases, there may be a desire to minimize the effect of high-frequency switching noise by placing the high-current driver physically close to the load. Also, newer devices that target the highest operating frequencies may not incorporate onboard gate drivers at all. Their PWM outputs are only intended to drive the high-impedance input to a driver such as the UCC2732x-Q1. Finally, the control device may be under thermal stress due to power dissipation and an external driver can help by moving the heat from the controller to an external package.

9.2 Functional Block Diagram



INPUT/OUTPUT TABLE

	ENBL	IN	OUT
INVERTING UCC27321-Q1	0	0	0
	0	1	0
	1	0	1
	1	1	0
NON INVERTING UCC27322-Q1	0	0	0
	0	1	0
	1	0	0
	1	1	1

9.3 Feature Description

9.3.1 Input Stage

The IN threshold has a 3.3-V logic sensitivity over the full range of VDD voltage; yet, it is equally compatible with 0-V to V_{DD} signals. The inputs of UCC2732x-Q1 family of drivers are designed to withstand 500-mA reverse current without either damage to the device or logic upset. In addition, the input threshold turnoff of the UCC2732x-Q1 is slightly raised for improved noise immunity. The input stage of each driver must be driven by a signal with a short rise or fall time. This condition is satisfied in typical power-supply applications, where the input signals are provided by a PWM controller or logic gates with fast transition times (<200 ns). The IN input of the driver functions as a digital gate, and is not intended for applications where a slow-changing input voltage is used to generate a switching output when the logic threshold of the input section is reached. While this may not be harmful to the driver, the output of the driver may switch repeatedly at a high frequency.

Feature Description (continued)

Users must not attempt to shape the input signals to the driver in an attempt to slow down (or delay) the signal at the output. If limiting the rise or fall times to the power device is desired, then an external resistance can be added between the output of the driver and the load device, which is generally a power MOSFET gate. The external resistor may also help dissipate power from the device package, as discussed in *Thermal Considerations*.

9.3.2 Output Stage

The TrueDrive output stage is capable of supplying ±9-A peak current pulses and swings to both VDD and GND and can encourage even the most stubborn MOSFETs to switch. The pullup and pulldown circuits of the driver are constructed of bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $R_{DS(ON)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor. Each output stage also provides a very low impedance to overshoot and undershoot due to the body diode of the internal MOSFET. This means that in many cases, external Schottky clamping diodes are not required.

This unique bipolar and MOSFET hybrid output architecture (TrueDrive) allows efficient current sourcing at low supply voltages. The UCC2732x-Q1 family delivers 9 A of gate drive where it is most needed during the MOSFET switching transition—at the Miller plateau region—providing improved efficiency gains.

9.3.3 Source and Sink Capabilities During Miller Plateau

Large power MOSFETs present a large load to the control circuitry. Proper drive is required for efficient, reliable operation. The UCC2732x-Q1 drivers have been optimized to provide maximum drive to a power MOSFET during the Miller plateau region of the switching transition. This interval occurs while the drain voltage is swinging between the voltage levels dictated by the power topology, requiring the charging or discharging of the drain-gate capacitance with current supplied or removed by the driver.

Two circuits are used to test the current capabilities of the UCC2732x-Q1 driver. In each case, external circuitry is added to clamp the output near 5 V while the device is sinking or sourcing current. An input pulse of 250 ns is applied at a frequency of 1 kHz in the proper polarity for the respective test. In each test, there is a transient period when the current peaked up and then settled down to a steady-state value. The noted current measurements are made at a time of 200 ns after the input pulse is applied, after the initial transient.

The circuit in Figure 25 is used to verify the current-sink capability when the output of the driver is clamped at approximately 5 V, a typical value of gate-source voltage during the Miller plateau region. The UCC2732x-Q1 is found to sink 9 A at V_{DD} = 15 V.

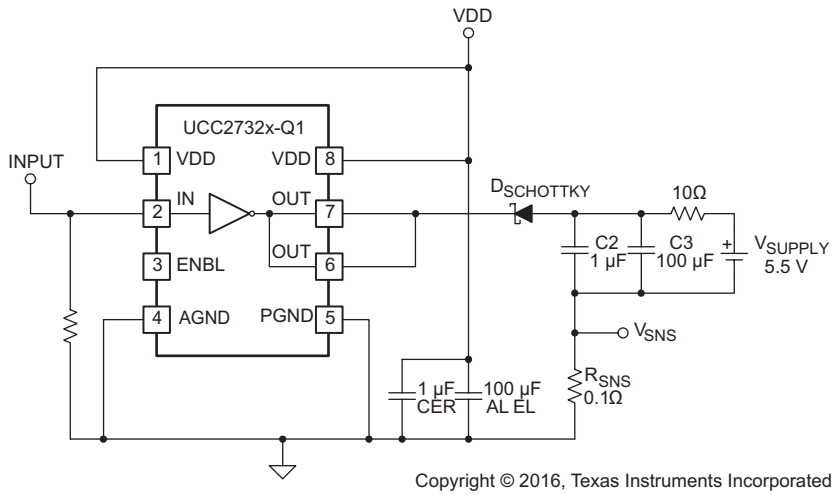


Figure 25. Sink Current Test Circuit

Feature Description (continued)

The circuit in Figure 26 is used to test the current-source capability with the output clamped to approximately 5 V with a string of Zener diodes. The UCC2732x-Q1 is found to source 9 A at V_{DD} = 15 V.

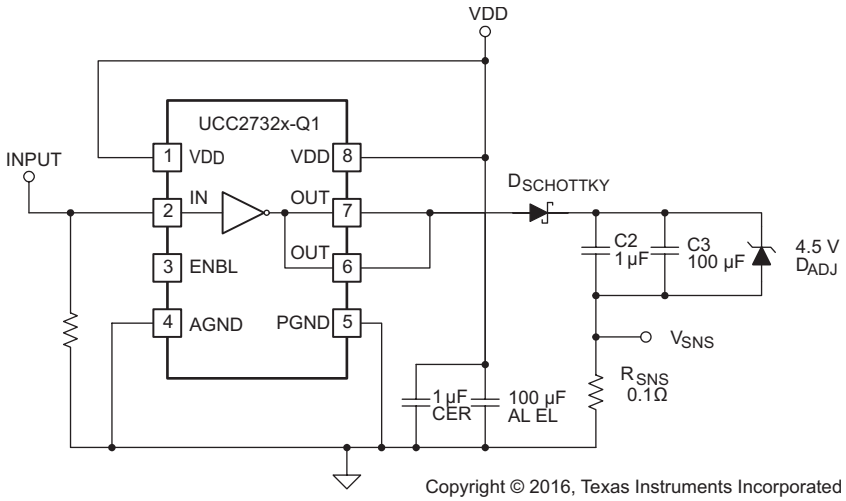


Figure 26. Source Current Test Circuit

The current-sink capability is slightly stronger than the current source capability at lower V_{DD}. This is due to the differences in the structure of the bipolar-MOSFET power output section, where the current source is a P-channel MOSFET and the current sink has an N-channel MOSFET.

In a large majority of applications, it is advantageous that the turnoff capability of a driver is stronger than the turnon capability. This helps to ensure that the MOSFET is held off during common power-supply transients that may turn the device back on.

9.3.4 VDD

Although quiescent VDD current is very low, total supply current is higher, depending on the OUT current and the programmed oscillator frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Q_g), average OUT current can be calculated from Equation 1:

$$I_{OUT} = Q_g \times f \quad (1)$$

where

- f = frequency

For the best high-speed circuit performance, TI recommends two VDD bypass capacitors to prevent noise problems. TI highly recommends the use of surface-mount components. A 0.1-µF ceramic capacitor must be placed closest to the VDD-to-ground connection. In addition, a larger capacitor (such as 1-µF) with relatively low ESR must be connected in parallel, to help deliver the high-current peaks to the load. The parallel combination of capacitors must present a low-impedance characteristic for the expected current levels in the driver application.

9.3.5 Drive Current and Power Requirements

The UCC2732x-Q1 family of drivers is capable of delivering 9 A of current to a MOSFET gate for a period of several hundred nanoseconds. High peak current is required to turn an N-channel device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground. This repeats at the operating frequency of the power device. An N-channel MOSFET is used in this discussion because it is the most common type of switching device used in high-frequency power-conversion equipment.

Feature Description (continued)

Design And Application Guide For High Speed MOSFET Gate Drive Circuits and *Practical Considerations in High Performance MOSFET, IGBT and MCT Gate Drive Circuits* contain detailed discussions of the drive current required to drive a power MOSFET and other capacitive-input switching devices. Much information is provided in tabular form to give a range of the current required for various devices at various frequencies. The information pertinent to calculating gate-drive current requirements is summarized here. See MOSFET and IGBT drivers for additional documentation.

When a driver is tested with a discrete capacitive load, it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by Equation 2:

$$E = ½CV^2$$

where

- C = load capacitor
- V = bias voltage feeding the driver (2)

There is an equal amount of energy transferred to ground when the capacitor is discharged. This leads to a power loss given by Equation 3:

$$P = 2 \times ½CV^2f$$

where

- f = switching frequency (3)

This power is dissipated in the resistive elements of the circuit. Thus, with no external resistor between the driver and gate, this power is dissipated inside the driver. Half of the total power is dissipated when the capacitor is charged, and the other half is dissipated when the capacitor is discharged. An actual example using the conditions of the previous gate-drive waveform must help clarify this.

With V_{DD} = 12 V, C_{LOAD} = 10 nF, and f = 300 kHz, the power loss can be calculated as in Equation 4:

$$P = 10\ nF \times (12\ V)^2 \times (300\ kHz) = 0.432\ W \quad (4)$$

With a 12-V supply, in Equation 5 this equates to a current of:

$$I = P / V = 0.432\ W / 12\ V = 0.036\ A \quad (5)$$

The switching load presented by a power MOSFET can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge required to swing the drain of the device between the on and off states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, the power that must be dissipated when charging a capacitor can be determined. This is done by using the equivalence Q_g = CeffV to provide the Equation 6 for power:

$$P = C \times V^2 \times f = Q_g \times V \times f \quad (6)$$

Equation 6 allows a power designer to calculate the bias power required to drive a specific MOSFET gate at a specific bias voltage.

9.3.6 Enable

UCC2732x-Q1 provides an enable input for improved control of the driver operation. This input also incorporates logic-compatible thresholds with hysteresis. The input is internally pulled up to V_{DD} with a 100-kΩ (typical) resistor for active-high operation. When ENBL is high, the device is enabled, and when ENBL is low, the device is disabled. The default state of the ENBL pin is to enable the device, and therefore can be left open for standard operation. The output state when the device is disabled is low, regardless of the input state. See the truth table (Table 2) for operation using enable logic.

The ENBL input is compatible with both logic signals and slow-changing analog signals. It can be directly driven, or a power-up delay can be programmed with a capacitor between ENBL and AGND.

9.4 Device Functional Modes

The UCC2732x-Q1 device has two functional modes; enabled when ENBL is HIGH and disabled when ENBL is LOW. Table 2 lists the logic of this device.

Table 2. Device Logic and Modes Table

	ENBL	IN	OUT
Inverting UCC27321-Q1	0	0	0
	0	1	0
	1	0	1
	1	1	0
Noninverting UCC27322-Q1	0	0	0
	0	1	0
	1	0	0
	1	1	1

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

High-current gate driver devices are required in switching power applications for a variety of reasons. To enable fast switching of power devices and reduce associated power losses, a powerful gate driver can be employed between the PWM output of controllers or signal isolation devices and the gates of the power semiconductor devices. Further, gate drivers are indispensable when sometimes it is just not feasible to have the PWM controller directly drive the gates of the switching devices. The situation may be encountered because the PWM signal from a digital controller or signal isolation device is often a 3.3-V or 5-V logic signal which is not capable of effectively turning on a power switch. A level-shifting circuitry is required to boost the logic-level signal to the gate-drive voltage to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on bipolar or MOSFET transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate for this because they lack level-shifting capability and low-drive voltage protection. Gate drivers effectively combine both the level-shifting and buffer drive functions. Gate drivers may also minimize the effect of switching noise by placing the high-current driver physically close to the power switch, drive gate-driver transformers and control floating power device gates, reducing power dissipation and thermal stress in controllers by absorbing gate-charge power losses.

In summary gate drivers are extremely important components in switching power combining benefits of high-performance, low-cost, low component count, board-space reduction, and simplified system design.

10.2 Typical Application

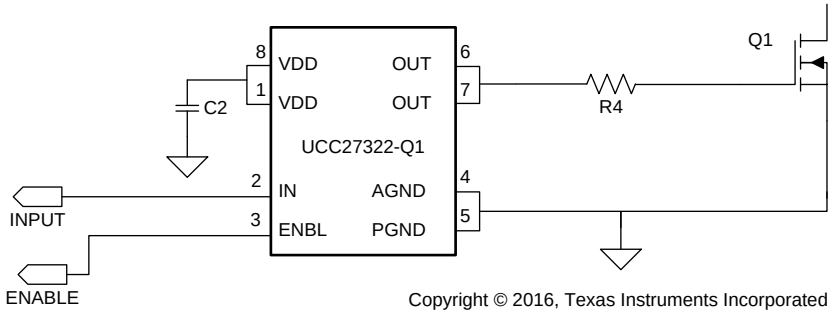


Figure 27. Typical Application Diagram of UCC27322-Q1

Typical Application (continued)

10.2.1 Design Requirements

When selecting the proper gate driver device for an end application, some design considerations must be evaluated first to make the most appropriate selection. The following design parameters should be used when selecting the proper gate driver device for an end application: input-to-output configuration, the input threshold type, bias supply voltage levels, peak source and sink currents, availability of independent enable and disable functions, propagation delay, power dissipation, and package type. See the example design parameters and requirements in Table 3.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input-to-output configuration	Noninverting
Input threshold type	CMOS
Bias supply voltage levels	12 V
dVDS/dt(1)	20 V/ns
Enable function	Yes
Propagation delay	<50 ns
Power dissipation	<0.45 W
Package type	SOIC (8)

(1) dVDS/dt is a typical requirement for a given design. This value can be used to find the peak source and sink currents required as shown in *Peak Source and Sink Currents*.

10.2.2 Detailed Design Procedure

10.2.2.1 Input-to-Output Configuration

The design must specify which type of input-to-out configuration is used. If turning on the power MOSFET or IGBT when the input signal is in high state is preferred, then a device capable of the noninverting configuration must be selected. If turning off the power MOSFET or IGBT when the input signal is in high state is preferred, then a device capable of the inverting configuration must be chosen. Based on this noninverting requirement of this application, the proper device is the UCC27322-Q1.

10.2.2.2 Input Threshold Type

The type of input voltage threshold determines the type of controller that can be used with the gate driver device. The UCC2732x-Q1 devices feature a TTL and CMOS-compatible input threshold logic, with wide hysteresis. The threshold voltage levels are low voltage and independent of the VDD supply voltage, which allows compatibility with both logic-level input signals from microcontrollers as well as higher-voltage input signals from analog controllers. See *Electrical Characteristics* for the actual input threshold voltage levels and hysteresis specifications for the UCC2732x-Q1 devices.

10.2.2.3 VDD Bias Supply Voltage

The bias supply voltage to be applied to the VDD pins of the device must never exceed the values listed in *Recommended Operating Conditions*. However, different power switches require different voltage levels to be applied at the gate. With a wide operating range from 4.5 V to 15 V, the UCC2732x-Q1 device can be used to drive a variety of power switches, such as Si MOSFETs (V_{GS} = 4.5 V, 10 V, 12 V), IGBTs (V_{GE} = 15 V), and wide-bandgap power semiconductors (such as GaN, certain types of which allow no higher than 6 V to be applied to the gate terminals).

10.2.2.4 Peak Source and Sink Currents

Generally, the switching speed of the power switch during turnon and turnoff must be as fast as possible to minimize switching power losses. The gate driver device must be able to provide the required peak current for achieving the targeted switching speeds for the targeted power MOSFET.

Using the example of a power MOSFET, the system requirement for the switching speed is typically described in terms of the slew rate of the drain-to-source voltage of the power MOSFET (such as dvds/dt). For example, the system requirement might state that a SPP20N60C3 power MOSFET must be turned on with a dvds/dt of 20 V/ns or higher under a DC bus voltage of 400 V in a continuous-conduction-mode (CCM) boost PFC-converter application. This type of application is an inductive hard-switching application and reducing switching power loss is critical. This requirement means that the entire drain-to-source voltage swing during power MOSFET turnon event (from 400 V in the OFF state to $V_{DS(ON)}$ in ON state) must be completed in approximately 20 ns or less. When the drain-to-source voltage swing occurs, the Miller charge of the power MOSFET (Q_{gd} for SPP20N60C3 power MOSFET is 33 nC, typically) is supplied by the peak current of gate driver. According to power MOSFET inductive switching mechanism, the gate-to-source voltage of the power MOSFET at this time is the Miller plateau voltage, which is typically a few volts higher than the threshold voltage of the power MOSFET ($V_{GS(th)}$).

To achieve the targeted dvds/dt, the gate driver must be capable of providing the Q_{gd} charge in 20 ns or less. In other words, a peak current of 1.65 A = (33 nC) / (20 ns) or higher must be provided by the gate driver. The UCC2732x-Q1 devices can provide 9-A peak sourcing or sinking current which clearly exceeds the design requirement and has the capability to meet the switching speed required. This 9-A peak sourcing or sinking current provides an extra margin against part-to-part variations in the Q_{gd} parameter of the power MOSFET along with additional flexibility to insert external gate resistors and fine tune the switching speed for efficiency versus EMI optimizations.

In practical designs, the parasitic trace in the gate driver circuit of the PCB has a definitive role to play on the power MOSFET switching speed. The effort of this trace inductance is to limit the di/dt of the output current pulse of the gate driver. To illustrate this effect, consider output current pulse waveform from the gate driver to be approximated to a triangular profile, where the area under the triangle (0.5 × IPEAK × time) would equal the total gate charge of the power MOSFET (Q_g for SPP20N60C3 power MOSFET is 87 nC typically). If the parasitic trace inductance limits the di/dt then a situation may occur in which the full peak current capability of the gate driver is not fully achieved in the time required to deliver the Q_g required for the power MOSFET switching. In other words, the time parameter in the equation would dominate and the IPEAK value of the current pulse would be much less than the true peak current capability of the device, while the required Q_g is still delivered. Because of this, the desired switching speed may not be realized, even when theoretical calculations indicate the gate driver can achieve the targeted witching speed. Thus, placing the gate driver device very close to the power MOSFET and designing a tight gate drive-loop with minimal PCB trace inductance is important to realize the full peak-current capability of the gate driver.

10.2.2.5 Enable and Disable Function

Certain applications demand independent control of the output state of the driver without involving the input signal. A pin which offers enable and disable functions achieves the requirements. For these applications, the UCC2732x-Q1 devices are suitable as they feature an input pin and an Enable pin.

10.2.2.6 Propagation Delay

The acceptable propagation delay from the gate driver is dependent on the switching frequency at which it is used and the acceptable level of pulse distortion to the system. The UCC2732x-Q1 devices feature 25-ns turnon propagation delay and 35-ns turnoff propagation delay (typical), which ensure very little distortion and allow operation at higher frequencies. See *Electrical Characteristics* for the propagation and *Switching Characteristics* of the UCC2732x-Q1 devices.

10.2.3 Application Curves

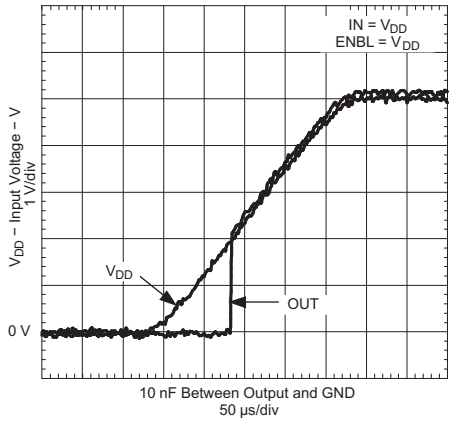


Figure 28. Output Behavior vs V_{DD} (UCC27322-Q1)

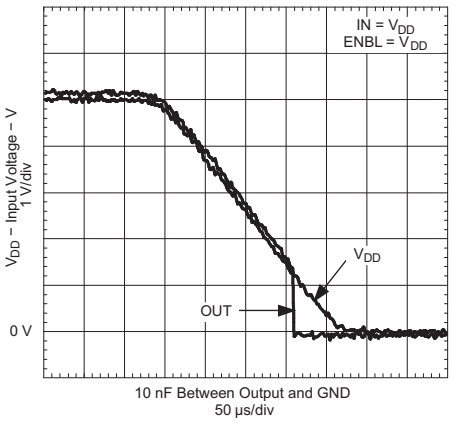


Figure 29. Output Behavior vs V_{DD} (UCC27322-Q1)

11 Power Supply Recommendations

Although quiescent VDD current is very low, total supply current is higher, depending on OUTA and OUTB current and the operating frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Q_g), average OUT current can be calculated using Equation 7.

$$I_{OUT} = Q_g \times f \quad (7)$$

For the best high-speed circuit performance, TI recommends two VDD bypass capacitors to prevent noise problems. TI also highly recommends using surface mount components. A 0.1-µF ceramic capacitor must be placed closest to the VDD to ground connection. In addition, a larger capacitor (such as 1 µF) with relatively low ESR must be connected in parallel to help deliver the high current peaks to the load. The parallel combination of capacitors presents a low impedance characteristic for the expected current levels in the driver application.

12 Layout

12.1 Layout Guidelines

It can be a significant challenge to avoid the overshoot or undershoot and ringing issues that can arise from circuit layout. The low impedance of these drivers and their high di/dt can induce ringing between parasitic inductances and capacitances in the circuit. Take utmost care in the circuit layout.

In general, position the driver physically as close to its load as possible. Place a 1-µF bypass capacitor as close to the output side of the driver as possible, connecting it to pins 1 and 8. Connect a single trace between the two VDD pins (pin 1 and pin 8); connect a single trace between PGND and AGND (pin 5 and pin 4). If a ground plane is used, it may be connected to AGND; do not extend the plane beneath the output side of the package (pins 5 to 8). Connect the load to both OUT pins (pins 7 and 6) with a single trace on the adjacent layer to the component layer; route the return current path for the output on the component side, directly over the output path.

Extreme conditions may require decoupling the input power and ground connections from the output power and ground connections. The UCCx732[1,2] has a feature that allows the user to take these extreme measures, if necessary. There is a small amount of internal impedance of about 15 Ω between the AGND and PGND pins; there is also a small amount of impedance (approximately 30 Ω) between the two VDD pins. To take advantage of this feature, connect a 1-µF bypass capacitor between VDD and PGND (pins 5 and 8) and connect a 0.1-µF bypass capacitor between VDD and AGND (pins 1 and 4). Further decoupling can be achieved by connecting between the two VDD pins with a jumper that passes through a 40-MHz ferrite bead and connects bias power only to pin 8 (VDD). Even more decoupling can be achieved by connecting between AGND and PGND with a pair of anti-parallel diodes (anode connected to cathode and cathode connected to anode).

12.2 Layout Example

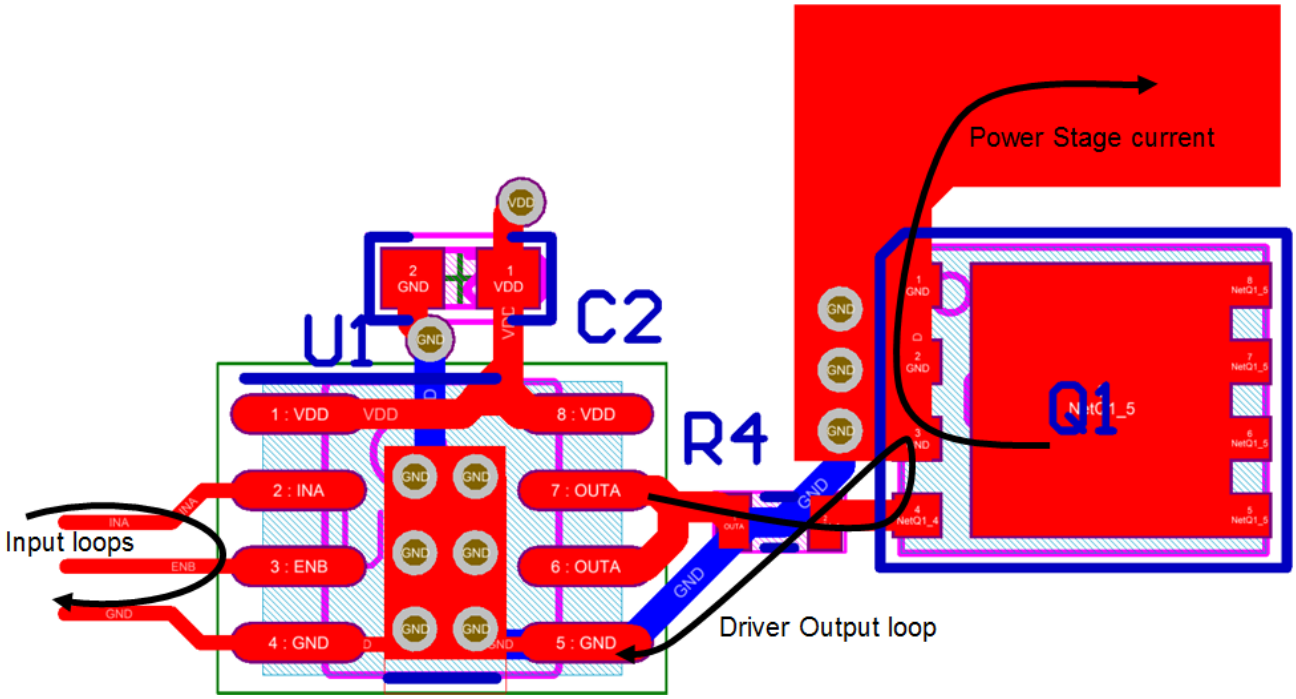


Figure 30. Layout Recommendation

12.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive-power requirements of the load and the thermal characteristics of the package. For a power driver to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The UCC2732x-Q1 family of drivers is available in two different packages to cover a range of application requirements.

The 8-pin SOIC (D) package has a power rating of approximately 0.5 W at T_A = 70°C. This limit is imposed in conjunction with the power derating factor also given in the table. The power dissipation in our earlier example is 0.432 W with a 10-nF load, 12-V V_{DD}, switched at 300 kHz. Thus, only one load of this size could be driven using the D package. The difficulties with heat removal limit the drive available in the older packages.

The 8-pin MSOP PowerPAD (DGN) significantly relieves this concern by offering an effective means of removing the heat from the semiconductor junction. As illustrated in *PowerPad Thermally Enhanced Package*, the PowerPAD packages offer a lead-frame die pad that is exposed at the base of the package. This pad is soldered to the copper on the PCB directly underneath the package, reducing the θ_{JC} to 4.7°C/W. Data is presented in *PowerPad Thermally Enhanced Package* to show that the power dissipation can be quadrupled in the PowerPAD package when compared to the standard packages. The PCB must be designed with thermal lands and thermal vias to complete the heat removal subsystem, as summarized in *PowerPAD Made Easy*. This allows a significant improvement in heatsink capability over that available in the D package and is shown to more than double the power capability of the D package.

NOTE

The PowerPAD thermal pad is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate, which is the ground of the device.

12.4 Power Dissipation

The UCC2732x-Q1 family of drivers are capable of delivering 9-A of current to a MOSFET gate for a period of several hundred nanoseconds. High peak current is required to turn an N-channel device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground. This repeats at the operating frequency of the power device. An N-channel MOSFET is used in this discussion because it is the most common type of switching device used in high-frequency power conversion equipment.

Design And Application Guide For High Speed MOSFET Gate Drive Circuits and *Practical Considerations in High Performance MOSFET, IGBT and MCT Gate Drive Circuits* contain detailed discussions of the drive current required to drive a power MOSFET and other capacitive-input switching devices. Much information is provided in tabular form to give a range of the current required for various devices at various frequencies. The information pertinent to calculating gate drive current requirements is summarized here.

When a driver device is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by Equation 8.

$$E = \frac{1}{2}CV^2$$

where

- C is the load capacitor
- V is the bias voltage feeding the driver (8)

There is an equal amount of energy transferred to ground when the capacitor is discharged. This leads to a power loss given by Equation 9.

$$P = 2 \times \frac{1}{2}CV^2f$$

where

- f is the switching frequency (9)

This power is dissipated in the resistive elements of the circuit. Thus, with no external resistor between the driver and gate, this power is dissipated inside the driver. Half of the total power is dissipated when the capacitor is charged, and the other half is dissipated when the capacitor is discharged. An example using the conditions of the previous gate-drive waveform helps to clarify this.

With V_{DD} = 12 V, C_{LOAD} = 10 nF, and f = 300 kHz, the power loss can be calculated as shown in Equation 11.

$$P = 10\ nF \times (12)^2 \times (300\ kHz) = 0.432\ W \quad (10)$$

With a 12-V supply, this would equate, as shown in Equation 11, to a current of:

$$I = \frac{P}{V} = \frac{0.432\ W}{12\ V} = 0.036A \quad (11)$$

The switching load presented by a power MOSFETcan be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge required to swing the drain of the device between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Qg, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence Qg = CeffV to provide Equation 12 for power.

$$P = C \times V^2 \times f = Qg \times V \times f \quad (12)$$

Equation 12 allows a power designer to calculate the bias power required to drive a specific MOSFET gate at a specific bias voltage.

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation, see the following:

- Power Supply Seminar SEM-1400 Topic 2: *Design And Application Guide For High Speed MOSFET Gate Drive Circuits* (SLUP133)
- *Practical Considerations in High Performance MOSFET, IGBT and MCT Gate Drive Circuits* (SLUA105)
- MOSFET and IGBT drivers
- *PowerPad Thermally Enhanced Package* (SLMA002)
- *PowerPAD Made Easy* (SLMA004)

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UCC27321-Q1	Click here	Click here	Click here	Click here	Click here
UCC27322-Q1	Click here	Click here	Click here	Click here	Click here

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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13.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27321QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27321Q	Samples
UCC27322QDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	EACQ	Samples
UCC27322QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27322Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UCC27321-Q1, UCC27322-Q1 :

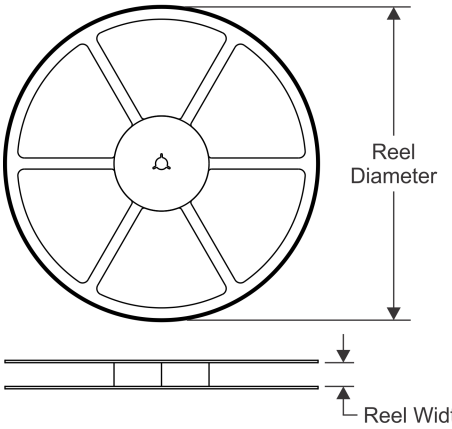
- Catalog: UCC27321, UCC27322
- Enhanced Product: UCC27322-EP

NOTE: Qualified Version Definitions:

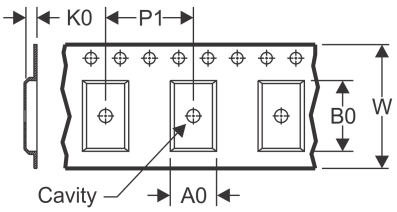
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

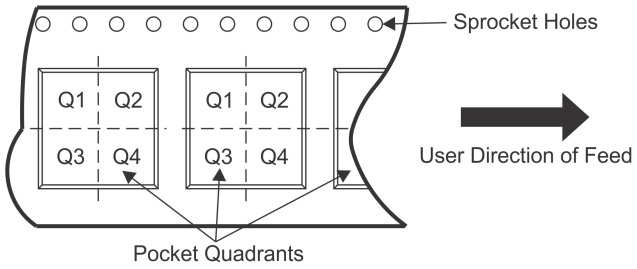


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

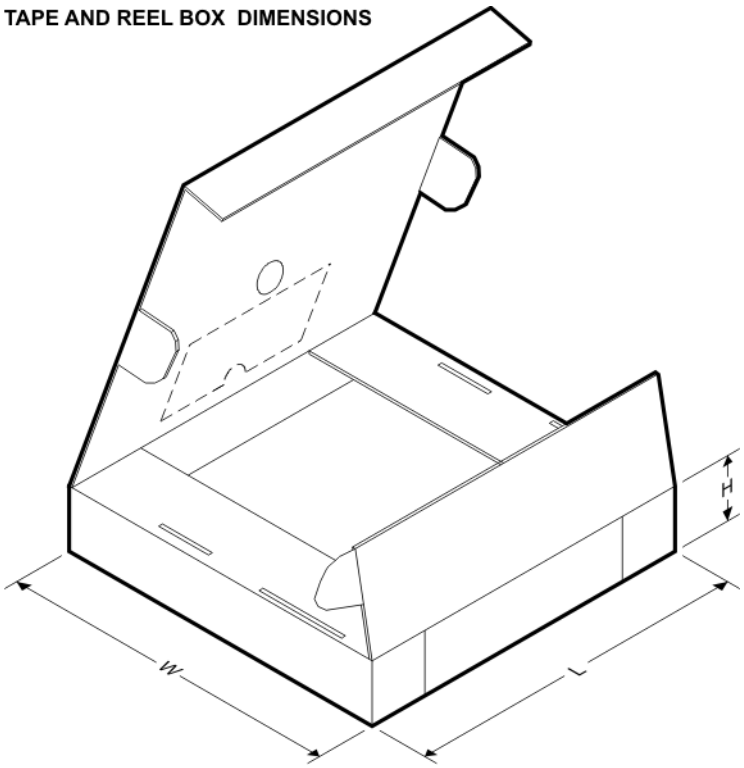
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

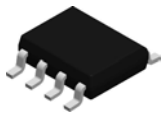
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27321QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27322QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27322QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27321QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
UCC27322QDGNRQ1	HVSSOP	DGN	8	2500	350.0	350.0	43.0
UCC27322QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0

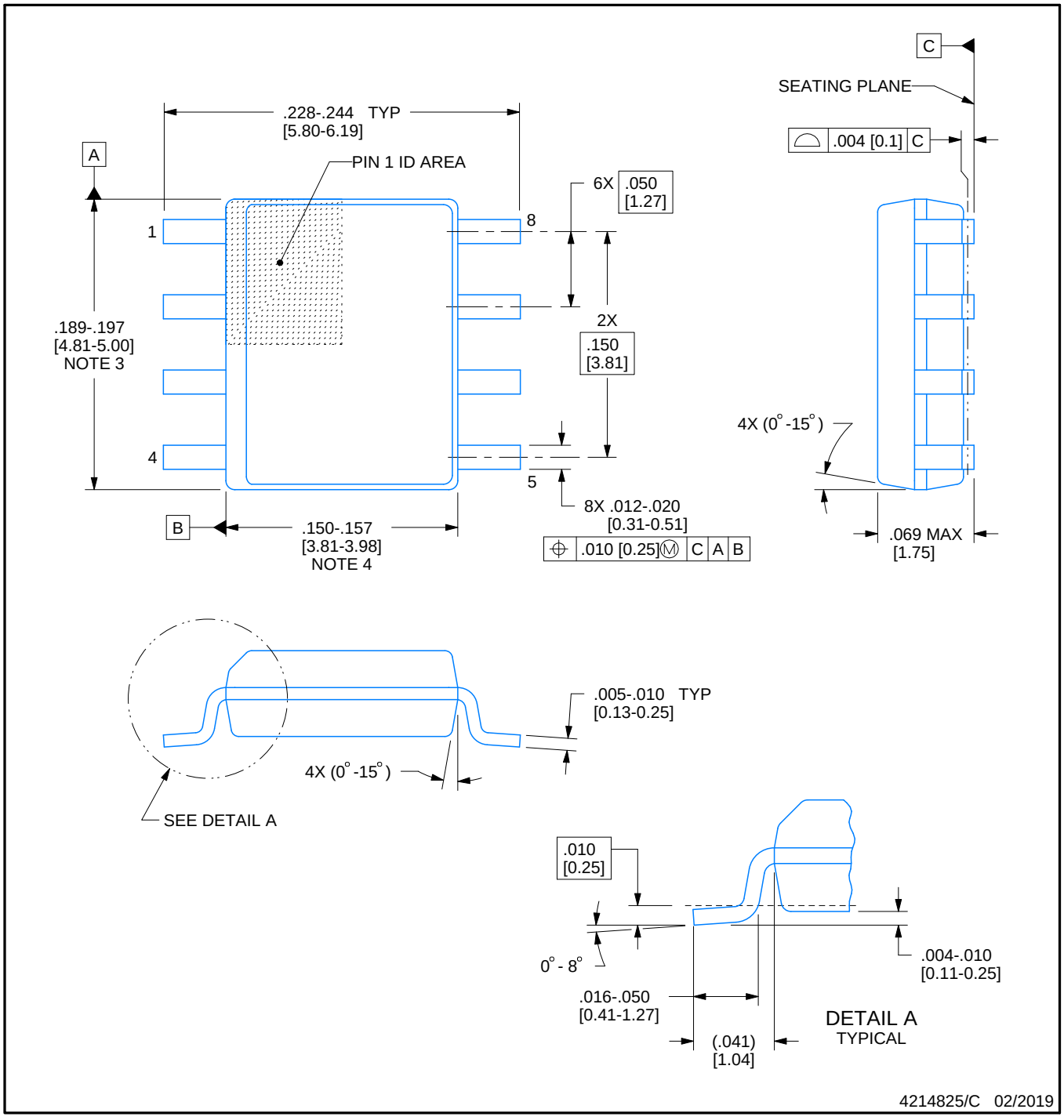


PACKAGE OUTLINE

D0008A

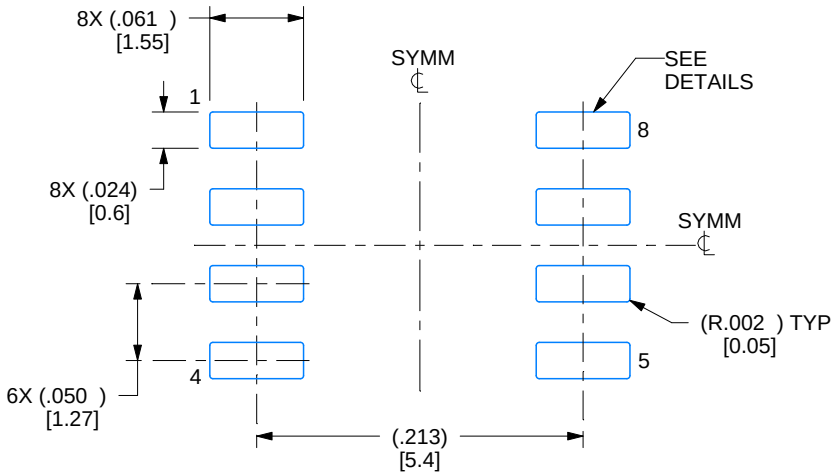
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

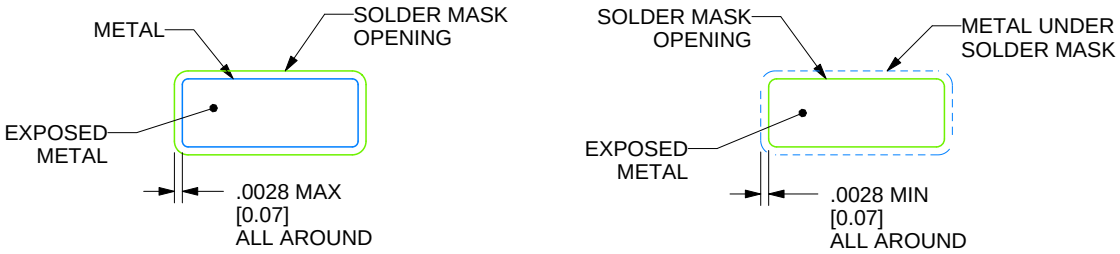


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

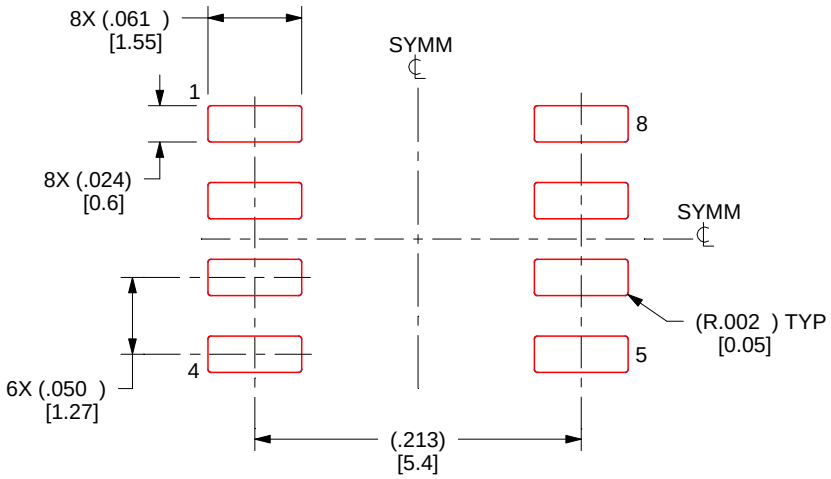
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



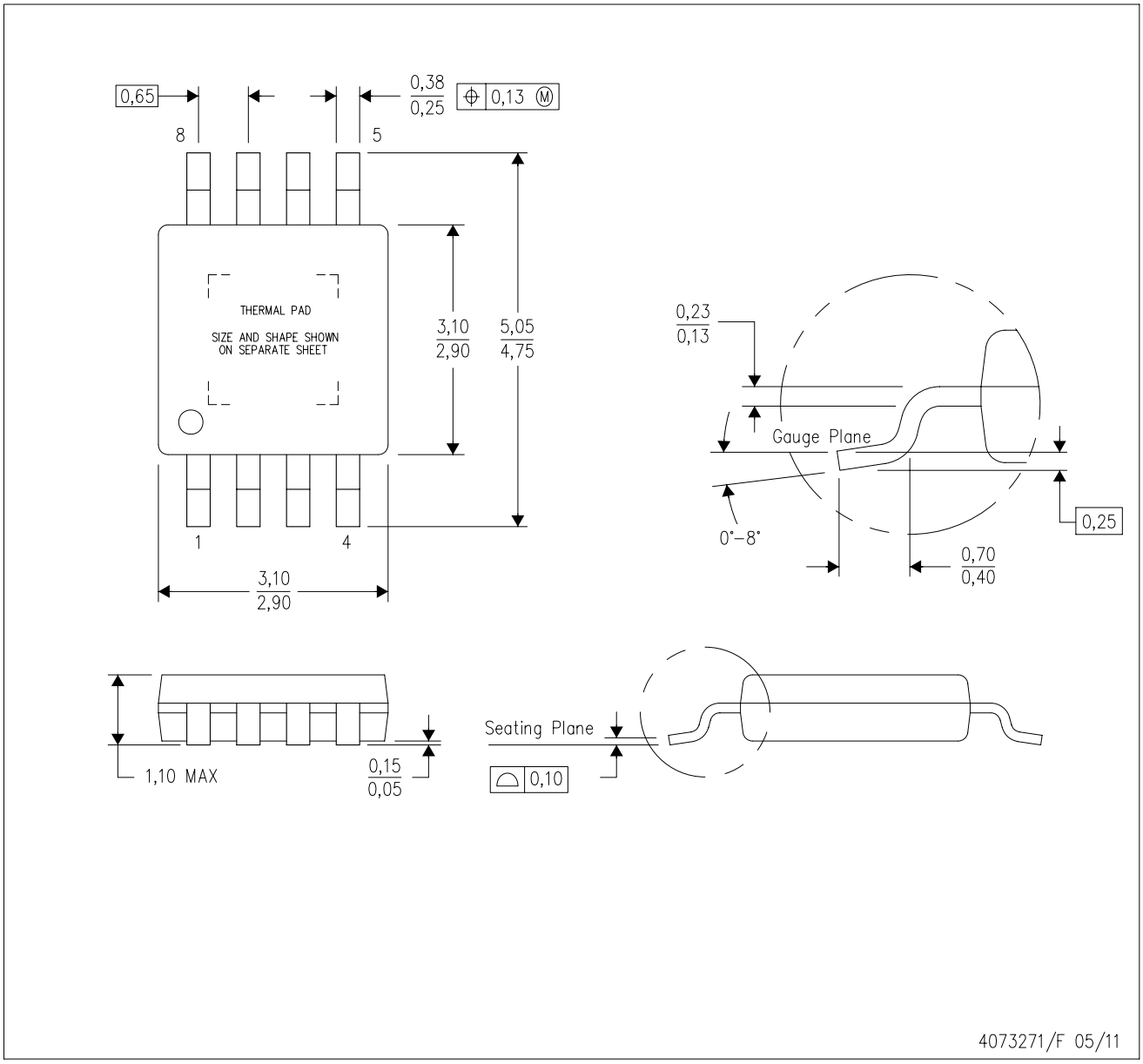
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

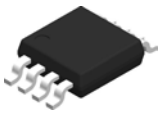


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

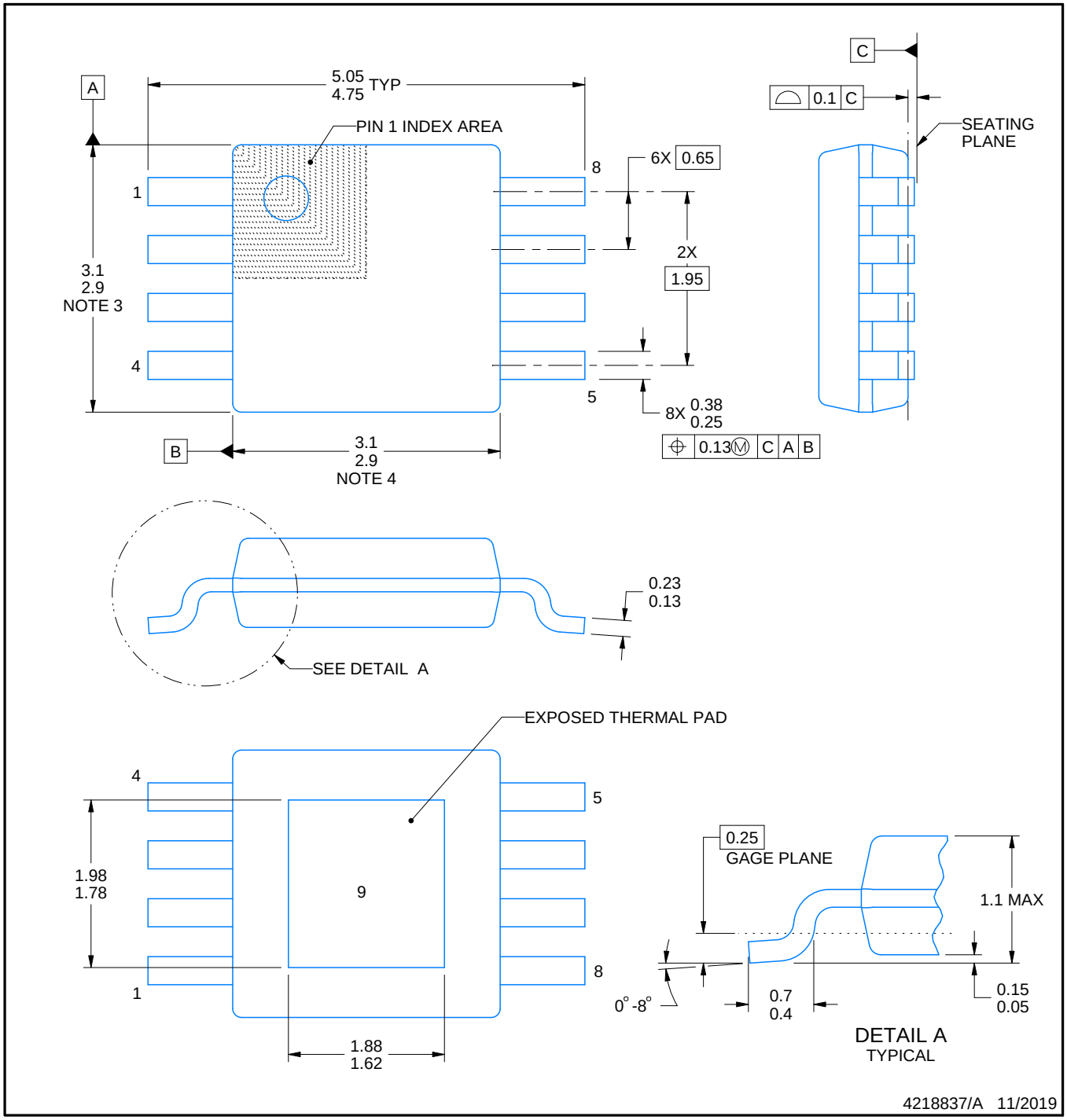
PACKAGE OUTLINE

DGN0008B



PowerPAD™ VSSOP - 1.1 mm max height

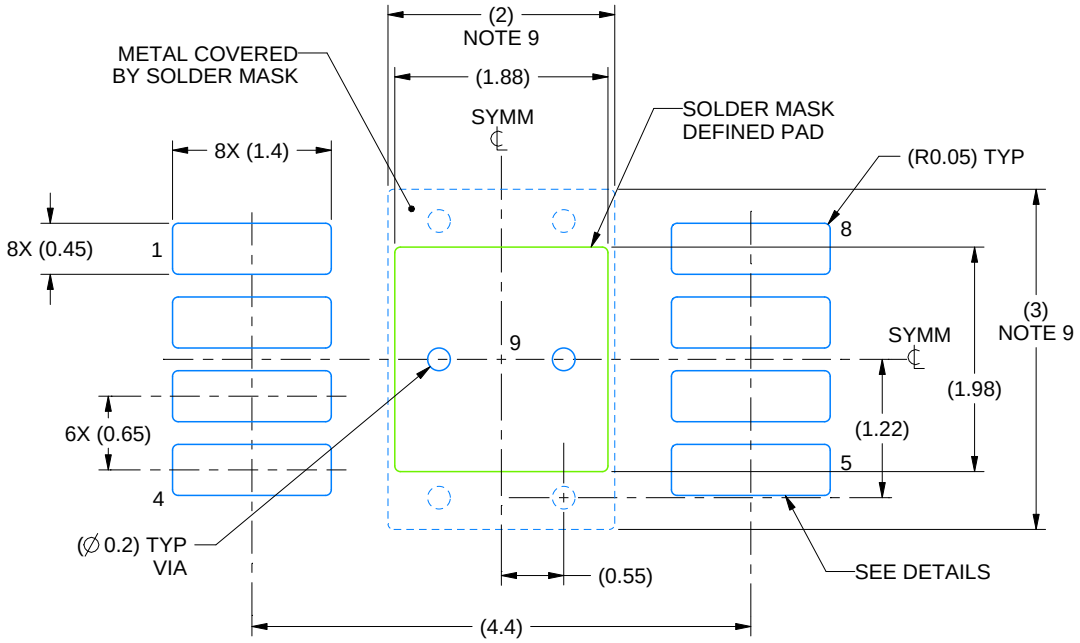
SMALL OUTLINE PACKAGE



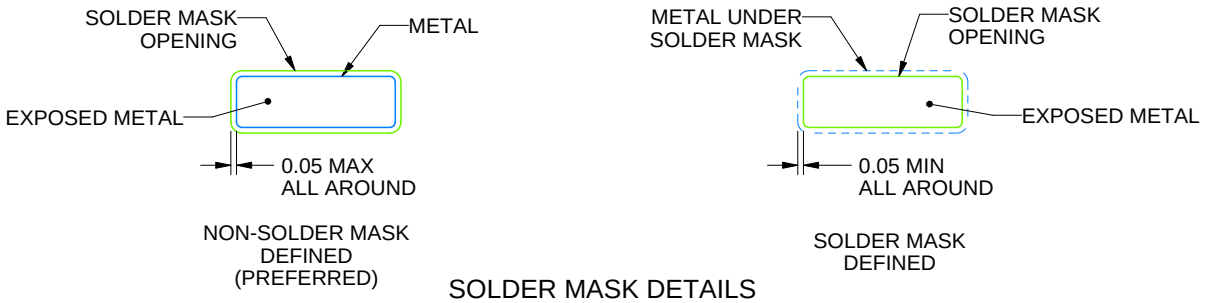
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

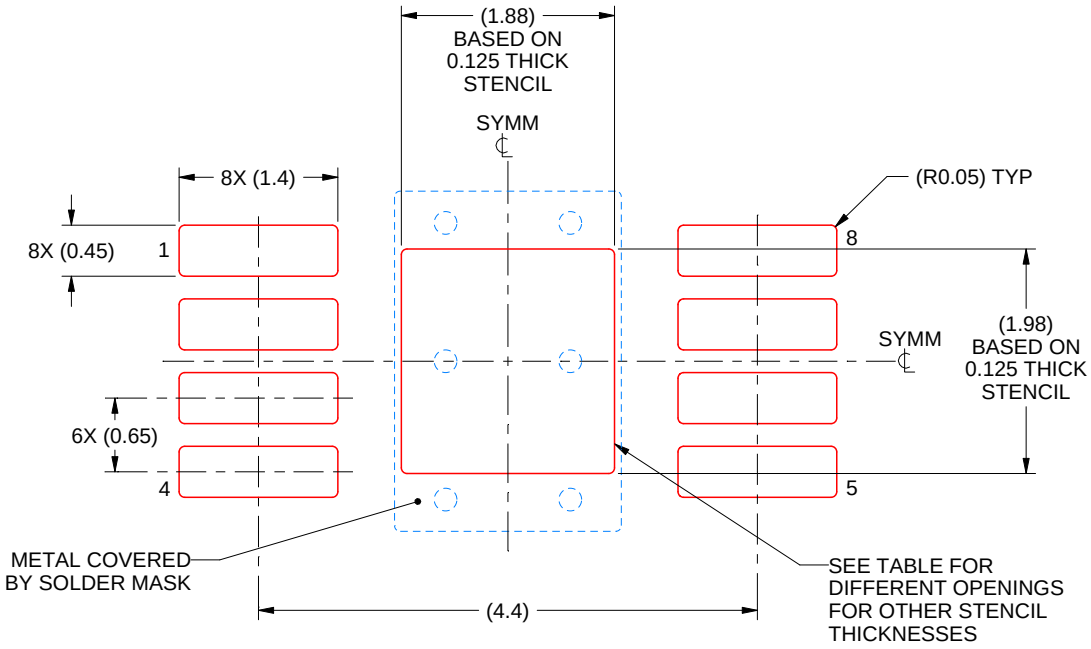


SOLDER MASK DETAILS

4218837/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.10 X 2.21
0.125	1.88 X 1.98 (SHOWN)
0.15	1.72 X 1.81
0.175	1.59 X 1.67

4218837/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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