



36V, Precision, Low-Noise, Wide-Band Amplifier

MAX9632

General Description

The MAX9632 is a low-noise, precision, wide-band operational amplifier that can operate in a very wide +4.5V to +36V supply voltage range. The IC operates in dual ($\pm 18V$) mode.

The exceptionally fast settling time and low distortion make the IC an excellent solution for precision acquisition systems. The rail-to-rail output swing maximizes the dynamic range when driving high-resolution 24-bit $\Sigma\Delta$ ADCs even with low supply voltages.

The IC achieves 55MHz of gain-bandwidth product and ultra-low $0.94nV/\sqrt{Hz}$ input voltage noise with only 3.9mA of quiescent current.

The IC is offered in 8-pin SO, μMAX ®, and TDFN packages and is rated for operation over the $-40^{\circ}C$ to $+125^{\circ}C$ temperature range.

Applications

High-Resolution ADC Drivers
High-Resolution DAC Buffers
Medical Imaging
Low-Noise Signal Processing
Test and Measurement Systems
ATE

Features

- ◆ $0.94nV/\sqrt{Hz}$ Ultra-Low Input Voltage Noise
- ◆ Very Fast 600ns Settling Time to 16-Bit Accuracy
- ◆ THD of -128dB at 10kHz
- ◆ Low Input Offset Voltage 125 μV (max)
- ◆ Low Input Offset Temperature Drift $0.5\mu V/^{\circ}C$ (max)
- ◆ Gain-Bandwidth Product 55MHz
- ◆ +4.5V to +36V Wide Supply Range
- ◆ Rail-to-Rail Output
- ◆ Unity-Gain Stable
- ◆ 8-Pin SO and TDFN Packages
- ◆ ESD 8kV HBM and 1kV CDM

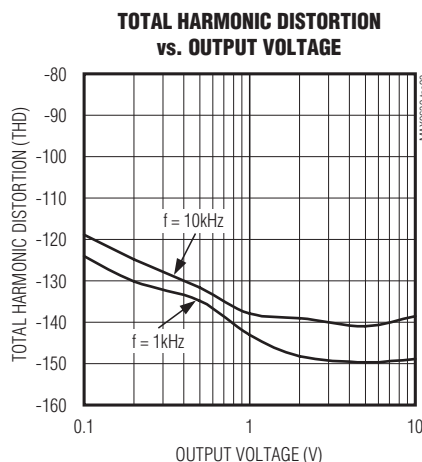
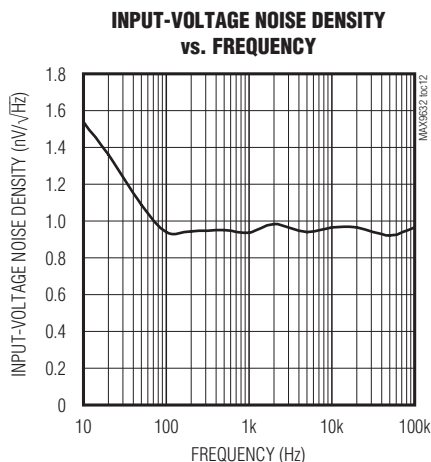
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX9632ASA+	$-40^{\circ}C$ to $+125^{\circ}C$	8 SO	—
MAX9632ATA+	$-40^{\circ}C$ to $+125^{\circ}C$	8 TDFN-EP*	BML
MAX9632AUA+	$-40^{\circ}C$ to $+125^{\circ}C$	8 μMAX	—

+ Denotes a lead(Pb)-free/RoHS-compliant package.

*EP = Exposed pad.

μMAX is a registered trademark at Maxim Integrated Products, Inc.



36V, Precision, Low-Noise, Wide-Band Amplifier

ABSOLUTE MAXIMUM RATINGS

VCC to VEE -0.3V to +40V
 All Other Pins..... (VEE - 0.3V) to (VCC + 0.3V)
 Short-Circuit (GND) Duration, OUT 10s
 Continuous Input Current (any pin)..... ± 20 mA
 Continuous Power Dissipation (TA = +70°C) (Note 1)
 Multilayer SO (derate 7.4mW/°C above +70°C) 588mW
 Multilayer TDFN (derate 23.8mW/°C above +70°C) ... 1905mW
 Multilayer μ MAX (derate 4.8mW/°C above +70°C) .. 387.8mW

ESD Protection

HBM 8kV
 CDM 1kV
 Operating Temperature Range -40°C to +125°C
 Junction Temperature +150°C
 Lead Temperature (soldering, 10s) +300°C
 Soldering Temperature (reflow) +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

6 TDFN

Junction-to-Ambient Thermal Resistance (θ_{JA}) 42°C/W
 Junction-to-Case Thermal Resistance (θ_{JC}) 8°C/W

8 SO

Junction-to-Ambient Thermal Resistance (θ_{JA}) 136°C/W
 Junction-to-Case Thermal Resistance (θ_{JC}) 38°C/W

8 μ MAX

Junction-to-Ambient Thermal Resistance (θ_{JA}) 206.3°C/W
 Junction-to-Case Thermal Resistance (θ_{JC}) 42°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maxim-ic.com/thermal-tutorial.

ELECTRICAL CHARACTERISTICS

(VCC = 15V, VEE = -15V, RL = 10k Ω to VGND, VIN+ = VIN- = VGND = 0V, VSHDN = VGND, TA = -40°C to +125°C. Typical values are at TA = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage Range	V _{CC}	Guaranteed by PSRR	4.5		36	V
Supply Current	I _{CC}			3.9	6.5	mA
Power-Supply Rejection Ratio	PSRR	T _A = +25°C	125	140		dB
		-40°C ≤ T _A ≤ +125°C	120			
SHUTDOWN						
Shutdown Input Voltage	V _{SHDN}	Device disabled	V _{CC} - 0.35		V _{CC}	V
		Device enabled	V _{EE}		V _{CC} - 3.0	
Shutdown Current	I _{SHDN}	V _{SHDN} = V _{CC}		1	15	μA
DC SPECIFICATIONS						
Input Offset Voltage	V _{OS}	T _A = +25°C		30	125	μV
		-40°C ≤ T _A ≤ +125°C			165	
Input Offset Voltage Drift	±ΔV _{OS}	(Note 3)		0.15	0.5	μV/°C
Input Bias Current	I _B			30	180	nA
Input Offset Current	I _{OS}			15	100	nA
Input Common-Mode Range	V _{CM}	Guaranteed by CMRR	V _{EE} + 1.8		V _{CC} - 1.4	V

36V, Precision, Low-Noise, Wide-Band Amplifier

ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = 15V$, $V_{EE} = -15V$, $R_L = 10k\Omega$ to V_{GND} , $V_{IN+} = V_{IN-} = V_{GND} = 0V$, $V_{SHDN} = V_{GND}$, $T_A = -40^\circ C$ to $+125^\circ C$. Typical values are at $T_A = +25^\circ C$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Common-Mode Rejection Ratio	CMRR	$V_{EE} + 1.8V \leq V_{CM} \leq V_{CC} - 1.4V$, $T_A = +25^\circ C$	120	135		dB
		$V_{EE} + 1.8V \leq V_{CM} \leq V_{CC} - 1.4V$, $-40^\circ C \leq T_A \leq +125^\circ C$	110			
Large-Signal Gain	A_{VOL}	$V_{EE} + 0.2V \leq V_{OUT} \leq V_{CC} - 0.2V$, $R_L = 10k\Omega$	125	140		dB
		$V_{EE} + 0.6V \leq V_{OUT} \leq V_{CC} - 0.6V$, $R_L = 600\Omega$	120	135		
Output Voltage Swing	V_{OH}	$V_{CC} - V_{OUT}$		50	150	mV
		$R_L = 600\Omega$		150	400	
	V_{OL}	$V_{OUT} - V_{EE}$		50	150	
		$R_L = 600\Omega$		150	400	
Short-Circuit Current	I_{SC}	$T_A = +25^\circ C$		56		mA
AC SPECIFICATIONS						
Gain-Bandwidth Product	GBWP			55		MHz
Slew Rate	SR	$0 \leq V_{OUT} \leq 5V$		30		V/ μs
Settling Time	t_S	To 0.0015%, $V_{OUT} = 10V_{P-P}$, $C_L = 100pF$, $A_V = 1V/V$		600		ns
Total Harmonic Distortion	THD	$f = 1kHz$, $V_{OUT} = 3V_{RMS}$, $R_L = 600\Omega$, $A_V = 1V/V$		-136		dB
		$f = 10kHz$, $V_{OUT} = 3V_{RMS}$, $R_L = 600\Omega$, $A_V = 1V/V$		-128		
Input-Voltage Noise Density	e_N	$f = 1kHz$		0.94		nV/ \sqrt{Hz}
Input Voltage Noise		$0.1Hz \leq f \leq 10Hz$		65		nV $_{P-P}$
Input-Current Noise Density	i_N	$f = 1kHz$		3.75		pA/ \sqrt{Hz}
Capacitive Loading	C_L	No sustained oscillation, $A_V = 1V/V$		350		pF

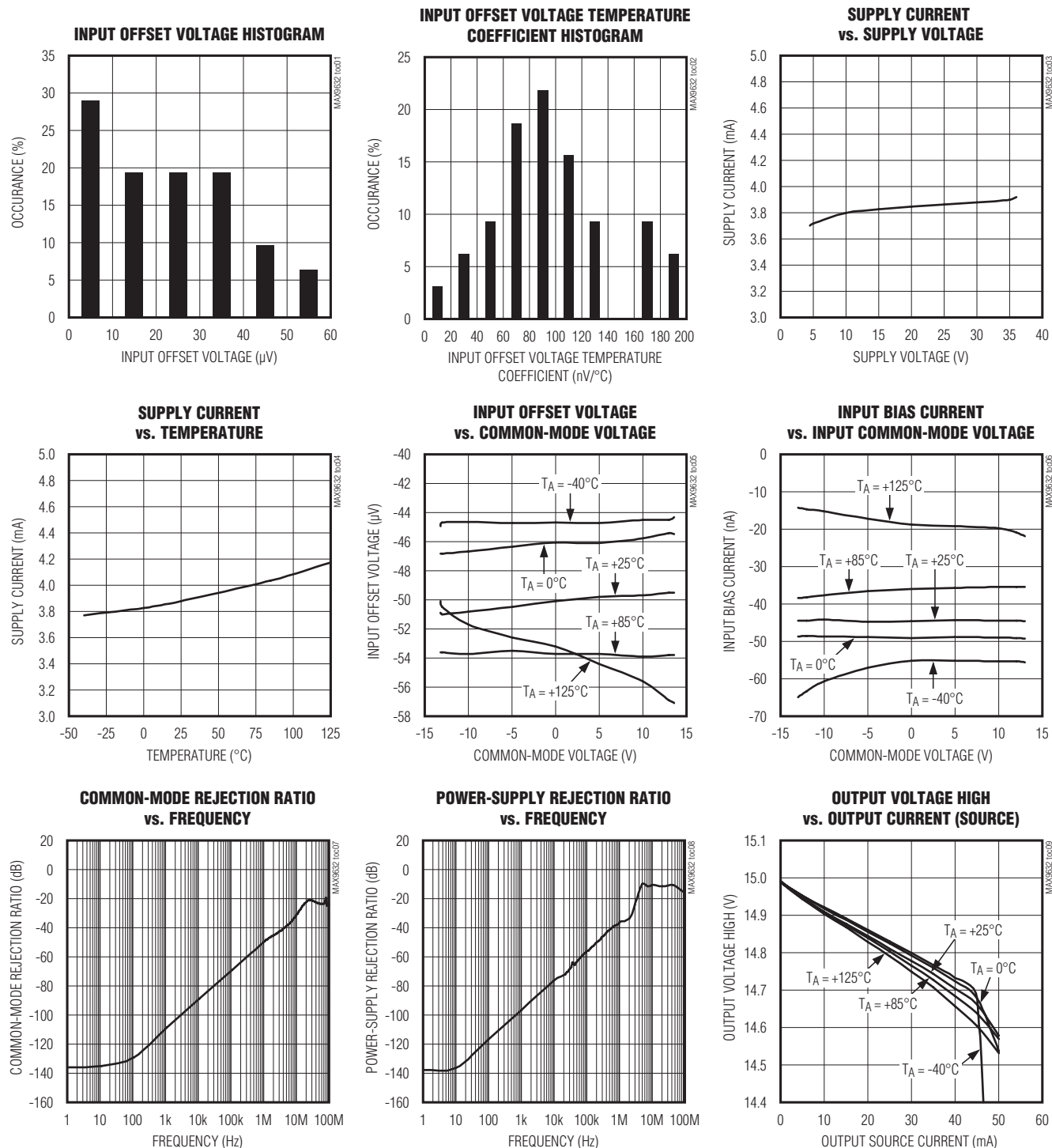
Note 2: All devices are 100% production tested at $T_A = +25^\circ C$. Temperature limits are guaranteed by design.

Note 3: Guaranteed by design.

36V, Precision, Low-Noise, Wide-Band Amplifier

Typical Operating Characteristics

($V_{CC} = 15V$, $V_{EE} = -15V$, $R_L = 10k\Omega$ to V_{GND} , $V_{IN+} = V_{IN-} = V_{GND} = 0V$, $V_{SHDN} = V_{GND}$, $T_A = -40^\circ C$ to $+125^\circ C$. Typical values are at $T_A = +25^\circ C$, unless otherwise noted.)

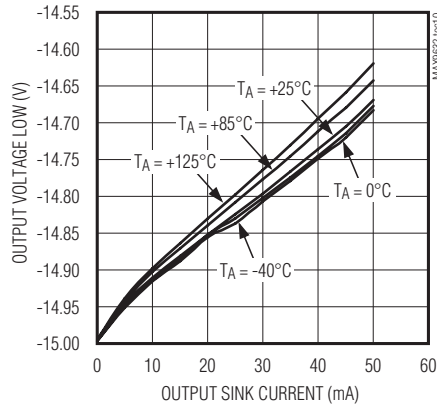


36V, Precision, Low-Noise, Wide-Band Amplifier

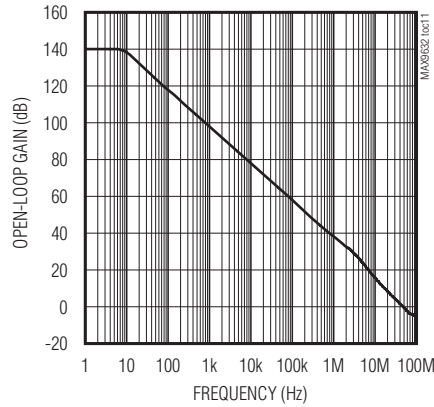
Typical Operating Characteristics (continued)

($V_{CC} = 15V$, $V_{EE} = -15V$, $R_L = 10k\Omega$ to V_{GND} , $V_{IN+} = V_{IN-} = V_{GND} = 0V$, $V_{SHDN} = V_{GND}$, $T_A = -40^\circ C$ to $+125^\circ C$. Typical values are at $T_A = +25^\circ C$, unless otherwise noted.)

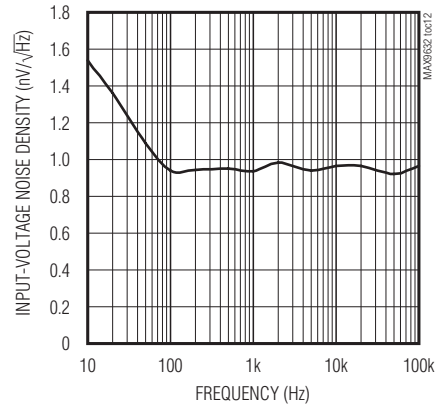
OUTPUT VOLTAGE LOW vs. OUTPUT CURRENT (SINK)



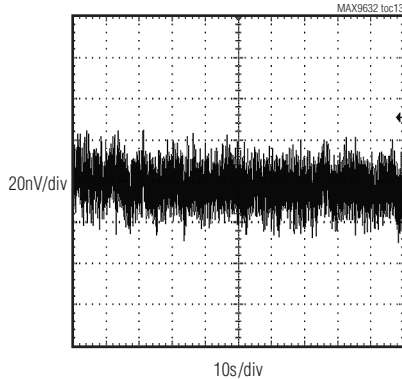
OPEN-LOOP GAIN vs. FREQUENCY



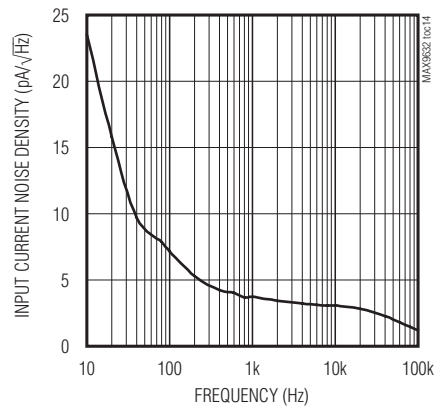
INPUT-VOLTAGE NOISE DENSITY vs. FREQUENCY



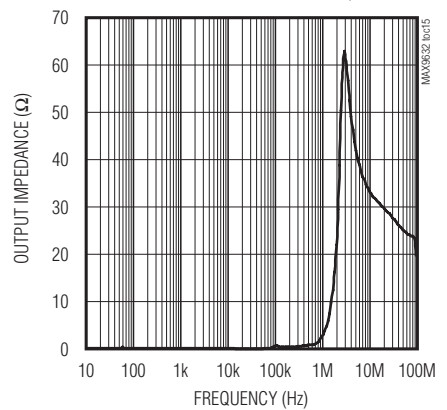
0.1Hz TO 10Hz NOISE vs. TIME



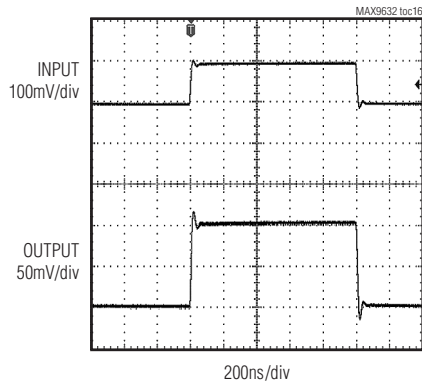
INPUT-CURRENT NOISE DENSITY vs. FREQUENCY



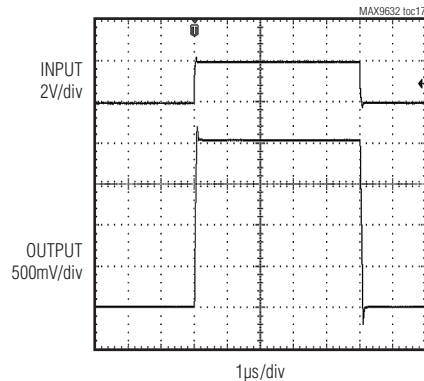
OUTPUT IMPEDANCE vs. FREQUENCY



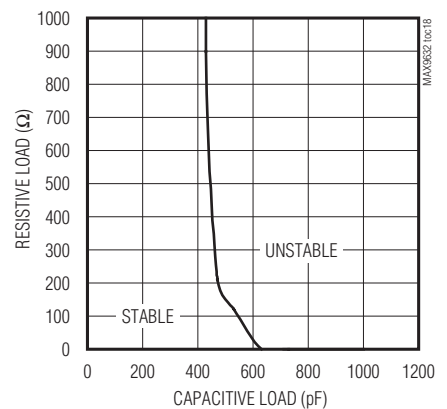
INPUT SMALL-SIGNAL STEP RESPONSE



INPUT LARGE-SIGNAL STEP RESPONSE



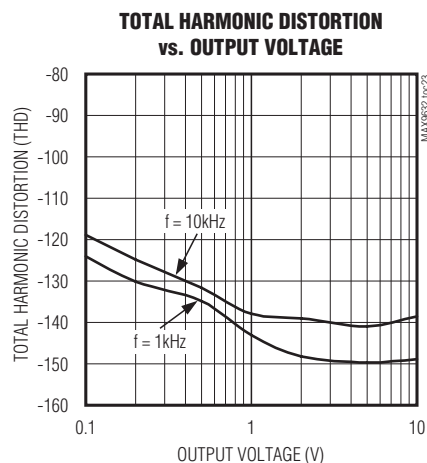
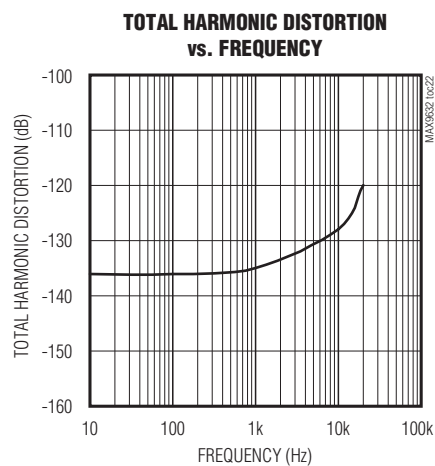
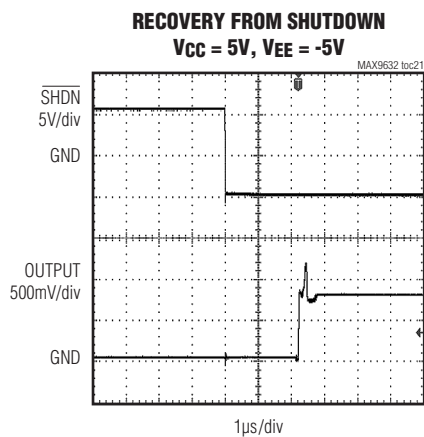
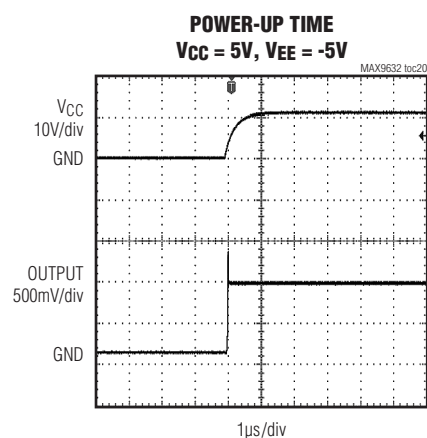
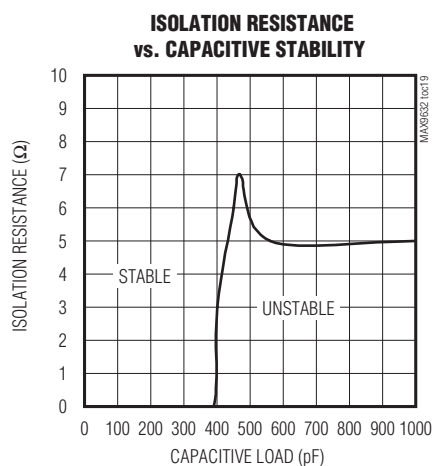
STABILITY vs. CAPACITIVE AND RESISTIVE LOAD PARALLEL



36V, Precision, Low-Noise, Wide-Band Amplifier

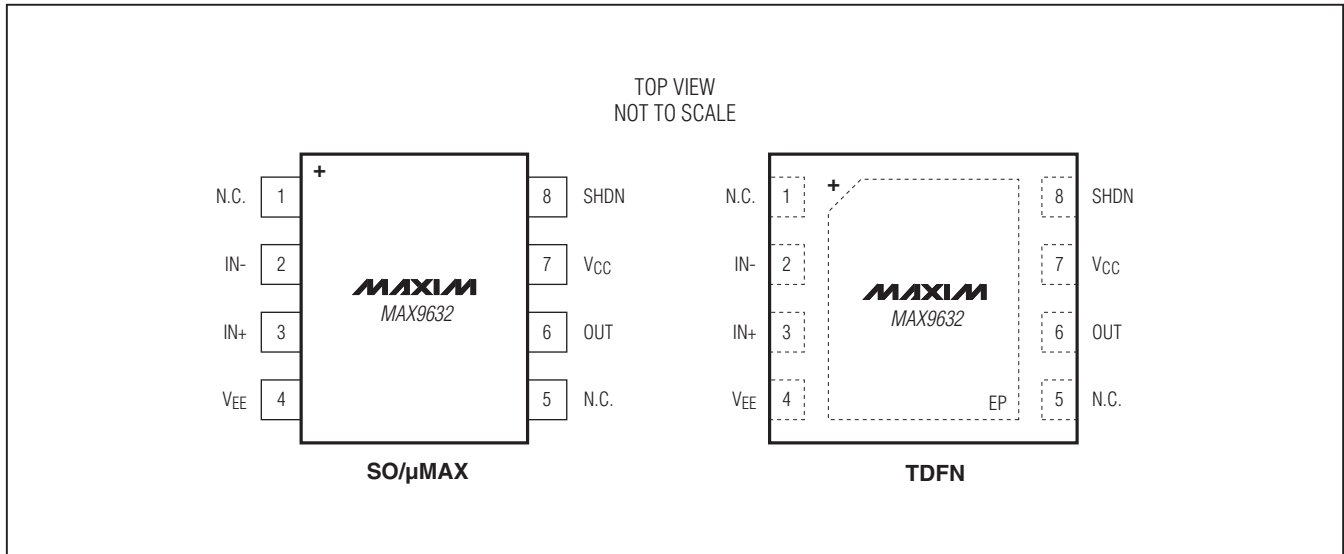
Typical Operating Characteristics (continued)

($V_{CC} = 15V$, $V_{EE} = -15V$, $R_L = 10k\Omega$ to V_{GND} , $V_{IN+} = V_{IN-} = V_{GND} = 0V$, $V_{SHDN} = V_{GND}$, $T_A = -40^\circ C$ to $+125^\circ C$. Typical values are at $T_A = +25^\circ C$, unless otherwise noted.)



36V, Precision, Low-Noise, Wide-Band Amplifier

Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1, 5	N.C.	Not Connected
2	IN-	Negative Input
3	IN+	Positive Input
4	VEE	Negative Supply Voltage
6	OUT	Output
7	VCC	Positive Supply Voltage
8	SHDN	Active-High Shutdown
—	EP	Exposed Pad (TDFN Only). Connect to a large VEE plane to maximize thermal performance. Not intended as an electrical connection point.

36V, Precision, Low-Noise, Wide-Band Amplifier

Detailed Description

The MAX9632 is designed in a new 36V, high-speed complementary BiCMOS process that is optimized for excellent AC dynamic performance combined with high-voltage operation.

The IC offers precision, high-bandwidth, ultra-low noise and exceptional distortion performance.

The IC is unity-gain stable and operates either with single-supply voltage up to 36V or with dual supplies up to $\pm 18V$.

Applications Information

Operating Supply Voltage

The IC can operate with dual supplies from $\pm 2.25V$ to $\pm 18V$ or with a single supply from $+4.5V$ to $+36V$ with respect to ground. Even though the IC supports high-voltage operation with excellent performance, the device can also operate in very popular applications at 5V.

Low Noise and Low Distortion

The IC is designed for extremely low-noise applications such as professional audio equipment, very high performance instrumentations, automated test equipment, and medical imaging. The low noise, combined with fast settling time, makes it ideal to drive high-resolution sigma-delta or SARs analog-to-digital converters.

The IC is also designed for ultra-low-distortion performance. THD specifications in the *Electrical Characteristics* table and *Typical Operating Characteristics* are calculated up to the fifth harmonic. Even when driving high-voltage swing up to 10V_{P-P}, the IC maintains excellent low distortion operation over and above 100kHz of bandwidth.

Rail-to-Rail Output Stage

The output stage swings to within 50mV (typ) of either power-supply rail with a 10k Ω load and provides a 55MHz GBW with a 30V/s slew rate. The device is unity-gain stable and can drive a 100pF capacitive load without compromising stability. Stability with higher capacitive loads can be improved by adding an isolation resistor in series with the op-amp output. This resistor improves the circuit's phase margin by isolating the load capacitor from the amplifier's output. The *Typical Operating Characteristics* show a profile of the isolation resistor and capacitive load values that maintain the device into the stable region.

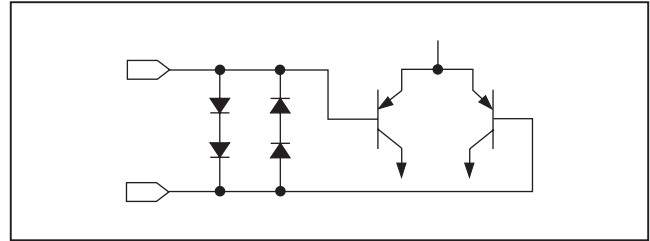


Figure 1. Input Protection Circuit

Input Differential Voltage Protection

During normal op-amp operation, the inverting and noninverting inputs of the IC are at essentially the same voltage. However, either due to fast input voltage transients or other fault conditions, these inputs can be forced to be at two different voltages.

Internal back-to-back diodes protect the inputs from an excessive differential voltage (Figure 1). Therefore, IN+ and IN- can be any voltage within the range shown in the *Absolute Maximum Ratings* section. Note the protection time is still dependent on the package thermal limits.

If the input signal is fast enough to create the internal diodes' forward bias condition, the input signal current must be limited to 20mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the signal input current. Care should be taken in choosing the input series resistor value, since it degrades the low-noise performance of the device.

Shutdown

The shutdown is referenced to the positive supply. See the *Electrical Characteristics* table for the proper levels of functionality. A high level (above $V_{CC} - 0.35V$) disables the op amp and puts the output into a high-impedance state. A low level (below $V_{CC} - 3V$) enables the device. As an example, if the op amp is powered with dual supplies of $\pm 15V$, the device is enabled when shutdown is at or below 12V. The device is disabled when shutdown is at or above 14.65V. If the op amp is powered with a single supply of 36V, the device is enabled when shutdown is at or below 33V. The device is disabled when shutdown is at or above 35.65V. This input must be connected to a valid high or low voltage and should not be left disconnected.

Power Supplies and Layout

The MAX9632 can operate with dual supplies from $\pm 2.25V$ to $\pm 18V$ or with a single supply from $+4.5V$ to $+36V$ with respect to ground. When used with dual supplies, bypass both VCC and VEE with their own 0.1 μF capacitor to ground. When used with a single supply, bypass VCC with a 0.1 μF capacitor to ground.

36V, Precision, Low-Noise, Wide-Band Amplifier

Careful layout technique helps optimize performance by decreasing the amount of stray capacitance at the op amp's inputs and outputs. To decrease stray capacitance, minimize trace lengths by placing external components close to the op amp's pins.

For high-frequency designs, ground vias are critical to provide a ground return path for high-frequency signals and should be placed near the decoupling capacitors. Signal routing should be short and direct to avoid parasitic effects. Avoid using right angle connectors since they may introduce a capacitive discontinuity and ultimately limit the frequency response.

Electrostatic Discharge (ESD)

The IC has built-in circuits to protect it from ESD events. An ESD event produces a short, high-voltage pulse that is transformed into a short current pulse once it discharges through the device. The built-in protection circuit provides a current path around the op amp that prevents it from being damaged. The energy absorbed by the protection circuit is dissipated as heat.

ESD protection is guaranteed up to $\pm 8\text{kV}$ with the Human Body Model (HBM). The Human Body Model simulates the ESD phenomenon wherein a charged body directly transfers its accumulated electrostatic charge to the ESD-sensitive device. A common example of this phenomenon is when a person accumulates static charge by walking across a carpet and then transfers all of the charge to an ESD-sensitive device by touching it.

Not all ESD events involve the transfer of charge into the device. ESD from a charged device to another body is also a common form of ESD.

If a charged device comes into contact with another conductive body that is at a lower potential, it discharges into that body. Such an ESD event is known as Charged Device Model (CDM) ESD, which can be even more destructive than HBM ESD (despite its shorter pulse duration) because of its high current. The IC guarantees CDM ESD protection up to $\pm 1\text{kV}$.

Driving High-Resolution Sigma-Delta ADCs

The MAX9632's excellent AC specifications and 55MHz bandwidth are a good fit for driving high-speed, precision delta-sigma ADCs. These ADCs require an ultra-low noise op amp to achieve signal-to-noise ratios (SNR) better than 100dB. The MAX11040 is a 24-bit, 4-channel, simultaneous-sampling ADC with 117dB SNR at 1ksps and 106dB at 16ksps. The MAX11040 measures analog inputs up to $\pm 2.2\text{V}$. Sampling up to 64ksps, the MAX11040 achieves better than -94dB THD and 94dB SFDR.

The MAX11040 measures four differential inputs simultaneously, outputting the data through an SPI™ interface to allow daisy-chaining the data outputs and inputs together. Therefore, up to eight MAX11040 devices can be placed in parallel to measure up to 32 inputs simultaneously. This is ideal for 3-phase power monitoring that requires multiple current and voltage readings and very wide dynamic range.

The *Typical Application Circuit* shows an example of the MAX9632 driving the MAX11040.

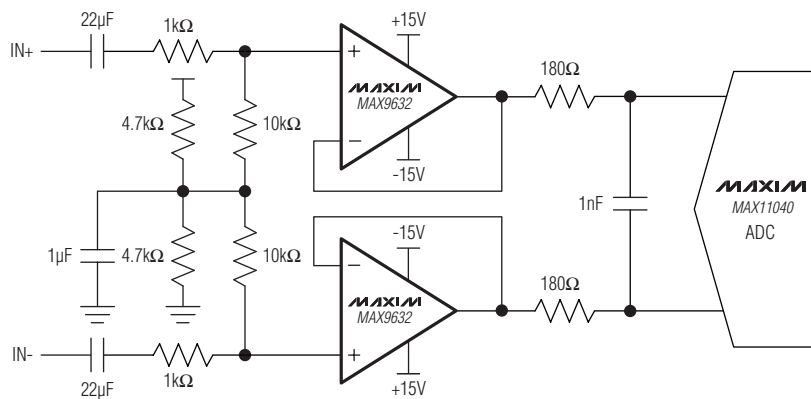
Chip Information

PROCESS: BiCMOS

SPI is a trademark of Motorola, Inc.

36V, Precision, Low-Noise, Wide-Band Amplifier

Typical Application Circuit



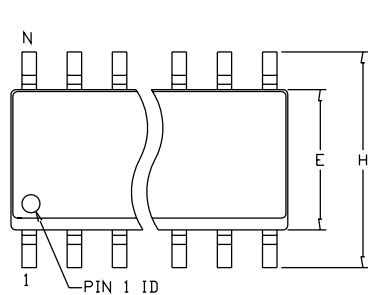
36V, Precision, Low-Noise, Wide-Band Amplifier

Package Information

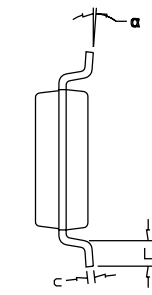
For the latest package outline information and land patterns (footprints), go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 SO	S8+2	21-0041	90-0096
8 TDFN-EP	T833+3	21-0137	90-0060
8 μ MAX	U8+3	21-0036	90-0092

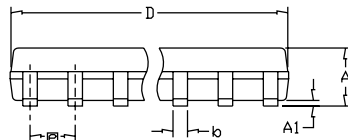
MAX9632



TOP VIEW



END VIEW



SIDE VIEW

COMMON DIMENSIONS				
SYMBOL	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
A	.053	.069	1.35	1.75
A1	.004	.010	0.10	0.25
b	.014	.019	0.35	0.49
c	.007	.010	0.19	0.25
E	.150	.157	3.80	4.00
e	.050 BSC		1.27 BSC	
H	.228	.244	5.80	6.20
L	.016	.050	0.40	1.27
a	0°	8°	0°	8°

VARIATION A				
SYMBOL	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
D	.189	.197	4.80	5.00
N	8			
MS012	AA			
PKG. CODE	S8-2, S8-4, S8-5, S8-6F, S8-7F, S8-8F, S8-10F, S8-11F, S8-16F			

VARIATION B				
SYMBOL	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
D	.337	.344	8.55	8.75
N	14			
MS012	AB			
PKG. CODE	S14-1, S14-4, S14-5, S14-6, S14M-4, S14M-5, S14M-6, S14M-7			

VARIATION C				
SYMBOL	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
D	.386	.394	9.80	10.00
N	16			
MS012	AC			
PKG. CODE	S16-1, S16-3, S16-5, S16-6, S16-8, S16-7F, S16-9F, S16-10F, S16M-3, S16M-6			

NOTES:

- ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.
- MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC # 10-0131.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.15 MM (.006") PER SIDE.
- LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
- MEETS JEDEC MS012
- ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

MAXIM

TITLE:
PACKAGE OUTLINE,
8L, 14L, 16L SOIC .150 INCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	1/1
	21-0041	C	

Package Information (continued)

TOP VIEW

Dimensions: E (width), D (height), $\frac{E}{2}$ (center offset), $\frac{D}{2}$ (center offset). Marking: 1 (PIN 1 INDEX AREA), A (MARKING), 8 (MARKING).

SIDE VIEW

Dimensions: A (thickness), A2 (height), A1 (height).

BOTTOM VIEW

Dimensions: E2 (width), D2 (height), b (pitch), k (height), e (pitch), $[(N/2)-1] \times e$ REF. (pitch). Labels: DETAIL A, 0.35x0.35 (pad size), PIN 1 ID, DAP, N (number of pins), 1 (PIN 1 INDEX AREA).

DETAIL A

Labels: (R IS OPTIONAL), L (height), $\frac{E}{2}$ (center offset), $\frac{D}{2}$ (center offset), TERMINAL TIP, EVEN TERMINAL, ODD TERMINAL.

TABLE

TITLE:		
PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm		
APPROVAL	DOCUMENT CONTROL NO.	REV.
	21-0137	J 1/2

—DRAWING NOT TO SCALE—

36V, Precision, Low-Noise, Wide-Band Amplifier

Package Information (continued)

For the latest package outline information and land patterns (footprints), go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.


COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS								
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e	
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF	
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF	
T1033MK-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF	
T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF	
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF	
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF	
T1433-3F	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF	

NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

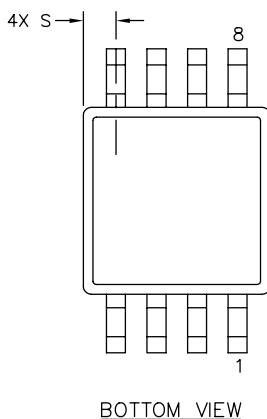
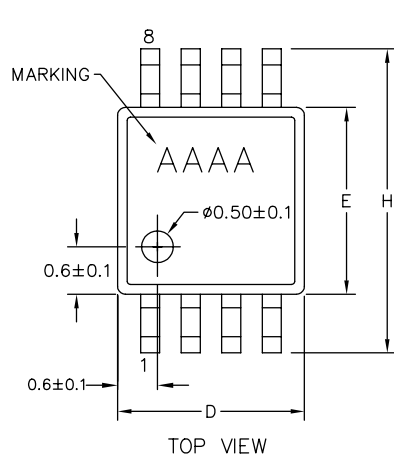
—DRAWING NOT TO SCALE—

		
TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm		
APPROVAL	DOCUMENT CONTROL NO. 21-0137	REV. J 2/2

36V, Precision, Low-Noise, Wide-Band Amplifier

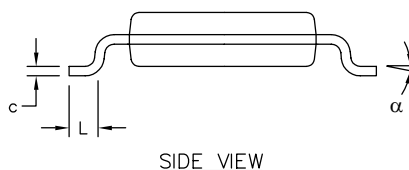
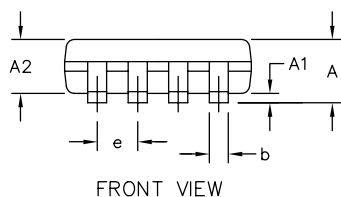
Package Information (continued)

For the latest package outline information and land patterns (footprints), go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.043	—	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
b	0.010	0.014	0.25	0.36
c	0.005	0.007	0.13	0.18
D	0.114	0.122	2.90	3.10
e	0.0256 BSC		0.65 BSC	
E	0.114	0.122	2.90	3.10
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°
S	0.0207 BSC		0.5250 BSC	

PKG. CODES:
U8-1; U8-3; U8CN-1



NOTES:

1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COMPLIES TO JEDEC MO-187, LATEST REVISION, VARIATION AA.
5. MARKING SHOWN IS FOR PKG. ORIENTATION ONLY.
6. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

—DRAWING NOT TO SCALE—

MAXIM			
TITLE: PACKAGE OUTLINE, 8L uMAX/uSOP			
APPROVAL	DOCUMENT CONTROL NO. 21-0036	REV. L	1/1

36V, Precision, Low-Noise, Wide-Band Amplifier

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/10	Initial release	—
1	4/11	Updated short-circuit current spec	3
2	8/11	Updated TDFN land pattern number	11
3	10/11	Added μ MAX package	1, 2, 7

MAX9632

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