



CYPRESS

PRELIMINARY

CY37512V

UltraLogic™ 3.3V 512-Macrocell ISR™ CPLD

Features

- 512 macrocells in 32 logic blocks
- 3.3V In-System Reprogrammable™ (ISR™)
 - JTAG-compliant on-board programming
 - Design changes don't cause pinout changes
 - Design changes don't cause timing changes
- IEEE standard 3.3V operation
 - 3.3V ISR
 - 5V tolerant
- Up to 264 I/Os
 - plus 5 dedicated inputs including 4 clock inputs
- High speed
 - $f_{MAX} = 83$ MHz

— $t_{PD} = 15$ ns

— $t_S = 8$ ns

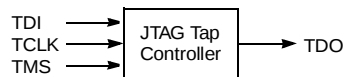
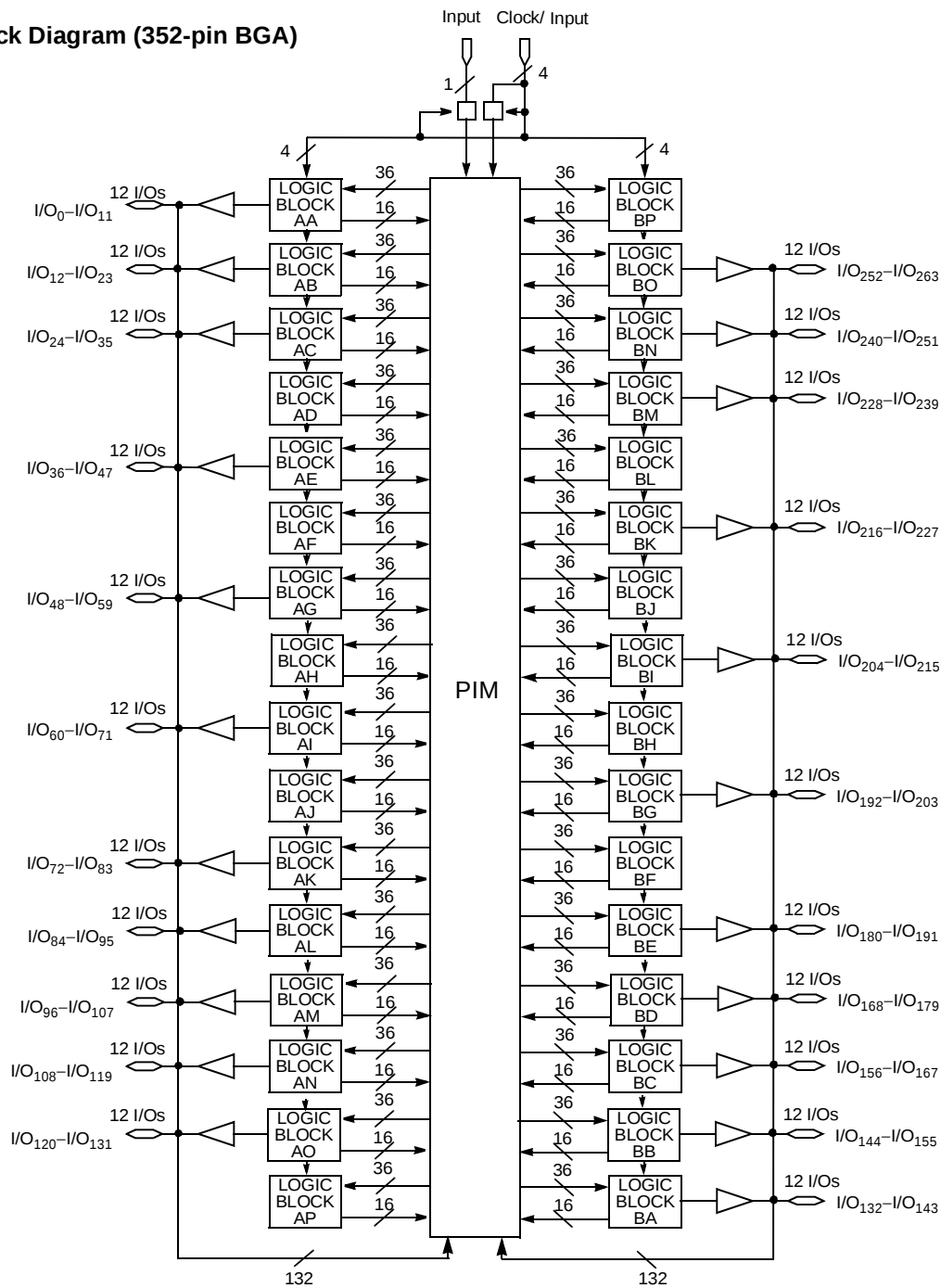
— $t_{CO} = 8$ ns

- Product-term clocking
- IEEE 1149.1 JTAG boundary scan
- Programmable slew rate control on individual I/Os
- Low power option on individual logic block basis
- User-Programmable Bus Hold capabilities on all I/Os
- Simple Timing Model
- PCI compliant^[1]
- Available in 208-pin PQFP, 256/352-lead BGA packages
- Pinout compatible with the CY37512, CY37256/37256V, CY37384/37384V

Note:

1. Due to the 5-V tolerant nature of the I/Os, the I/Os are not clamped to V_{CC} .

Logic Block Diagram (352-pin BGA)



37512V-1

Selection Guide

	CY37512V-83	CY37512V-66
Maximum Propagation Delay, t_{PD} (ns)	15	20
Minimum Set-Up, t_S (ns)	8	10
Maximum Clock to Output, t_{CO} (ns)	8	10
Typical Supply Current, I_{CC} (mA) in Low Power Mode	240	240

Functional Description

The CY37512V is an In-System Reprogrammable (ISR) Complex Programmable Logic Device (CPLD) and is part of the Ultra37000™ family of high-density, high-speed CPLDs. Like all members of the Ultra37000 family, the CY37512V is designed to bring the ease of use and high performance of the 22V10 to high-density PLDs.

# of Pins	# Buried Macrocells	# I/O Macrocells	Package Types
208	352	160	PQFP
256	320	192	BGA
352	248	264	BGA

For a more detailed description of the architecture and features of the CY37512V see the Ultra37000 family data sheet.

Fully Routable with 100% Logic Utilization

The CY37512V is designed with a robust routing architecture which allows utilization of the entire device with a fixed pinout. This makes Ultra37000 optimal for implementing on-board design changes using ISR without changing pinouts.

Simple Timing Model

The CY37512V features a very simple timing model with predictable delays. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. The timing model allows for design changes with ISR without causing changes to system performance.

Low Power Operation

Each Logic Block of the CY37512V can be configured as either High-Speed (default) or Low-Power. In the Low-Power mode,

the logic block consumes approximately 50% less power and slows down by t_{LP} .

Output Slew Rate Control

Each output can be configured with either a fast edge rate (default) for high performance, or a slow edge rate for added noise reduction. In the fast edge rate mode, outputs switch at 3V/ns max. and in the slow edge rate mode, outputs switch at 1V/ns max. There is a nominal delay for I/Os using the slow edge rate mode.

In System Reprogramming

The CY37512V can be programmed in system using IEEE 1149.1 compliant JTAG programming protocol. The CY37512V can also be programmed on a number of traditional parallel programmers including Cypress's *Impulse3™* programmer and industry standard third-party programmers. For an overview of ISR programming, refer to the Ultra37000 Family data sheet and for UltraISR cable and software specifications, refer to InSRkit: ISR Programming data sheet (CY3600i).

User-Programmable Bus Hold

All outputs of the CY37512V can either be configured into bus hold mode or left floating. When in bus hold mode, the undriven outputs retain their last value with a weak latch. This feature allows the designer the flexibility of either eliminating or including external pull-up/pull-down resistors. Enabling this feature affects all I/Os simultaneously.

Design Tools

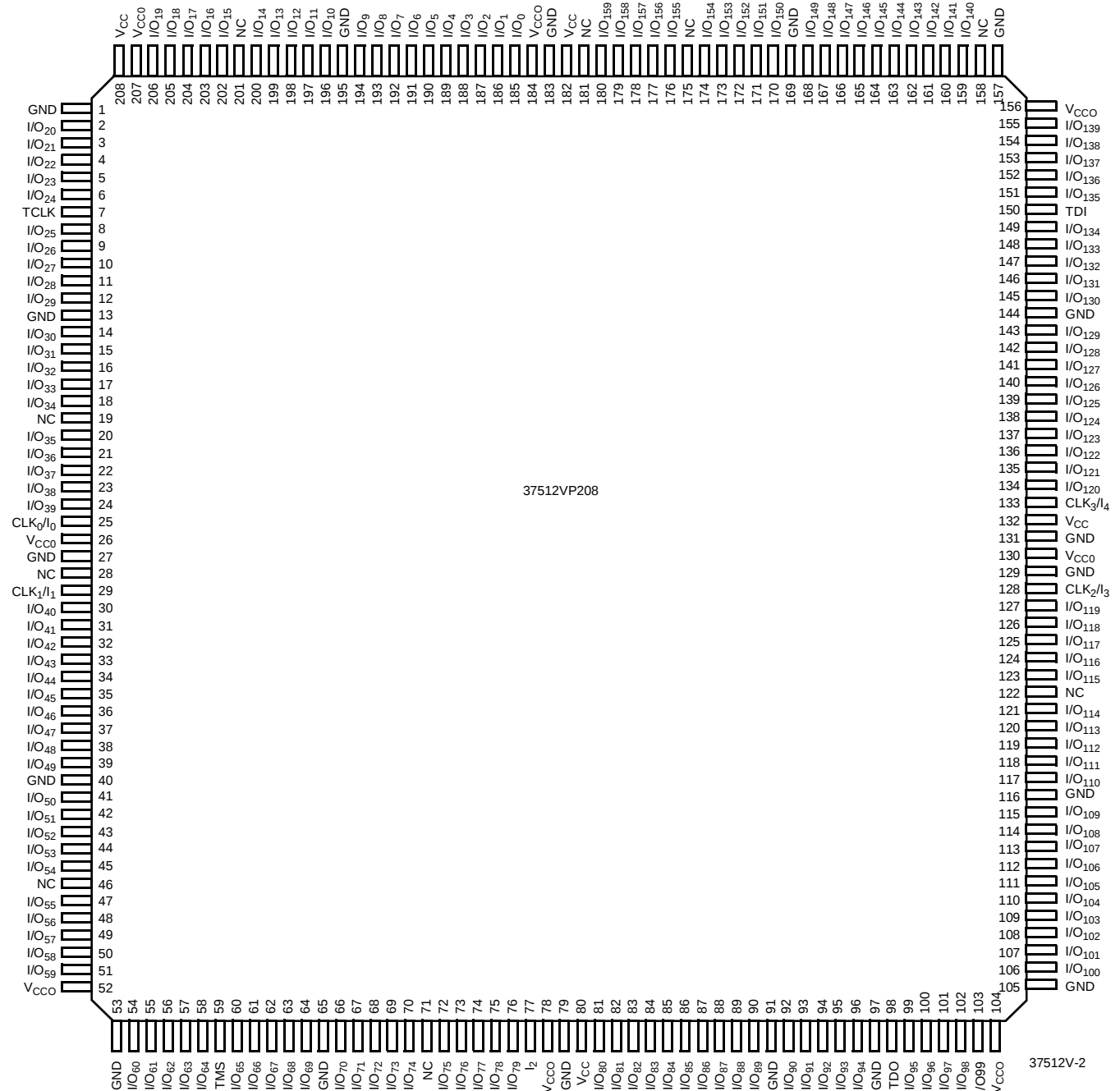
Development software for the CY37512V is available from Cypress's *Warp™* or third-party bolt-in software packages as well as a number of third-party development packages. Please refer to the *Warp* or third-party tool support data sheets for further information.



Pin Configurations

208-pin PQFP/CQFP

Top View





Pin Configurations

256-ball BGA Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	I/O ₂₁	NC	I/O ₁₆	I/O ₁₂	I/O ₉	I/O ₇	I/O ₄	I/O ₀	I/O ₁₉₀	I/O ₁₈₉	I/O ₁₈₆	I/O ₁₈₂	NC	I/O ₁₇₈	I/O ₁₇₅	NC	NC	I/O ₁₆₉	I/O ₁₆₈	A
B	I/O ₂₃	I/O ₂₀	I/O ₁₉	I/O ₁₈	I/O ₁₅	I/O ₁₁	I/O ₈	I/O ₅	I/O ₁	I/O ₁₉₁	I/O ₁₈₇	I/O ₁₈₅	I/O ₁₈₁	NC	NC	I/O ₁₇₄	I/O ₁₇₁	I/O ₁₇₀	NC	I/O ₁₆₆	B
C	NC	NC	I/O ₂₂	NC	I/O ₁₇	I/O ₁₄	I/O ₁₀	I/O ₆	I/O ₂	NC	I/O ₁₈₈	I/O ₁₈₄	I/O ₁₈₀	I/O ₁₇₉	I/O ₁₇₆	I/O ₁₇₃	I/O ₁₇₂	I/O ₁₆₇	I/O ₁₆₅	I/O ₁₆₂	C
D	I/O ₂₄	NC	NC	GND	NC	V _{CCO}	I/O ₁₃	GND	I/O ₃	NC	V _{CC}	I/O ₁₈₃	GND	I/O ₁₇₇	V _{CCO}	NC	GND	I/O ₁₆₄	TDI	I/O ₁₆₀	D
E	I/O ₂₇	I/O ₂₆	I/O ₂₅	NC													I/O ₁₆₃	I/O ₁₆₁	I/O ₁₅₉	I/O ₁₅₆	E
F	I/O ₃₀	TCK	I/O ₂₈	V _{CCO}													V _{CCO}	I/O ₁₅₈	NC	I/O ₁₅₄	F
G	I/O ₃₃	I/O ₃₂	I/O ₃₁	I/O ₂₉													I/O ₁₅₇	I/O ₁₅₅	I/O ₁₅₃	I/O ₁₅₂	G
H	I/O ₃₅	NC	I/O ₃₄	GND													GND	I/O ₁₅₁	I/O ₁₅₀	I/O ₁₄₉	H
J	I/O ₃₉	I/O ₃₈	I/O ₃₇	I/O ₃₆													I/O ₁₄₈	I/O ₁₄₇	I/O ₁₄₆	I/O ₁₄₅	J
K	I/O ₄₂	I/O ₄₀	I/O ₄₁	V _{CC}													I/O ₁₄₄	CLK ₃ /I ₄	NC	NC	K
L	I/O ₄₃	I/O ₄₄	I/O ₄₅	I/O ₄₆													V _{CC}	CLK ₂ /I ₃	I/O ₁₄₃	NC	L
M	I/O ₄₇	CLK ₀ /I ₀	CLK ₁ /I ₁	I/O ₄₈													I/O ₁₃₉	I/O ₁₄₀	I/O ₁₄₁	I/O ₁₄₂	M
N	I/O ₄₉	I/O ₅₀	I/O ₅₁	GND													GND	I/O ₁₃₆	I/O ₁₃₇	I/O ₁₃₈	N
P	I/O ₅₂	I/O ₅₃	I/O ₅₅	I/O ₅₈													I/O ₁₃₁	I/O ₁₃₃	I/O ₁₃₄	I/O ₁₃₅	P
R	I/O ₅₄	I/O ₅₆	I/O ₅₉	V _{CCO}													V _{CCO}	I/O ₁₃₀	NC	I/O ₁₃₂	R
T	I/O ₅₇	I/O ₆₀	I/O ₆₂	I/O ₆₅													I/O ₁₂₄	I/O ₁₂₇	I/O ₁₂₈	I/O ₁₂₉	T
U	I/O ₆₁	I/O ₆₃	I/O ₆₆	GND	I/O ₇₆	V _{CCO}	I/O ₈₂	GND	I/O ₉₁	V _{CC}	I/O ₉₈	I/O ₁₀₂	GND	I/O ₁₁₂	V _{CCO}	NC	GND	I/O ₁₂₃	I/O ₁₂₂	I/O ₁₂₆	U
V	I/O ₆₄	I/O ₆₇	I/O ₆₉	I/O ₇₅	I/O ₇₈	I/O ₈₁	I/O ₈₅	I/O ₈₈	I/O ₉₂	I ₂	I/O ₉₇	I/O ₁₀₁	I/O ₁₀₅	I/O ₁₀₉	I/O ₁₁₃	TDO	I/O ₁₁₄	I/O ₁₁₇	I/O ₁₂₁	I/O ₁₂₅	V
W	I/O ₆₈	I/O ₇₀	I/O ₇₂	I/O ₇₄	I/O ₇₉	I/O ₈₃	I/O ₈₆	I/O ₈₉	I/O ₉₃	I/O ₉₅	I/O ₉₆	I/O ₁₀₀	I/O ₁₀₄	I/O ₁₀₇	I/O ₁₁₀	NC	NC	I/O ₁₁₅	I/O ₁₁₈	I/O ₁₂₀	W
Y	I/O ₇₁	I/O ₇₃	I/O ₇₇	TMS	I/O ₈₀	I/O ₈₄	I/O ₈₇	I/O ₉₀	I/O ₉₄	NC	NC	I/O ₉₉	I/O ₁₀₃	I/O ₁₀₆	I/O ₁₀₈	I/O ₁₁₁	NC	NC	I/O ₁₁₆	I/O ₁₁₉	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

*NOTE: Center pins must be connected to GND to aid thermal dissipation.



Pin Configurations

352-ball BGA

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
GND	GND	I/O ₁₉	I/O ₁₅	I/O ₁₃	I/O ₃₄	I/O ₃₁	I/O ₂₈	I/O ₂₅	I/O ₁₀	I/O ₇	I/O ₄	I/O ₁	I/O ₂₆₃	I/O ₂₆₀	I/O ₂₅₇	I/O ₂₅₄	I/O ₂₃₉	I/O ₂₃₇	I/O ₂₃₂	I/O ₂₂₉	I/O ₂₅₀	I/O ₂₄₈	I/O ₂₄₄	GND	GND	A
GND	NC	I/O ₁₈	I/O ₁₇	I/O ₁₄	I/O ₃₅	I/O ₃₂	I/O ₂₉	I/O ₂₆	I/O ₁₁	I/O ₈	I/O ₅	I/O ₂	V _{CC}	I/O ₂₆₁	I/O ₂₅₈	I/O ₂₅₅	I/O ₂₅₂	I/O ₂₃₄	I/O ₂₃₁	I/O ₂₂₈	I/O ₂₄₉	I/O ₂₄₆	I/O ₂₄₅	I/O ₂₄₀	GND	B
I/O ₂₃	I/O ₃₈	I/O ₃₇	I/O ₁₆	I/O ₁₂	I/O ₃₃	I/O ₃₀	I/O ₂₇	I/O ₂₄	I/O ₉	I/O ₆	I/O ₃	I/O ₀	I/O ₂₆₂	I/O ₂₅₉	I/O ₂₅₆	I/O ₂₅₃	I/O ₂₃₈	I/O ₂₃₅	I/O ₂₃₃	I/O ₂₃₀	I/O ₂₅₁	I/O ₂₄₇	I/O ₂₂₅	I/O ₂₂₄	I/O ₂₂₇	C
I/O ₃₉	I/O ₄₀	I/O ₃₆	NC	NC	I/O ₂₁	I/O ₂₀	V _{CC}	V _{CC}	NC	GND	GND	V _{CC}	V _{CC}	GND	GND	NC	V _{CC}	V _{CC}	I/O ₂₃₆	I/O ₂₄₃	NC	NC	I/O ₂₂₆	I/O ₂₂₂	I/O ₂₂₃	D
I/O ₄₂	TCK	I/O ₄₁	NC																			NC	TDI	I/O ₂₂₁	I/O ₂₂₀	E
I/O ₄₅	I/O ₄₄	I/O ₄₃	I/O ₂₂																			I/O ₂₄₂	I/O ₂₁₉	I/O ₂₁₈	I/O ₂₁₇	F
I/O ₄₈	I/O ₄₇	I/O ₄₆	I/O ₆₃																			I/O ₂₄₁	I/O ₂₁₆	I/O ₂₁₅	I/O ₂₁₄	G
I/O ₄₉	I/O ₅₀	I/O ₅₁	V _{CC}																			V _{CC}	I/O ₂₁₁	I/O ₂₁₂	I/O ₂₁₃	H
I/O ₅₂	I/O ₅₃	I/O ₅₄	V _{CC}																			V _{CC}	I/O ₂₀₈	I/O ₂₀₉	I/O ₂₁₀	J
I/O ₅₅	I/O ₅₆	I/O ₅₇	NC																			NC	I/O ₂₀₅	I/O ₂₀₆	I/O ₂₀₇	K
I/O	I/O ₅₉	I/O ₅₈	GND																			GND	I/O ₂₀₄	I4	I/O ₁₉₇	L
I/O ₆₁	I/O ₆₀	I1	GND																			GND	I3	I/O ₂₀₃	I/O ₂₀₂	M
I/O ₆₄	V _{CC}	I/O ₆₂	V _{CC}																			V _{CC}	I/O ₂₀₁	I/O ₂₀₀	I/O ₁₉₉	N
I/O ₆₅	I/O ₆₆	I/O ₆₇	V _{CC}																			V _{CC}	I/O ₁₉₆	V _{CC}	I/O ₁₉₈	P
I/O ₆₈	I/O ₆₉	I/O ₇₀	GND																			GND	I/O ₁₉₃	I/O ₁₉₄	I/O ₁₉₅	R
I/O ₇₁	I/O ₈₄	I/O ₈₅	GND																			GND	I/O ₁₇₈	I/O ₁₇₉	I/O ₁₉₂	T
I/O ₈₈	I/O ₈₇	I/O ₈₆	NC																			NC	I/O ₁₇₇	I/O ₁₇₆	I/O ₁₇₅	U
I/O ₉₁	I/O ₉₀	I/O ₈₉	V _{CC}																			V _{CC}	I/O ₁₇₄	I/O ₁₇₃	I/O ₁₇₂	V
I/O ₉₄	I/O ₉₃	I/O ₉₂	V _{CC}																			V _{CC}	I/O ₁₇₁	I/O ₁₇₀	I/O ₁₆₉	W
I/O ₉₅	I/O ₇₂	I/O ₇₃	I/O ₁₁₀																			I/O ₁₅₃	I/O ₁₉₀	I/O ₁₉₁	I/O ₁₆₈	Y
I/O ₇₄	I/O ₇₅	I/O ₇₆	I/O ₁₁₁																			I/O ₁₅₂	I/O ₁₈₇	I/O ₁₈₈	I/O ₁₈₉	AA
I/O ₇₇	I/O ₇₈	I/O ₇₉	N/C																			NC	I/O ₁₈₄	I/O ₁₈₅	I/O ₁₈₆	AB
I/O ₈₁	I/O ₈₀	I/O ₁₀₈	N/C	NC	I/O ₁₁₂	I/O ₁₁₃	V _{CC}	V _{CC}	NC	GND	GND	V _{CC}	V _{CC}	GND	GND	NC	V _{CC}	V _{CC}	I/O ₁₅₀	I/O ₁₅₁	NC	NC	I/O ₁₅₅	I/O ₁₈₃	I/O ₁₈₂	AC
I/O ₁₀₉	I/O ₈₂	I/O ₈₃	I/O ₁₁₇	I/O ₉₇	I/O ₁₀₀	I/O ₁₀₂	I/O ₁₀₅	I/O ₁₂₀	I/O ₁₂₃	I/O ₁₂₆	I/O ₁₂₉	I2	I/O ₁₃₃	I/O ₁₃₆	I/O ₁₃₉	I/O ₁₄₂	I/O ₁₅₇	I/O ₁₅₉	I/O ₁₆₁	I/O ₁₆₃	I/O ₁₆₆	I/O ₁₄₆	I/O ₁₈₀	I/O ₁₈₁	I/O ₁₅₄	AD
GND	NC	I/O ₁₁₅	I/O ₁₁₆	I/O ₁₁₉	I/O ₉₈	I/O ₁₀₁	I/O ₁₀₃	I/O ₁₀₆	I/O ₁₂₁	I/O ₁₂₄	I/O ₁₂₇	V _{CC}	I/O ₁₃₀	I/O ₁₃₄	I/O ₁₃₇	I/O ₁₄₀	I/O ₁₄₃	I/O ₁₆₀	I/O ₁₆₂	I/O ₁₆₅	I/O ₁₄₄	I/O ₁₄₇	I/O ₁₄₈	NC	GND	AE
GND	GND	I/O ₁₁₄	I/O ₁₁₈	I/O ₉₆	I/O ₉₉	TMS	I/O ₁₀₄	I/O ₁₀₇	I/O ₁₂₂	I/O ₁₂₅	I/O ₁₂₈	I/O ₁₃₁	I/O ₁₃₂	I/O ₁₃₅	I/O ₁₃₈	I/O ₁₄₁	I/O ₁₅₆	I/O ₁₅₈	TDO	I/O ₁₆₄	I/O ₁₆₇	I/O ₁₄₅	I/O ₁₄₉	GND	GND	AF
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied -55°C to +125°C

Supply Voltage to Ground Potential -0.5V to +4.6V

DC Voltage Applied to Outputs

in High Z State -0.5V to +4.6V

DC Input Voltage -0.5V to +4.6V

DC Program Voltage 3.0V to 3.6V

Current into Outputs 8 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range^[2]

Range	Ambient Temperature ^[2]	Junction Temperature	V _{CC}
Commercial	0°C to +70°C	0°C to +90°C	3.3V ± 0.3V
Industrial	-40°C to +85°C	-40°C to +125°C	3.3V ± 0.3V
Military ^[3]	-55°C to +125°C	-55°C to +130°C	3.3V ± 0.3V

Shaded areas contain advanced information.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min. I _{OH} = -4 mA (Com'l) ^[4] I _{OH} = -3 mA (Mil) ^[4]	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min. I _{OL} = 8 mA (Com'l) ^[4] I _{OL} = 6 mA (Mil) ^[4]		0.5	V
V _{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH voltage for all inputs ^[5]	2.0	V _{CCmax}	V
V _{IL}	Input LOW Voltage	Guaranteed Input Logical LOW voltage for all inputs ^[5]	-0.5	0.8	V
I _{IX}	Input Load Current	V _I = GND or V _{CC}	-10	10	μA
I _{OZ}	Output Leakage Current	V _O = GND or V _{CC} , Output Disabled	-50	50	μA
I _{OS}	Output Short Circuit Current ^[6, 7]	V _{CC} = Max., V _{OUT} = 0.5V	-30	-160	mA
I _{BHL}	Input Bus Hold LOW Sustaining Current	V _{CC} = Min., V _{IL} = 0.8V	+75		μA
I _{BHH}	Input Bus Hold HIGH Sustaining Current	V _{CC} = Min., V _{IH} = 2.0V	-75		μA
I _{BHLO}	Input Bus Hold LOW Overdrive Current	V _{CC} = Max.		+500	μA
I _{BHHO}	Input Bus Hold HIGH Overdrive Current	V _{CC} = Max.		-500	μA

Inductance^[7]

Parameter	Description	Test Conditions	208-lead PQFP	Unit
L	Maximum Pin Inductance	V _{IN} = 3.3V at f = 1 MHz	11	nH

Notes:

- Normal Programming Conditions apply across Ambient Temperature Range for specified programming methods. For more information on programming the Ultra37000 family devices see the Ultra37000 family data sheet.
- T_A is the "instant on" case temperature.
- I_{OH} = -2 mA, I_{OL} = 2 mA for TDO.
- These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
- Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
- Tested initially and after any design or process changes that may affect these parameters.

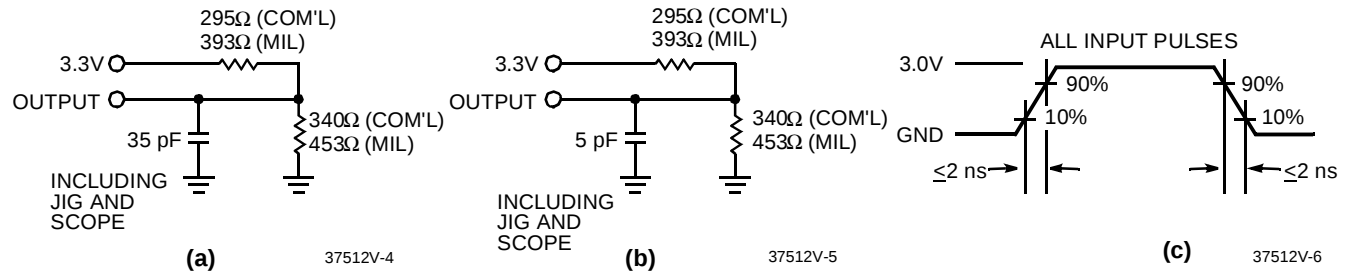
Capacitance^[7]

Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	$V_{IN} = 3.3V$ at $f = 1$ MHz at $T_A = 25^\circ C$	8	pF
C_{CLK}	Clock Signal Capacitance	$V_{IN} = 3.3V$ at $f = 1$ MHz at $T_A = 25^\circ C$	12	pF

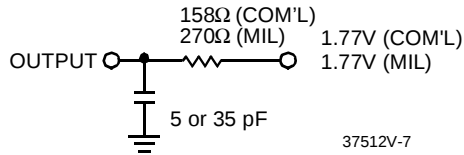
Endurance Characteristics^[7]

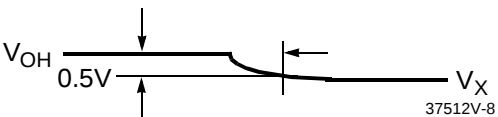
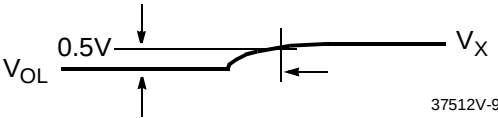
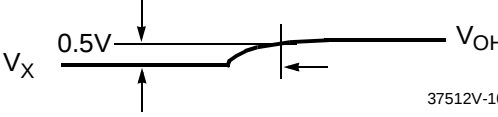
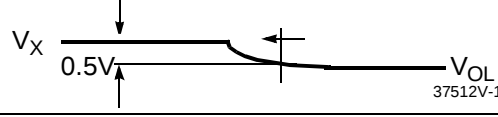
Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions ^[2]	1,000	10,000	Cycles

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Parameter ^[8]	V_X	Output Waveform–Measurement Level
$t_{ER(-)}$	1.5V	 37512V-8
$t_{ER(+)}$	2.6V	 37512V-9
$t_{EA(+)}$	1.5V	 37512V-10
$t_{EA(-)}$	V_{the}	 37512V-11

(d) Test Waveforms

Note:

8. t_{ER} measured with 5-pF AC Test Load and t_{EA} measured with 35-pF AC Test Load.

Switching Characteristics Over the Operating Range^[9]

Parameter	Description	37512V-83		37512V-66		Unit
		Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters						
t _{PD} ^[10, 11]	Input to Combinatorial Output		15		20	ns
t _{PDL} ^[10, 11]	Input to Output Through Transparent Input or Out-put Latch		18		22	ns
t _{PDLL} ^[10, 11]	Input to Output Through Transparent Input and Out-put Latches		19		24	ns
t _{EA} ^[10, 11]	Input to Output Enable		19		24	ns
t _{ER} ^[10]	Input to Output Disable		19		24	ns
Input Register Parameters						
t _{WL}	Clock or Latch Enable Input LOW Time ^[7]	4		5		ns
t _{WH}	Clock or Latch Enable Input HIGH Time ^[7]	4		5		ns
t _{IS}	Input Register or Latch Set-Up Time	3		4		ns
t _{IH}	Input Register or Latch Hold Time	3		4		ns
t _{ICO} ^[10, 11]	Input Register Clock or Latch Enable to Combina-torial Output		19		24	ns
t _{ICOL} ^[10, 11]	Input Register Clock or Latch Enable to Output Through Transparent Output Latch		21		26	ns
Synchronous Clocking Parameters						
t _{CO} ^[11]	Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable to Output		8		10	ns
t _S ^[10]	Set-Up Time from Input to Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable	8		10		ns
t _H	Register or Latch Data Hold Time	0		0		ns
t _{CO2} ^[10, 11]	Output Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable to Combinatorial Output De-lay (Through Logic Array)		19		24	ns
t _{SCS} ^[10]	Output Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable to Output Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable (Through Logic Array)	12		15		ns
t _{SL} ^[10]	Set-Up Time from Input Through Transparent Latch to Output Register Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable	15		15		ns
t _{HL}	Hold Time for Input Through Transparent Latch from Output Register Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable	0		0		ns
Product Term Clocking Parameters						
t _{COPT} ^[10, 11]	Product Term Clock or Latch Enable (PTCLK) to Output		15		20	ns
t _{SPT}	Set-Up Time from Input to Product Term Clock or Latch Enable (PTCLK)	4.5		6		ns
t _{HPT}	Register or Latch Data Hold Time	4.5		6		ns

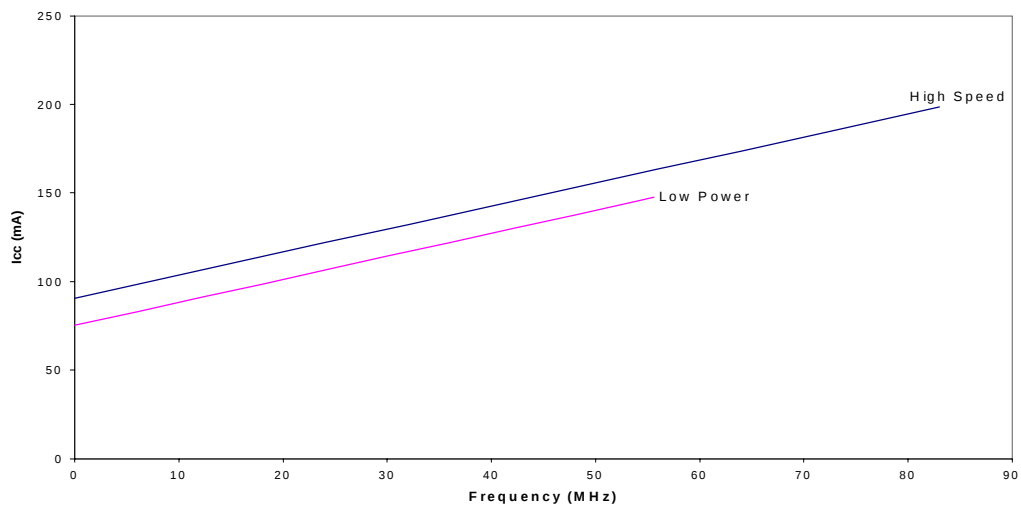
Notes:

9. All AC parameters are measured with 16 outputs switching and 35-pF AC Test Load.
10. Logic Blocks operating in low power mode, add t_{LP} to this spec.
11. Outputs using Slow Output Slew Rate, add t_{SLEW} to this spec.

Switching Characteristics Over the Operating Range^[9] (continued)

Parameter	Description	37512V-83		37512V-66		Unit
		Min.	Max.	Min.	Max.	
$t_{ISPT}^{[10]}$	Set-Up Time for Buried Register Used as an Input Register from Input to Product Term Clock or Latch Enable (PTCLK)		-2		-2	ns
t_{IHPT}	Buried Register Used as an Input Register or Latch Data Hold Time		14		19	ns
$t_{CO2PT}^{[10, 11]}$	Product Term Clock or Latch Enable (PTCLK) to Output Delay (Through Logic Array)		24		30	ns
Pipelined Mode Parameters						
$t_{ICS}^{[10]}$	Input Register Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) to Output Register Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃)	12		15		ns
Operating Frequency Parameters						
f_{MAX1}	Maximum Frequency with Internal Feedback (Least of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$) ^[7]	83		66		MHz
f_{MAX2}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$)	125		100		MHz
f_{MAX3}	Maximum Frequency with External Feedback (Lesser of $1/(t_{CO} + t_S)$ or $1/(t_{WL} + t_{WH})$)	67.5		50		MHz
f_{MAX4}	Maximum Frequency in Pipelined Mode (Least of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$)	66.6		66.7		MHz
Reset/Preset Parameters						
t_{RW}	Asynchronous Reset Width ^[7]	15		20		ns
$t_{RR}^{[10]}$	Asynchronous Reset Recovery Time ^[7]	17		22		ns
$t_{RO}^{[10, 11]}$	Asynchronous Reset to Output		21		26	ns
t_{PW}	Asynchronous Preset Width ^[7]	15		20		ns
$t_{PR}^{[10]}$	Asynchronous Preset Recovery Time ^[7]	17		22		ns
$t_{PO}^{[10, 11]}$	Asynchronous Preset to Output		21		26	ns
User Option Parameters						
t_{LP}	Low Power Adder		4		4	ns
t_{SLEW}	Slow Output Slew Rate Adder		2		2	ns
JTAG Timing Parameters						
t_S JTAG	Set-Up Time from TDI and TMS to TCK	0		0		ns
t_H JTAG	Hold Time on TDI and TMS	20		20		ns
t_{CO} JTAG	Falling Edge of TCK to TDO		20		20	ns
f_{JTAG}	Maximum JTAG Tap Controller Frequency		20		20	MHz

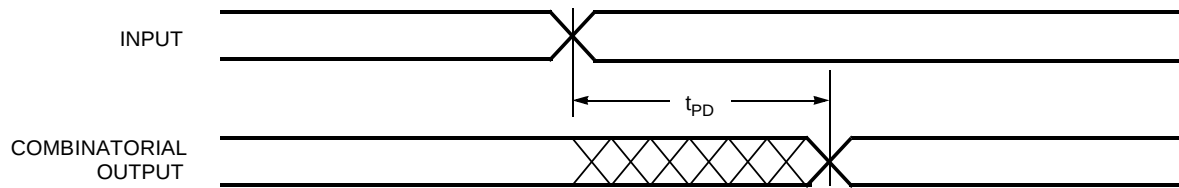
Typical I_{CC} Characteristics



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 3.3V$, $T_A = \text{Room Temperature}$

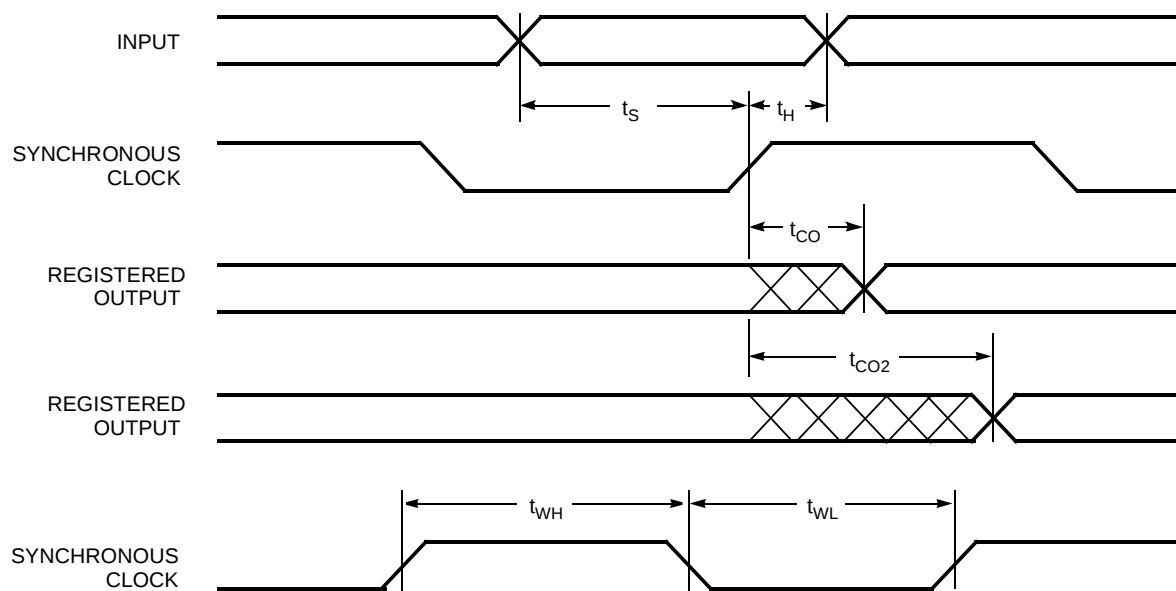
Switching Waveforms

Combinatorial Output



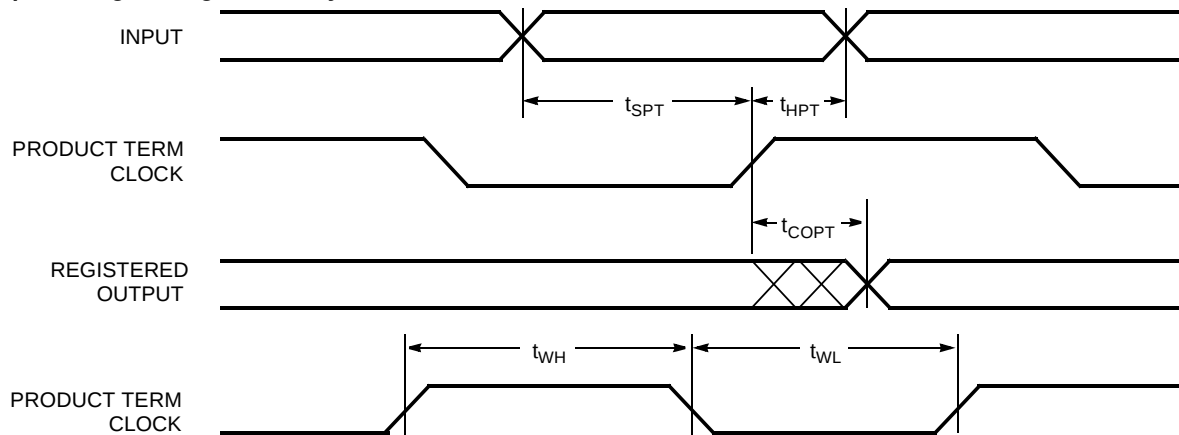
37512V-12

Registered Output with Synchronous Clocking



37512V-13

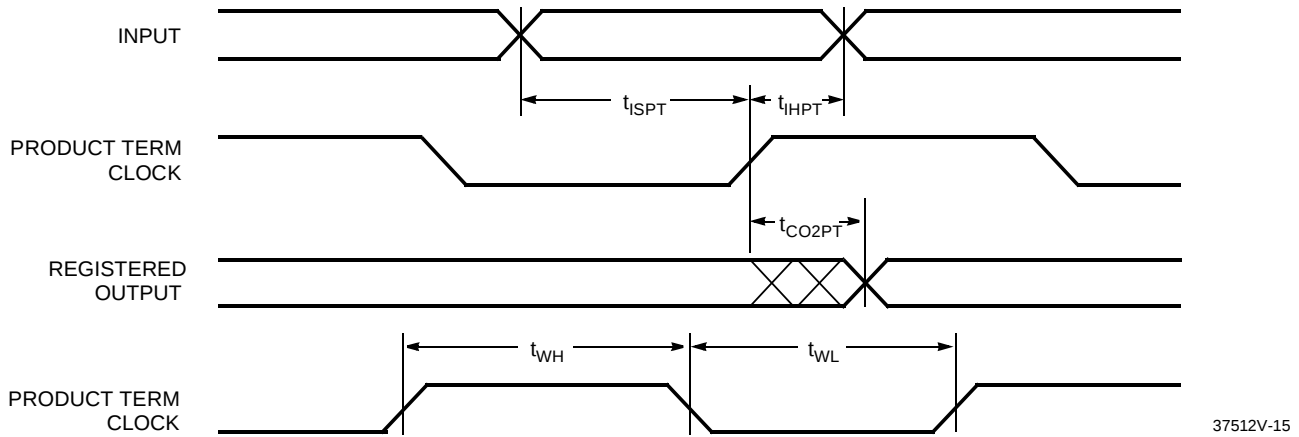
Registered Output with Product Term Clocking Input Going Through the Array



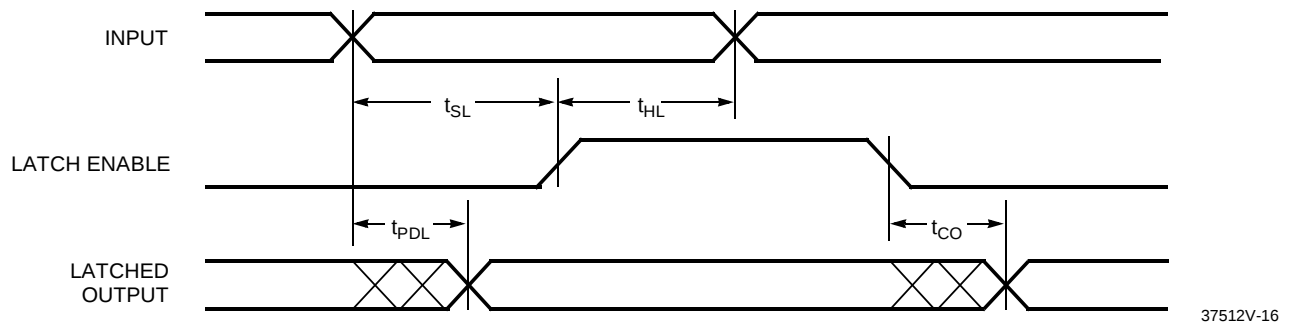
37512V-14

Switching Waveforms (continued)

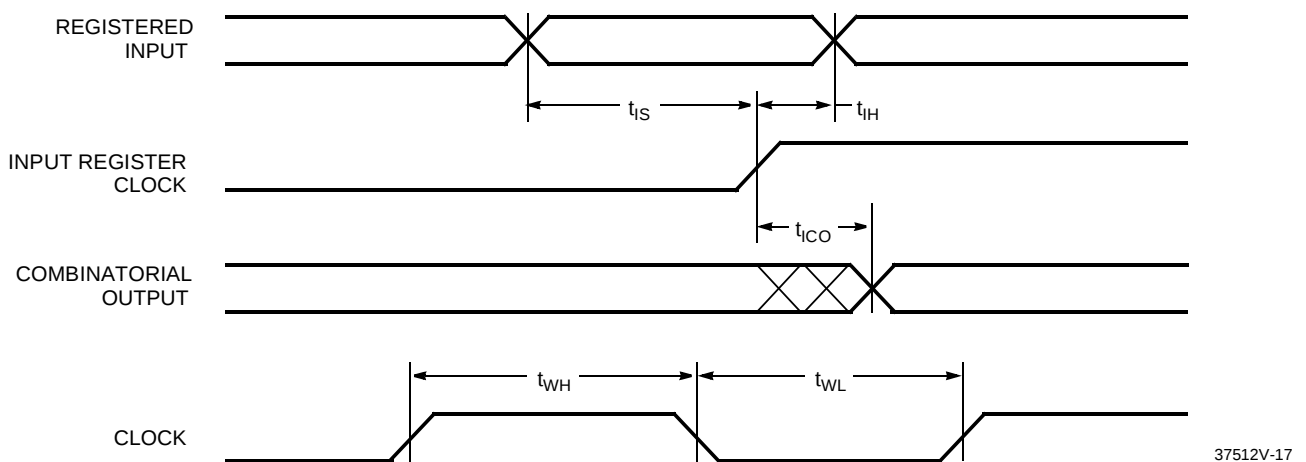
Registered Output with Product Term Clocking Input Coming From Adjacent Buried Register



Latched Output

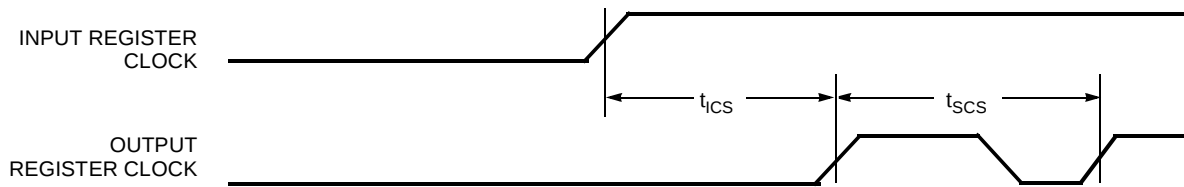


Registered Input



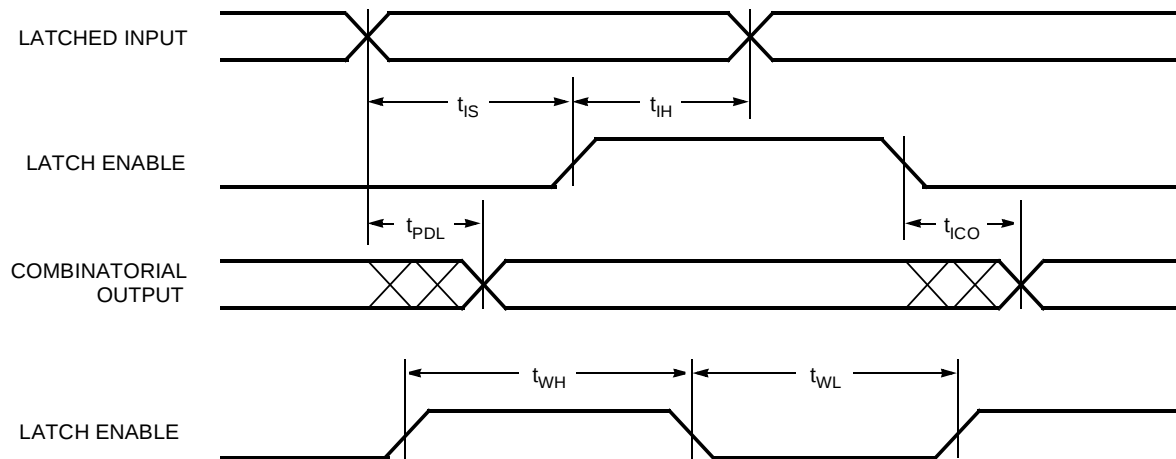
Switching Waveforms (continued)

Clock to Clock



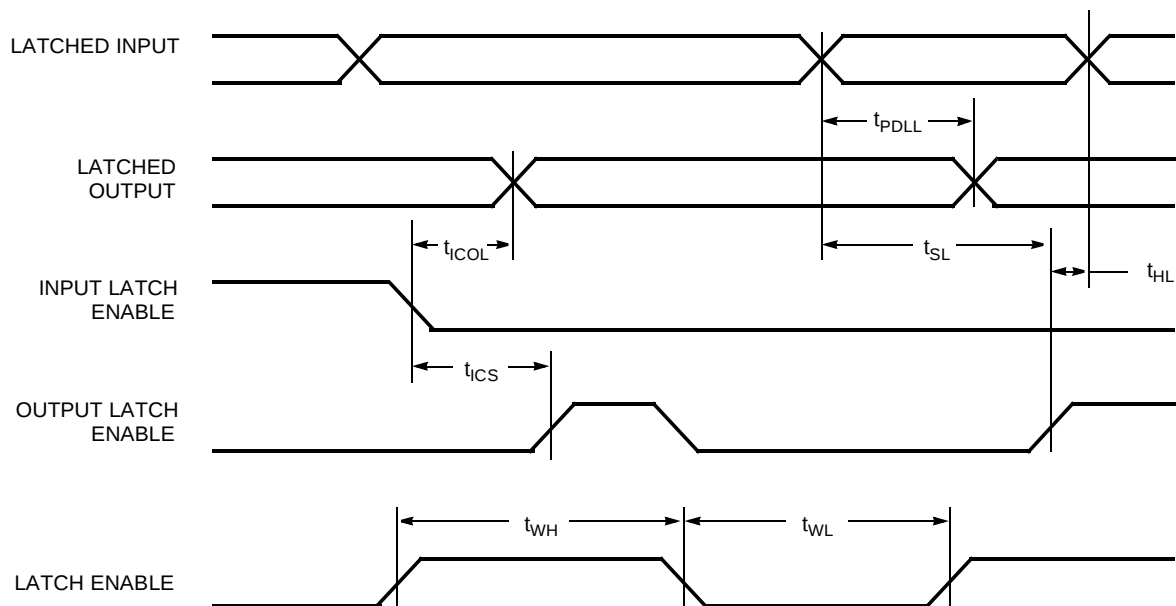
37512V-18

Latched Input



37512V-19

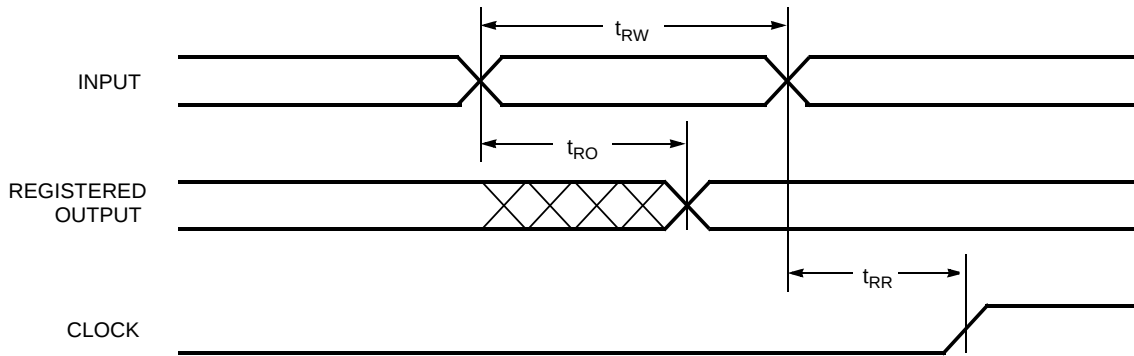
Latched Input and Output



37512V-20

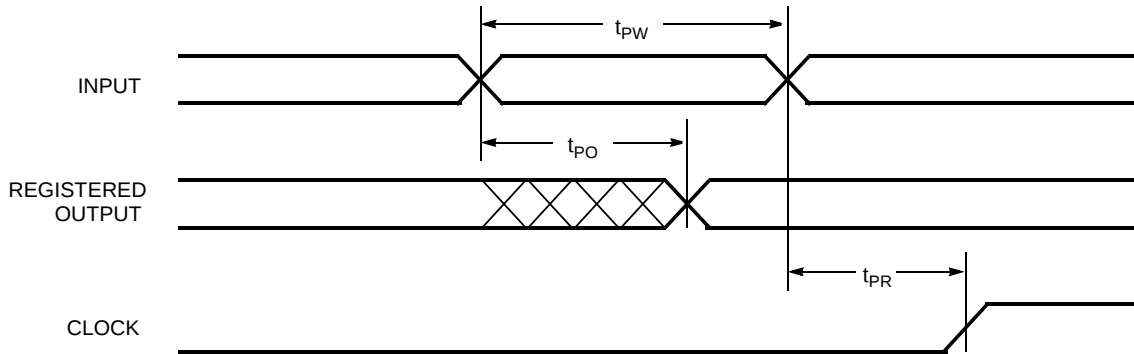
Switching Waveforms (continued)

Asynchronous Reset



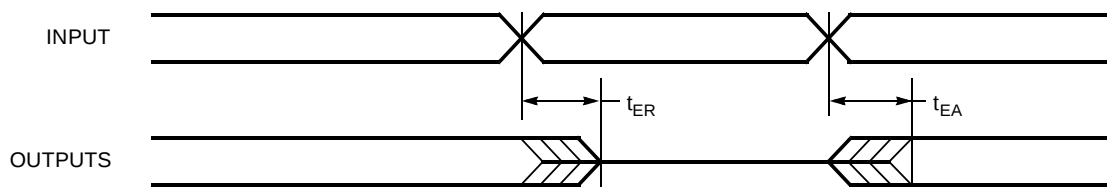
37512V-21

Asynchronous Preset



37512V-22

Output Enable/Disable



37512V-23

**Ordering Information**

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
83	CY37512VP208-83NC	N208	208-Pin Plastic Quad Flatpack	Commercial
	CY37512VP256-83BGC	BG256	256-Pin Ball Grid Array	
	CY37512VP352-83BGC	BG352	352-Pin Ball Grid Array	
66	CY37512VP208-66NC	N208	208-Pin Plastic Quad Flatpack	Commercial
	CY37512VP256-66BGC	BG256	256-Pin Ball Grid Array	
	CY37512VP352-66BGC	BG352	352-Pin Ball Grid Array	
	CY37512VP208-66NI	N208	208-Pin Plastic Quad Flatpack	Industrial
	CY37512VP256-66BGI	BG256	256-Pin Ball Grid Array	
	CY37512VP352-66BGI	BG352	352-Pin Ball Grid Array	
	CY37512VP208-66UMB	U208	208-Pin Ceramic Quad Flatpack	Military

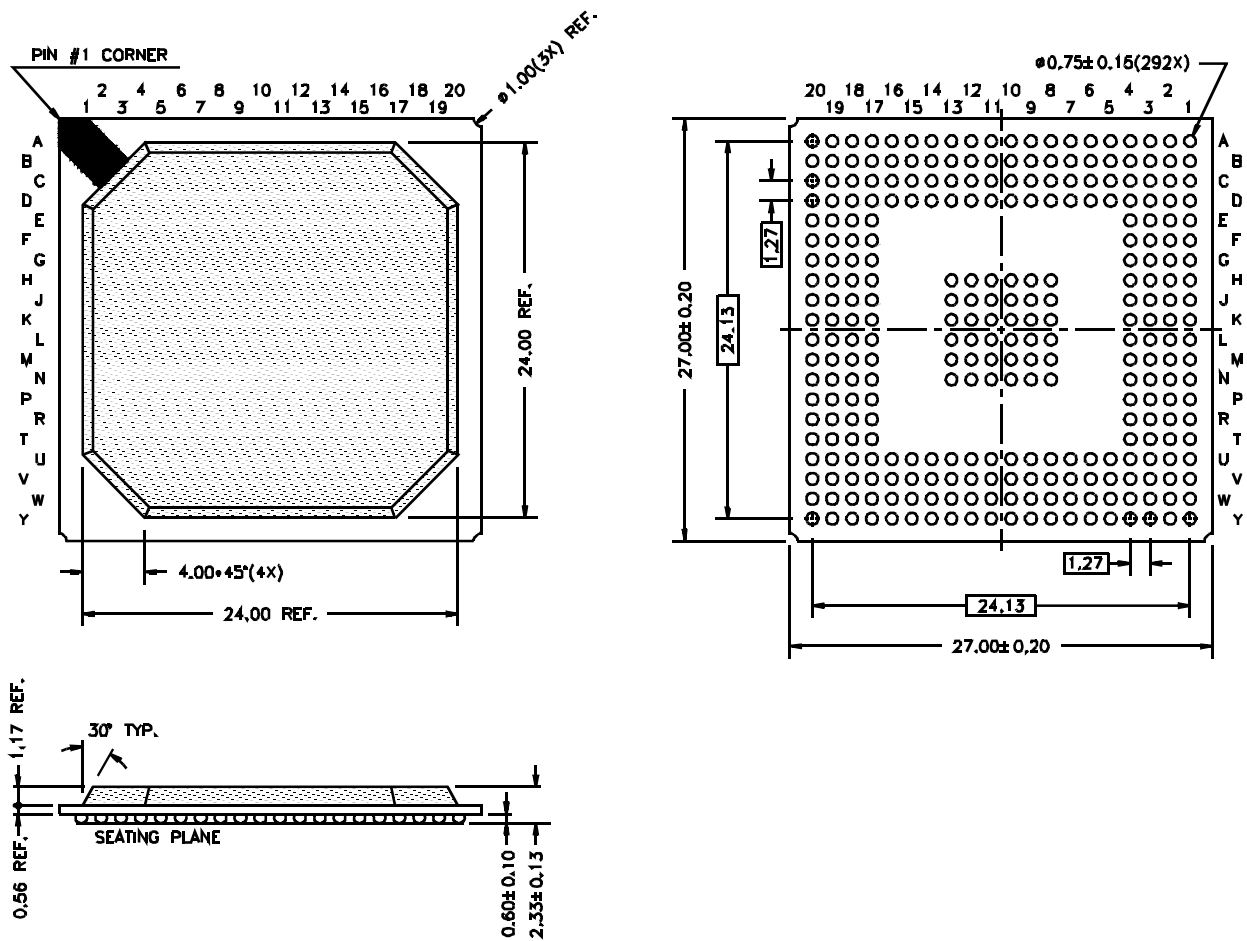
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Document #: 38-00719-A

Package Diagrams

256-Lead Ball Grid Array (27 x 27 x 2.33 mm) BG256



Package Diagrams (continued)

208-Lead Plastic Quad Flatpack N208

