

12-BIT, 21-MSPS, ULTRALOW-POWER CCD SIGNAL PROCESSOR

FEATURES

- 12-Bit, 21-MSPS, Analog-to-Digital Converter
- Low Power: 70 mW Minimum
Power-Down Mode: 4 mW
- Low Input-Referred Noise: 75-dB
SNR Typical at 0-dB Gain
- Novel Optical-Black (OB) Calibration
- Low-Aperture Delay
- Single 3-V Supply Operation
- DNL: $\leq \pm 0.5$ LSB and
INL: $\leq \pm 1.5$ LSB Typical at 0-dB Gain
- Programmable-Gain Range: 0 dB to 36 dB,
Gain Resolution of 0.05 dB/Step
- 48-Pin TQFP Package

APPLICATIONS

- Digital Still Camera
- Digital Video Camera

DESCRIPTION

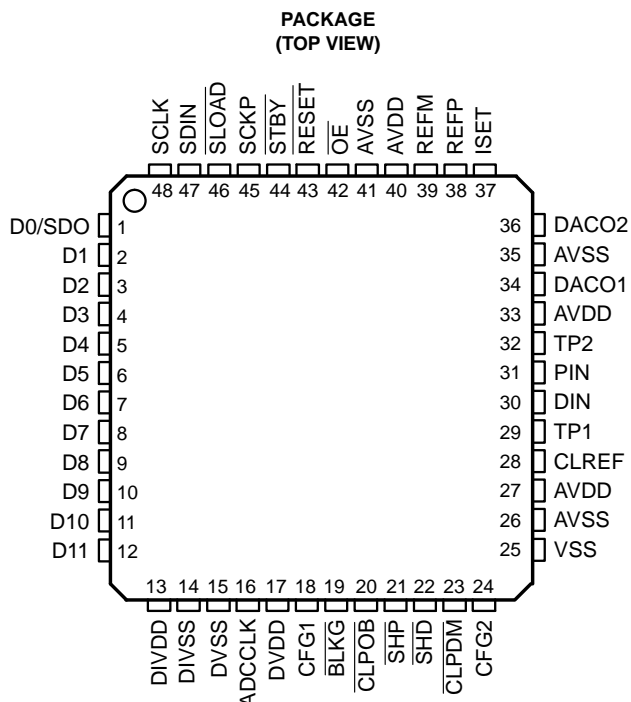
The VSP1221 is a highly-integrated mixed-signal IC used for signal conditioning and analog-to-digital conversion at the output of a CCD array. The IC has a correlated double sampler (CDS) and an analog programmable-gain amplifier (PGA) stage followed by an analog-to-digital converter (ADC) and a digital PGA stage. The CDS is used to sample the CCD signal and is followed by the analog PGA stage. The ADC is a 12-bit, 21-MSPS pipelined ADC. The digital PGA provides further amplification.

Additionally, there is an offset calibration loop for optical-black correction. The optical-black reference level is user-programmable. The chip also has two 8-bit digital-to-analog converters (DAC) for external analog settings.

The chip has a serial port for configuring internal control registers.

The VSP1221 is available in a 48-pin TQFP package and operates from a single 3-V power supply.

PIN ASSIGNMENTS



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
VSP1221PFB	Active	Production	TQFP (PFB) 48	250 JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	VSP1221
VSP1221PFB.B	Active	Production	TQFP (PFB) 48	250 JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	VSP1221

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TRAY

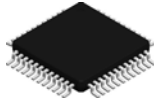


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (μm)	P1 (mm)	CL (mm)	CW (mm)
VSP1221PFB	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
VSP1221PFB.B	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

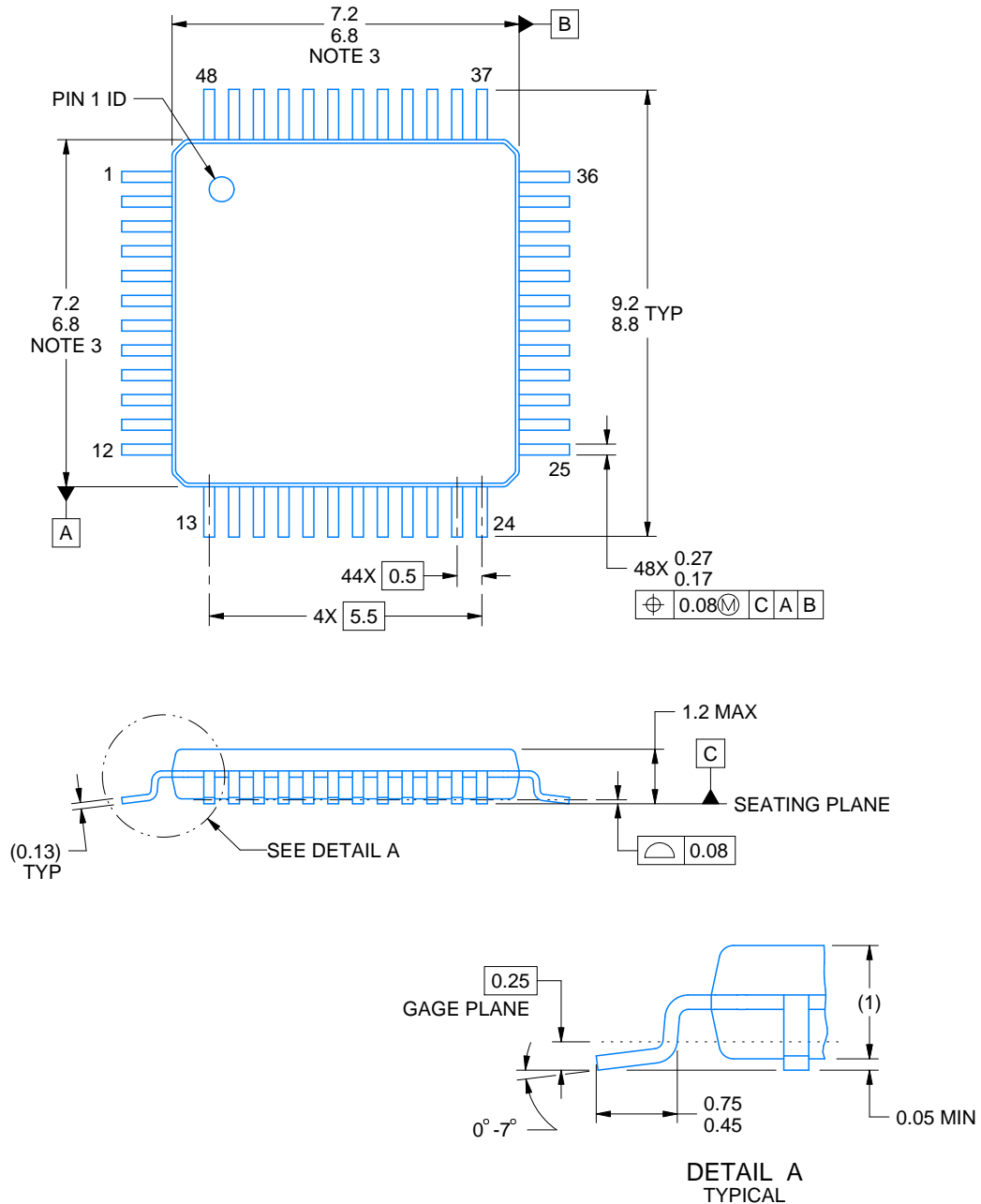
PFB0048A



PACKAGE OUTLINE

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



4215157/A 03/2024

NOTES:

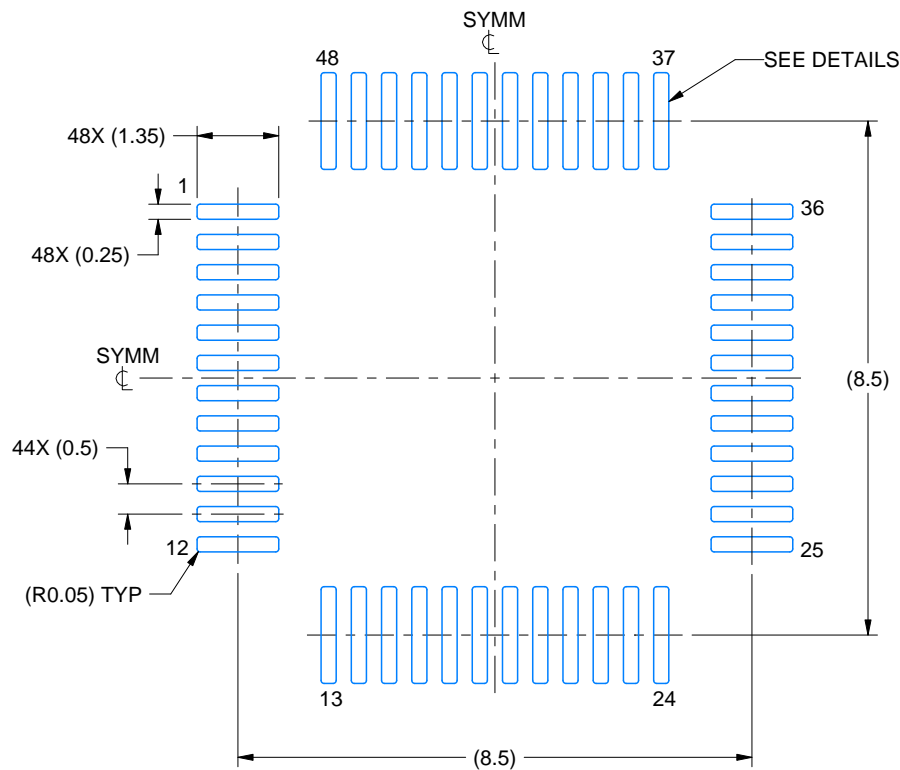
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.

EXAMPLE BOARD LAYOUT

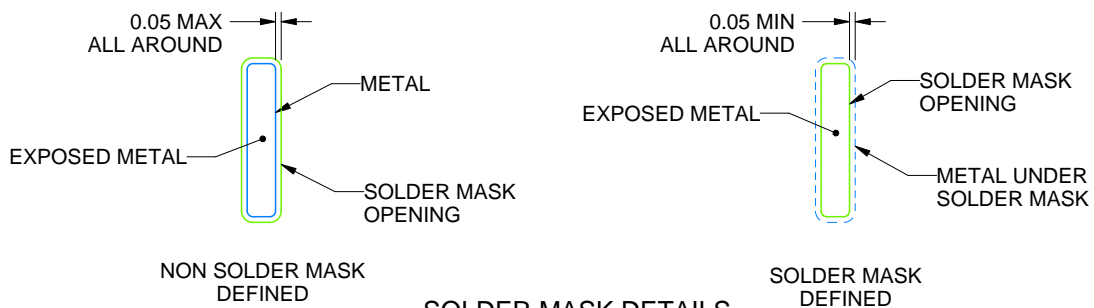
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TQFP - 1.2 mm max height

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LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



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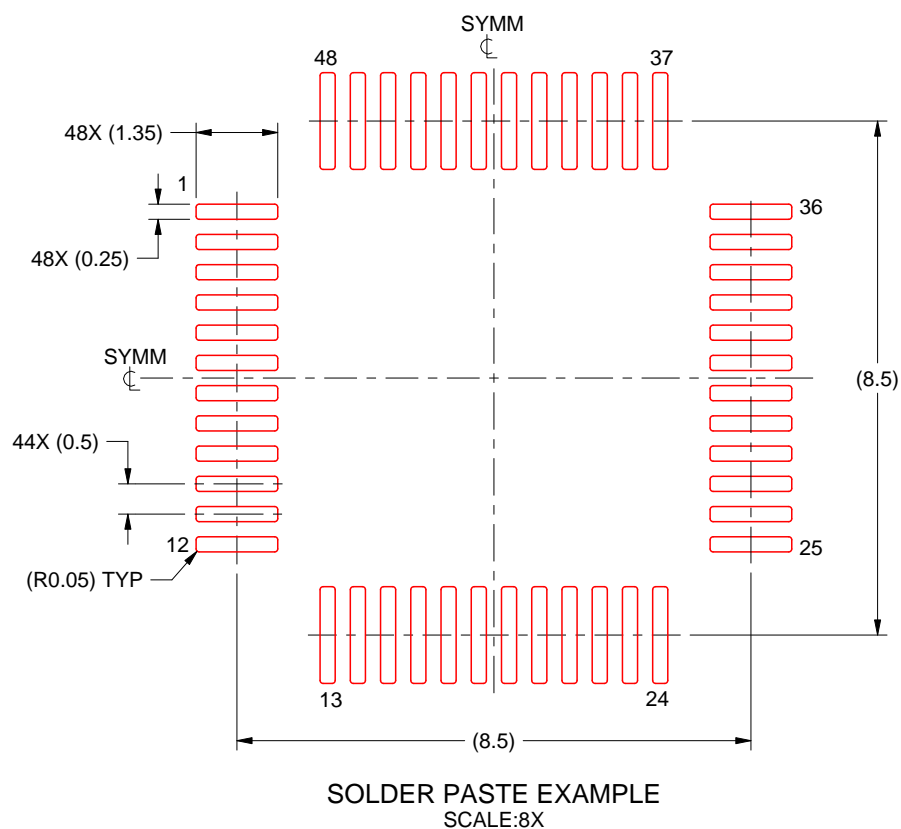
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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TQFP - 1.2 mm max height

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4215157/A 03/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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