SERIAL REAL-TIME CLOCK

IDT5P90005

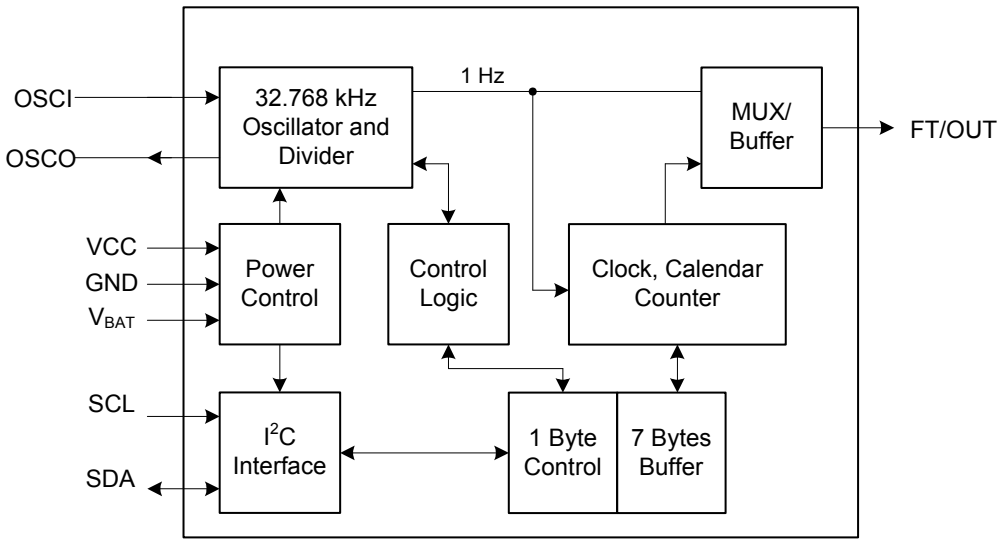
Description

The IDT5P90005 is a serial real-time clock (RTC) device that consumes ultra-low power and provides a full binary-coded decimal (BCD) clock/calendar. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. The end of the month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year. Access to the clock/calendar registers is provided by an I^2C interface capable of operating in fast I^2C mode. Built-in Power-sense circuitry detects power failures and automatically switches to the backup supply, maintaining time and date operation.

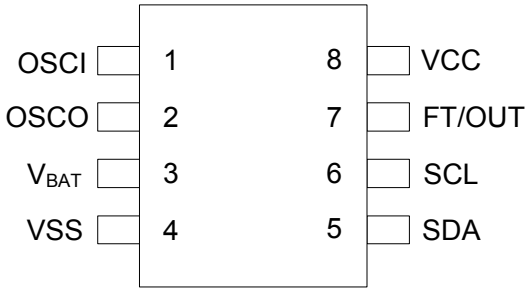
Features

- Packaged in 8-pin SOIC
- Counters for seconds, minutes, hours, days, date, months, years, and century
- 32 kHz crystal oscillator integrating load capacitance (12.5 pF) providing exceptional oscillator stability and high crystal series resistance operation
- Serial interface supports I2C bus (100 or 400 kHz protocol)
- Ultra low battery supply current of 0.8 µA (typ at 3 V)
- 2.0 to 5.5 V clock operating voltage
- Automatic switch over and deselect circuitry
- Automatic leap year compensation
- Operating temperature of -40 to +85°C

Block Diagram



Pin Assignment



8-Pin (150 mil) SOIC

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	OSCI	Input	Oscillator input.
2	OSCO	Output	Oscillator output.
3	V_{BAT}	Power	Battery supply voltage.
4	VSS	Power	Connect to ground.
5	SDA	I/O	Serial data address input/output.
6	SCL	Input	Serial clock.
7	FT/OUT	Output	Frequency test/output driver (open drain).
8	VCC	Power	Supply voltage.

Device Operation

The IDT5P90005 clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct slave address (D0h). The 8 bytes contained in the device can then be accessed sequentially in the following order:

1st byte: seconds register

2nd byte: minutes register

3rd byte: century/hours register

4th byte: day register

5th byte: date register

6th byte: month register

7th byte: years register

8th byte: control register

The IDT5P90005 clock continually monitors VCC for an out-of-tolerance condition. Should VCC fall below VSO, the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time, to prevent erroneous data from being written to the device from an out-of-tolerance system. When VCC falls below VSO, the device automatically switches over to the battery and powers down into an ultra low current mode of operation to conserve battery life. Upon power-up, the device switches from battery to VCC at VSO and recognizes inputs.

I²C Serial Data Bus

The IDT5P90005 supports the I²C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The IDT5P90005 operates as a slave on the I²C bus. Within the bus specifications, a standard mode (100 kHz maximum clock rate) and a fast mode (400 kHz maximum clock rate) are defined. The IDT5P90005 works in both modes. Connections to the bus are made via the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (see the “Data Transfer on I²C Serial Bus” figure):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

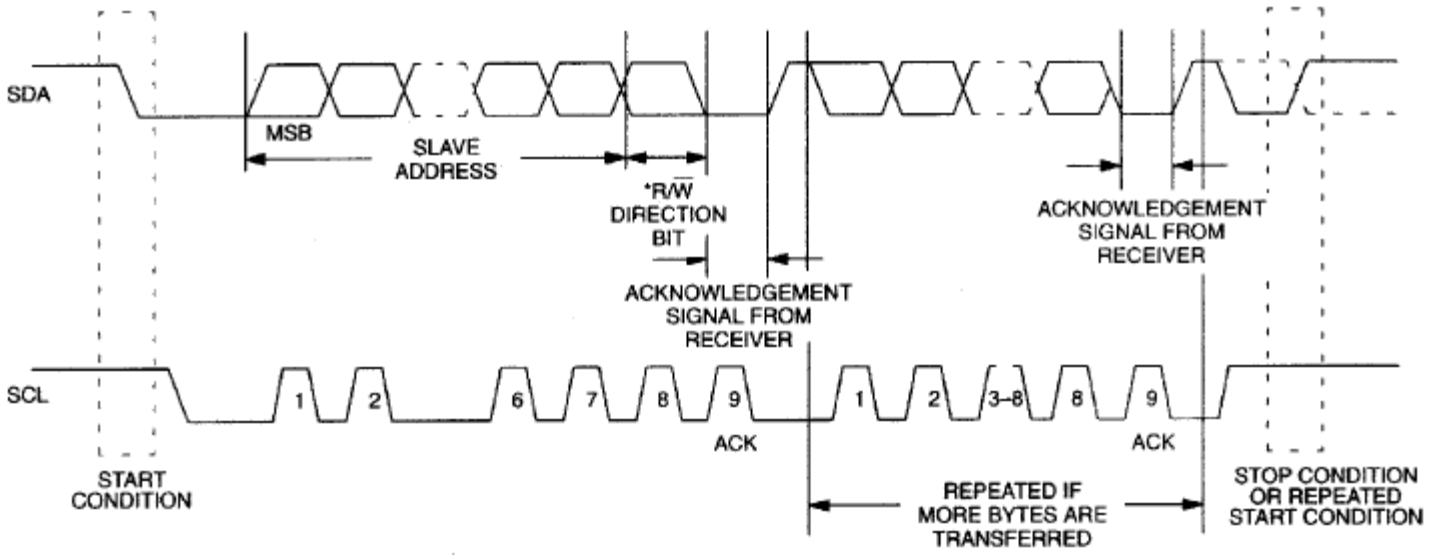
Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Data Transfer on I²C Serial Bus



Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

1) **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.

2) **Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. This is followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

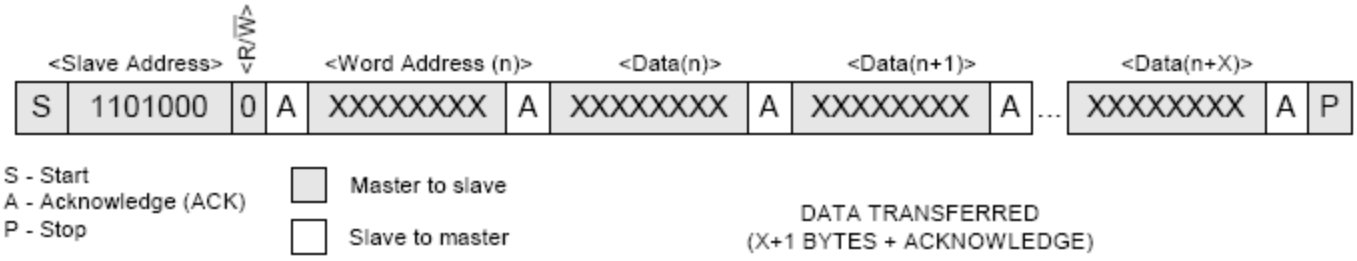
The IDT5P90005 can operate in the following two modes:

1) **Slave Receiver Mode (Write Mode):** Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (see the “Data Write–Slave Receiver Mode” figure). The slave address byte is the first byte received after the START condition is generated by the master. The slave address byte contains the 7-bit IDT5P90005 address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which is 0 for a write. After receiving and decoding the slave address byte the slave outputs an acknowledge on the SDA line. After the IDT5P90005 acknowledges the slave address + write bit, the master transmits a register address to the IDT5P90005. This sets the register pointer on the IDT5P90005, with the IDT5P90005 acknowledging the transfer. The master may then transmit zero or more bytes of data, with the IDT5P90005 acknowledging each byte received. The address pointer increments after each data byte is transferred. The master generates a STOP condition to terminate the data write.

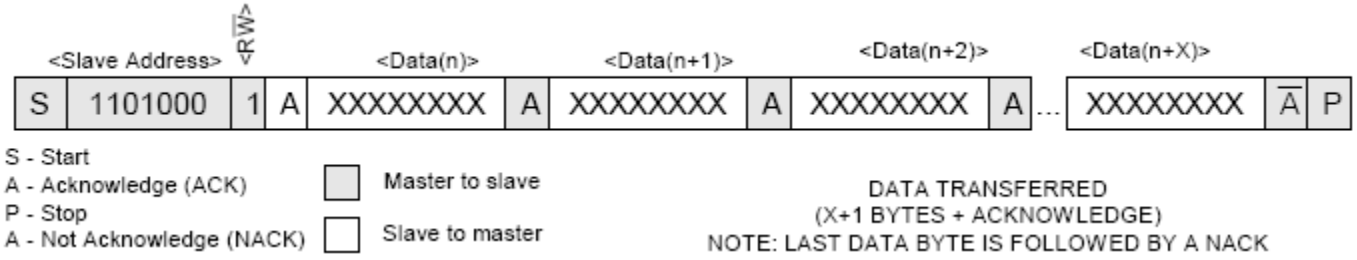
2) **Slave Transmitter Mode (Read Mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the IDT5P90005 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (see the “Data Read–Slave Transmitter Mode” figure). The slave address byte is the first byte received after the START condition is generated by the master. The slave address byte contains the 7-bit IDT5P90005 address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which is 1 for a read. After receiving and decoding the slave address byte the slave outputs an acknowledge on the SDA line. The IDT5P90005

then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The address pointer is incremented after each byte is transferred. The IDT5P90005 must receive a “not acknowledge” to end a read.

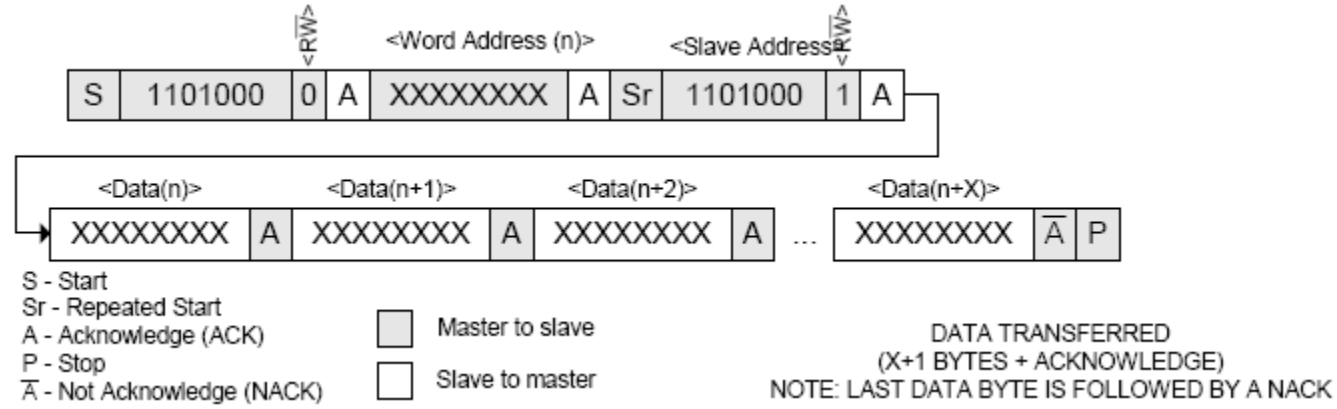
Data Write – Slave Receiver Mode



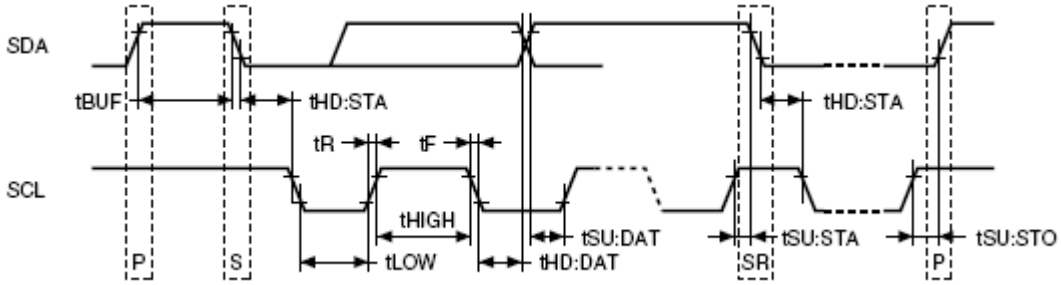
Data Read (from current Pointer location) – Slave Transmitter Mode



Data Read (Write Pointer, then Read) – Slave Receive and Transmit



Bus Timing Requirements Sequence



Note: P=STOP and S=START.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT5P90005. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Parameter	Condition	Min.	Typ.	Max.	Units
Supply Voltage, VCC	Referenced to GND	-0.3		7	V
Input or Output Voltages	Referenced to GND	-0.3		7	V
Clock Outputs	Referenced to GND	-0.5		VDD+ 0.5	V
Storage Temperature		-55		125	°C
Soldering Temperature[1]	Max 10 seconds			260	°C
Output Current				20	mA
Ambient Operating Temperature		-40		+85	°C
Power Dissipation				0.25	W

Note 1: Re flow at peak temperature of 260°C (total thermal budget not to exceed 245°C for greater than 30 seconds).

Caution: Negative undershoots below -0.3 V are not allowed on any pin while in the backup mode.

DC and AC Parameters

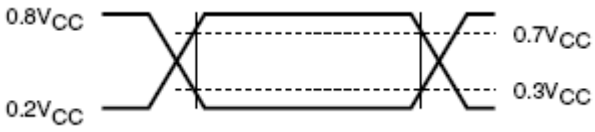
This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC characteristic tables are derived from tests performed under the measurement conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Operating and AC Measurement Conditions[1]

Parameter	Rating
Supply Voltage, VCC	2.0 to 5.5 V
Ambient Operating Temperature	-40 to +85ºC
Load Capacitance	100 pF
Input Rise and Fall times	≤ 5 ns
Input Pulse Voltages	0.2 VCC to 0.8 VCC
Input and Output TIming Reference Voltages	0.3 VCC to 0.7 VCC

Note 1: Output Hi-Z is defined as the point where data is no longer driven.

AC Testing Input/Output Waveform



Capacitance

Parameter[1,2]	Symbol	Min.	Typ.	Max.	Units
Input Capacitance	C_{IN}			7	pF
Output Capacitance (SDA, FT/OUT)	C_{OUT}[3]			10	pF
Low-pass Filter Input Time Constant (SDA and SCL)	t_{LP}	250		1000	ns

Note 1: Effective capacitance measured with power supply at 3.3 V; sampled only, not 100% tested.

Note 2: At 25°C, f = 1 MHz.

Note 3: Output deselected.

DC Characteristics

Parameter	Symbol	Conditions[1]	Min.	Typ.	Max.	Units
Input Leakage Current	I_{LI}	0V = VIN = VCC			±1	µA
Output Leakage Current	I_{LO}	0V = VOUT = VCC			±1	µA
Supply Current	I_{CC1}	Switch Frequency = 100 kHz			300	µA
RTC Supply Current (standby)	I_{CC2}	SCL, SDA = VCC - 0.3			70	µA
Input Low Voltage	V_{IL}		-0.3		0.3VCC	V
Input High Voltage	V_{IH}		0.7VCC		VCC+0.5	V
Output Low Voltage	V_{OL}	I_{OL} = 3.0 mA			0.4	V
Output Low Voltage (open drain)		FT/OUT			5.5	V
Battery Supply Voltage	V_{BAT}		2.5		3.5	V
Battery Supply Current	I_{BAT}	TA = 25°C, VCC = 0V Oscillator ON, V_{BAT} = 3 V		0.8	1	µA

Note 1: Valid for ambient operating temperature: TA = –40 to 85 °C; VCC = 2.0 to 5.5 V (except where noted).

Crystal Electrical Characteristics

Parameter[1]	Symbol	Min.	Typ.	Max.	Units
Resonant Frequency	f_O		32.768		kHz
Series Resistance	R_S			60	KΩ
Load Capacitance	C_L		12.5		pF

Note 1: Load capacitors are integrated within the IDT5P90005. Circuit board layout considerations for the 32.768 kHz crystal of minimum trace lengths and isolation from RF generating signals should be taken into account.

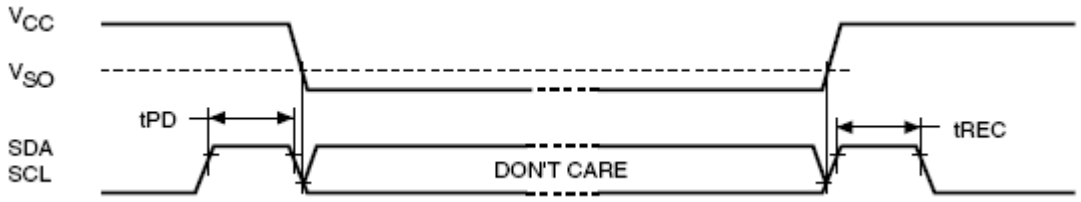
AC Electrical Characteristics

Unless stated otherwise, **VCC = 2.0 to 5.5 V**, Ambient Temperature -40 to +85°C

Parameter	Symbol	STANDARD MODE		FAST MODE		Units
		Min.	Max.	Min.	Max.	
SCL Clock Frequency	f_{SCL}		100		400	kHz
Clock Low Period	t_{LOW}	4.7		1.3		µs
Clock High Period	t_{HIGH}	4.0		0.6		µs
SDA and SCL Rise time	t_R		1		0.3	µs
SDA and SCL Fall Time	t_F		300		300	ns
START Condition Hold Time (after this period the first clock pulse is generated)	t_{HD}:STA	4				µs
START Condition Setup Time (only relevant for a repeated start condition)	t_{SU}:STA	4.7		0.6		µs
Data Hold Time	t_{HD}:DAT[1]	0		1.3		ns
Data Setup Time	t_{SU}:DAT	250		100		ns
STOP Condition Setup Time	t_{SU}:STO	4.0		0.6		µs
Time the bus must be free before a new transmission can start	t_{BUF}	4.7		1.3		µs

Note 1: Transmitter must internally provide a hold time to bridge the undefined region (300 ns max) of the falling edge of SCL.

Power Down/Up Mode AC Waveforms



RTC Power Down/Up AC Characteristics

Parameter[1,2]	Symbol	Min.	Typ.	Max.	Units
SCL and SDA at VIH before Power Down	t_{PD}	0			ns
SCL and SDA at VIH after Power Up	t_{rec}	10		2000	µs

Note 1: Valid for ambient operating temperature: TA = –40 to 85 °C; VCC = 2.0 to 5.5 V (except where noted).

Note 2: VCC fall time should not exceed 5 mV/µs.

RTC Power Down/Up Trip Points DC Characteristics

Parameter[1,2]	Symbol	Min.	Typ.	Max[3]	Units
Backup Switchover Voltage	V_{SO}[3]	V_{BAT}-0.90	V_{BAT}-0.50	V_{BAT}-0.30	V

Note 1: Valid for ambient operating temperature: TA = –40 to 85 °C; VCC = 2.0 to 5.5 V (except where noted).

Note 2: All voltages referenced to VSS.

Note 3: Switchover and deselect point.

Clock Operation

The eight byte clock register (see “Register Map” table) is used to both set the clock and to read the date and time from the clock, in a binary coded decimal format. Seconds, minutes, and hours are contained within the first three registers. Bits D6 and D7 of clock register 2 (century/hours register) contain the century enable bit (CEB) and the century bit (CB). Setting CEB to a '1' will cause CB to toggle, either from '0' to '1' or from '1' to '0' at the turn of the century (depending upon its initial state). If CEB is set to a '0', CB will not toggle. Bits D0 through D2 of register 3 contain the day (day of week). Registers 4, 5 and 6 contain the date (day of month), month and years. The final register is the control register (this is described in the clock calibration section). Bit D7 of register 0 contains the STOP bit (ST). Setting this bit to a '1' will cause the oscillator to stop. If the device is expected to spend a significant amount of time on the shelf, the oscillator may be stopped to reduce current drain. When reset to a '0' the oscillator restarts within one second.

When reading or writing the time and date registers, secondary(user) buffers are used to prevent error when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on any start or stop, and when the address pointer rolls over to zero. The countdown chain is reset whenever the seconds register is written. Write transfers occurs on the acknowledge pulse from the device. To avoid rollover issues, once the countdown chain is reset, the remaining time and date registers must be written within one second. If enabled, the 1Hz square-wave output transitions high 500ms after the seconds data transfer, provided the oscillator is already running.

Note: *In order to guarantee oscillator start-up after the initial power-up, set the ST bit to a '1,' then reset this bit to a '0.' This sequence enables a “kick start” circuit which aids the oscillator start-up during worst case conditions of voltage and temperature.*

Register Map[1]

Address	Data								Function/Range BCD Format	
	D7	D6	D5	D4	D3	D2	D1	D0		
0	ST	10 seconds			Seconds				Seconds	00 - 59
1	R	10 minutes			Minutes				Minutes	00 - 59
2	CEB[2]	CB	10 hours		Hours				Century/Hours	0-1/00-23

Address	Data								Function/Range BCD Format	
	D7	D6	D5	D4	D3	D2	D1	D0		
3	R	R	R	R	R	Day			Day	01 - 07
4	R	R	10 date		Date				Date	01 - 31
5	R	R	R	10 M	Month				Month/Century	01 - 12
6	10 years				Years				Year	00 - 99
7	OUT	FT	R	R	R	R	R	R	Control	

Note 1. Keys:

FT = frequency test bit
ST = stop bit
OUT = output level
CEB = century enable bit
CB = century bit

R = Reserved BIT(keep same as default value)

Note 2. When CEB is set to '1', CB will toggle from '0' to '1' or from '1' to '0' at the turn of the century (dependent upon the initial value set).When CEB is set to '0', CB will not toggle.

Output Driver Pin

When the FT bit is not set, the FT/OUT pin becomes an output driver that reflects the contents of D7 of the control register. In other words, when D6 of address 7 is a zero and D7 of address 7 is a zero and then the FT/OUT pin will be driven low.

Note: *The FT/OUT pin is open drain which requires an external pull-up resistor.*

Table

FT	OUT	FT/OUT
0	0	0
0	1	1
1	x	512Hz

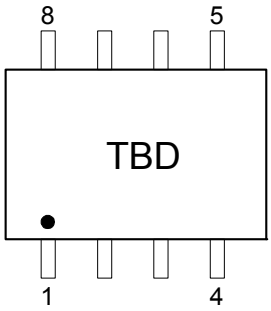
Initial Power-on Defaults

Upon initial application of power to the device, the FT bit will be set to a '0' and the OUT bit will be set to a '1'. All other register bits will initially power on in a random state.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W

Marking Diagram

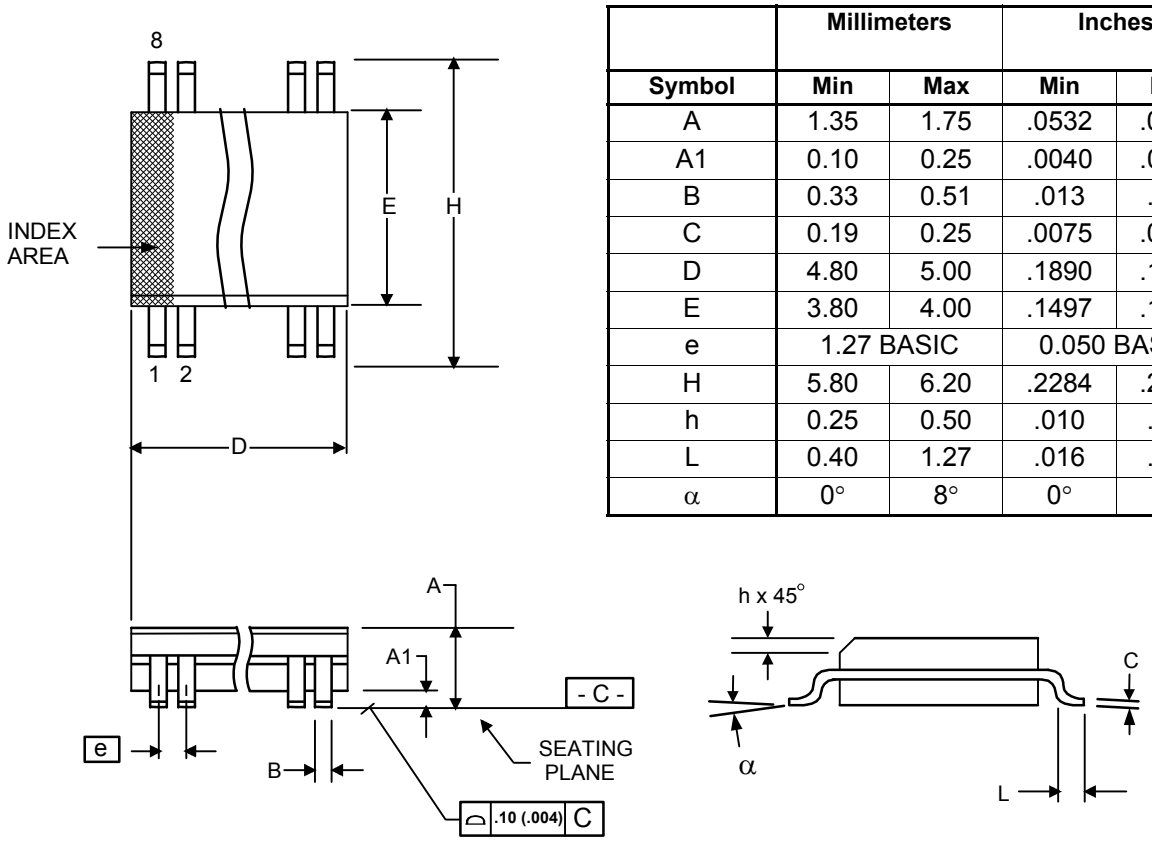


Notes:

1. ###### is the lot number.
2. YYWW is the last two digits of the year and week that the part was assembled.
3. Bottom marking: country of origin if not USA.

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
5P90005DCGI	see page 6	Tubes	8-pin SOIC	-40 to +85° C
5P90005DCGI8		Tape and Reel	8-pin SOIC	-40 to +85° C

Parts ordered with a "G" after the two-letter package code are the Pb-Free configuration and are RoHS compliant.

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