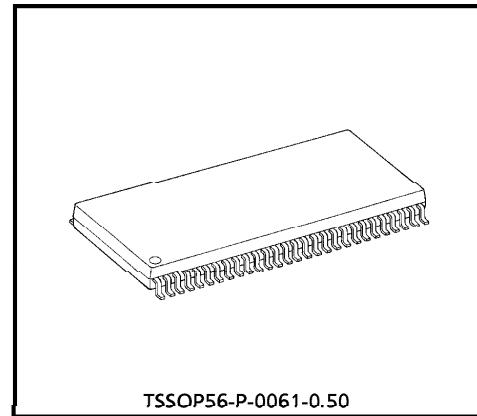


TC74VCX16646FT

LOW VOLTAGE 16-BIT BUS TRANSCEIVER / REGISTER
WITH 3.6V TOLERANT INPUTS AND OUTPUTS

The TC74VCX16646FT is a high performance CMOS 16-bit BUS TRANSCEIVER / REGISTER. Designed for use in 1.8, 2.5 or 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. It is also designed with over voltage tolerant inputs and outputs up to 3.6V.

This device is bus transceiver with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers. All inputs are equipped with protection circuits against static discharge.



Weight : 0.25g (Typ.)

FEATURES

- Low Voltage Operation : $V_{CC} = 1.8 \sim 3.6V$
- High Speed Operation : $t_{pd} = TBD$ (max.) at $V_{CC} = 3.0V$ (1.8V)
- : $t_{pd} = TBD$ (max.) at $V_{CC} = 2.3 \sim 2.7V$
- : $t_{pd} = TBD$ (max.) at $V_{CC} = 1.8V$
- 3.6V Tolerant inputs and outputs.
- Output Current : $I_{OH}/I_{OL} = \pm 24mA$ (min.) at $V_{CC} = 3.0V$
- : $I_{OH}/I_{OL} = \pm 18mA$ (min.) at $V_{CC} = 2.3V$
- : $I_{OH}/I_{OL} = \pm 6mA$ (min.) at $V_{CC} = 1.8V$
- Latch-up Performance : $\pm 300mA$
- ESD Performance : Human Body Model $> \pm 2000V$
- : Machine Model $> \pm 200V$
- Package : TSSOP (Thin Shrink Small Outline Package)
- Bidirectional interface between 2.5V and 3.3V signals.
- Power Down Protection is provided on all inputs and outputs

PRELIMINARY

Note 1) Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
2) All floating (high impedance) bus terminal must have their input level fixed by means of pull up or pull down resistors.

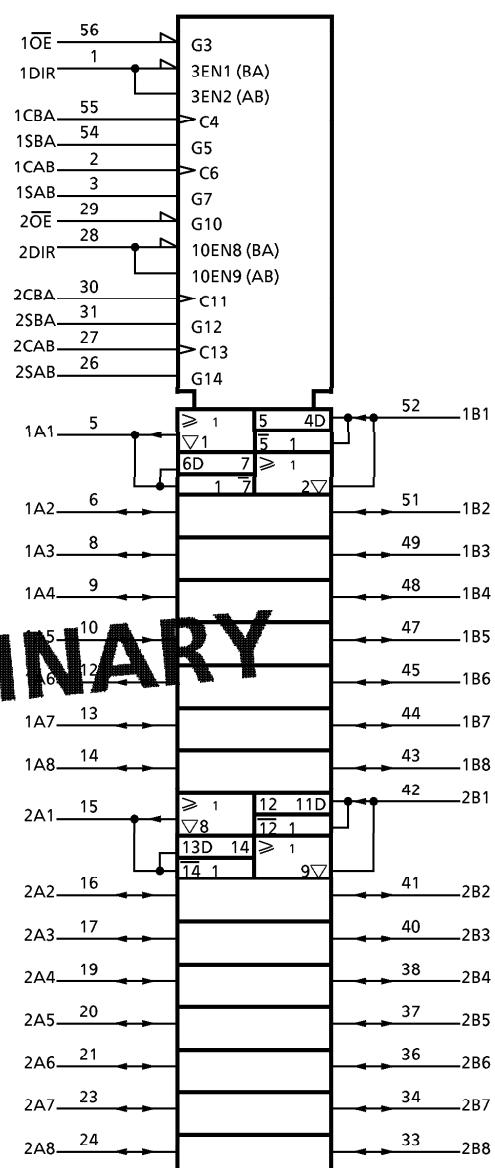
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PIN ASSIGNMENT

1DIR	1	56	1 \overline{OE}
1CAB	2	55	1CBA
1SAB	3	54	1SBA
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
V _{CC}	7	50	V _{CC}
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V _{CC}	22	35	V _{CC}
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2SAB	26	31	2SBA
2CAB	27	30	2CBA
2DIR	28	29	2 \overline{OE}

SYMBOL



(TOP VIEW)

TRUTH TABLE

CONTROL INPUTS						BUS		FUNCTION
\overline{OE}	DIR	CAB	CBA	SAB	SBA	A	B	
H	X	X*	X*	X	X	INPUT	INPUT	The output functions of A and B Busses are disabled.
		—	—	X	X	Z	Z	
L	H	X*	X*	L	X	INPUT	OUTPUT	Both A and B Busses are used as inputs to the internal flip-flops. Data on the Bus will be stored on the rising edge of the Clock.
		—	—	L	X	L	L	
		—	X*	L	X	H	H	The data on the A bus are displayed on the B bus.
		—	X*	L	X	L	L	
		—	X*	H	X	X	Qn	The data in the A storage flop-flops are displayed on the B Bus.
		—	X*	H	X	L	L	
L	L	X*	X*	X	X	OUTPUT	INPUT	The data on the B Bus are displayed on the A bus.
		X*	—	X	X	H	H	
		X*	—	X	L	L	L	The data on the B Bus are displayed on the A Bus, and are stored into the B storage flop-flops on the rising edge of CBA.
		X*	—	X	H	H	H	
PRELIMINARY								

X : Don't care

Z : High Impedance

Qn : The data stored into the internal flip-flops by most recent low to high transition of the clock inputs.

* The clocks are not internally with either \overline{OE} or DIR. Therefore, data on the A and / or B Busses may be clocked into the storage flip-flops at any time.

SYSTEM DIAGRAM

