SM843001-212

ClockWorks™ Fibre Channel, 212.5MHz, Ultra-Low Jitter LVPECL Clock Frequency Synthesizer

General Description

The SM843001-212 is a Fibre Channel, 212.5MHz LVPECL clock frequency synthesizer and a member of the ClockWorks™ family of devices from Micrel. It provides a low-noise timing solution for high-speed, high-accuracy synthesis of clock signals. It includes a patented RotaryWave® architecture that provides a stable clock with very low phase noise.

Power supplies of either 2.5V or 3.3V are supported, with superior jitter and phase noise performance. The device synthesizes a 212.5MHz, low-noise, LVPECL output for Fibre Channel applications. The crystal reference frequency used is 26.5625MHz.

The SM843001-212 is an excellent replacement for IDT FemtoClocks®, with improved waveform integrity, and jitter.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

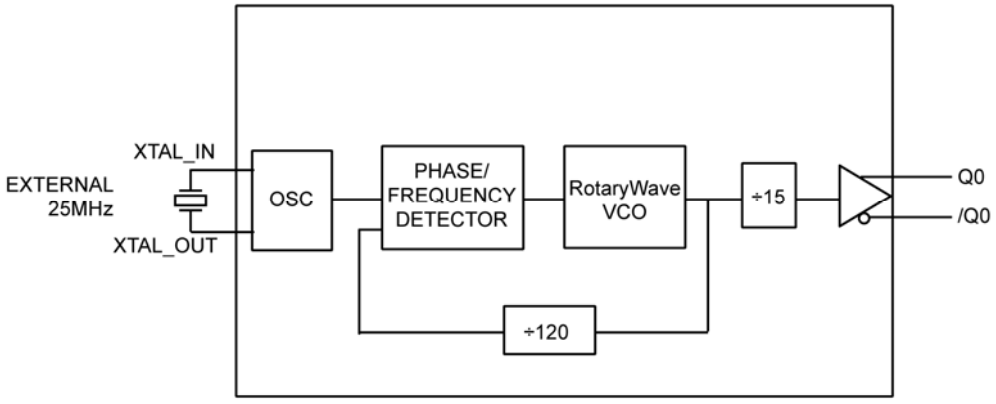
Features

- Generates a low jitter LVPECL output
- 2.5V or 3.3V operating voltage
- Typical phase jitter ~170fs (637kHz to 10MHz) @212.5MHz
- Crystal frequency: 26.5625MHz
- 212.5MHz output frequency
- RMS Phase Noise @ 212.5MHz:
  - 1kHz: –119dBc/Hz
  - 10kHz: –127dBc/Hz
  - 100kHz: –135dBc/Hz
  - 1MHz: –138dBc/Hz
  - 10MHz: –160dBc/Hz
  - 20MHz: –165dBc/Hz
- Industrial temperature range
- Green, RoHS-, and PFOS-compliant
- Available in 8-pin TSSOP

Applications

- Fibre Channel
- Storage Networking (SAN)

Block Diagram



ClockWorks is a trademark of Micrel, Inc.
RotaryWave is a registered trademark of Multigig, Inc.
FemtoClocks is a registered trademark of IDT, Inc.

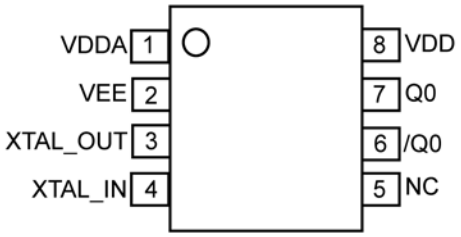
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking
SM843001-212KA	K-8	Industrial	843001-212
SM843001-212KA TR[2]	K-8	Industrial	843001-212

Notes:

1. Devices are Green, RoHS-compliant and PFOS-compliant.
2. Tape and Reel.

Pin Configuration



8-Pin TSSOP (K-8)

Pin Description

Pin Number	Pin Name	Type	Level	Pin Function
1	V_{DDA}	PWR		Analog 2.5V or 3.3V Power Supply. No filter resistor needed.
2	V_{EE}	PWR		Ground.
3	XTAL_OUT	O, (SE)	12pF crystal	Crystal Reference Output, no load caps needed.
4	XTAL_IN	I, (SE)	12pF crystal	Crystal Reference Input, no load caps needed.
5	NC	-		No Connect
6	/Q0	O, (DIF)	LVPECL	Differential Clock Output
7	Q0	O, (DIF)	LVPECL	Differential Clock Output
8	V_{DD}	PWR		2.5V or 3.3V Power Supply

Absolute Maximum Ratings[1]

Supply Voltage (V_{DDA}, V_{DD},) ..... +4.6V
Input Voltage (V_{IN}) ..... –0.50V to V_{DD}+0.5V
LVPECL Output Current (I_{OUT})
Continuous 50mA
Surge 100mA
Lead Temperature (soldering, 20sec.) ..... 260°C
Case Temperature ..... 115°C
Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{IN}) ..... +2.375V to +3.465V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Thermal Resistance
TSSOP (θ_{JA})(Still Air) ..... 141°C/W

DC Electrical Characteristics[3]

V_{DD} = V_{DDA} = 3.3V ±5%; T_A = –40°C to +85°C, unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{DD}	Core Supply Voltage		3.135	3.30	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.30	3.465	V
I_{DDA}	Analog Supply Current			48	60	mA
I_{EE}	Total Supply Current	No load		87	110	mA

V_{DD} = V_{DDA} = 2.5V ±5%; T_A = –40°C to +85°C, unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{DD}	Core Supply Voltage		2.375	2.50	2.625	V
V_{DDA}	Analog Supply Voltage		2.375	2.50	2.625	V
I_{DDA}	Analog Supply Current			48	60	mA
I_{EE}	Total Supply Current	No load		80	100	mA

LVPECL DC Electrical Characteristics[3][4]

V_{DD} = V_{DDA} = 2.5V ±5% or 3.3V ±5%, T_A = –40°C to +85°C, unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	50Ω to V_{DD} – 2V	V_{DD} – 1.145	V_{DD} – 0.97	V_{DD} – 0.845	V
V_{OL}	Output Low Voltage	50Ω to V_{DD}-2V	V_{DD} – 1.945	V_{DD} – 1.77	V_{DD} – 1.645	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6	0.8	1.0	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. The circuit is designed to meet the DC specifications shown in the above tables after thermal equilibrium has been established with a transverse airflow greater than 500 lfpm.
4. See Figure 4 for load test circuit example.

AC Electrical Characteristics[5]

V_{DD} = V_{DDA} = 2.5V ±5% or 3.3V ±5%, T_A = –40°C to +85°C, unless noted.

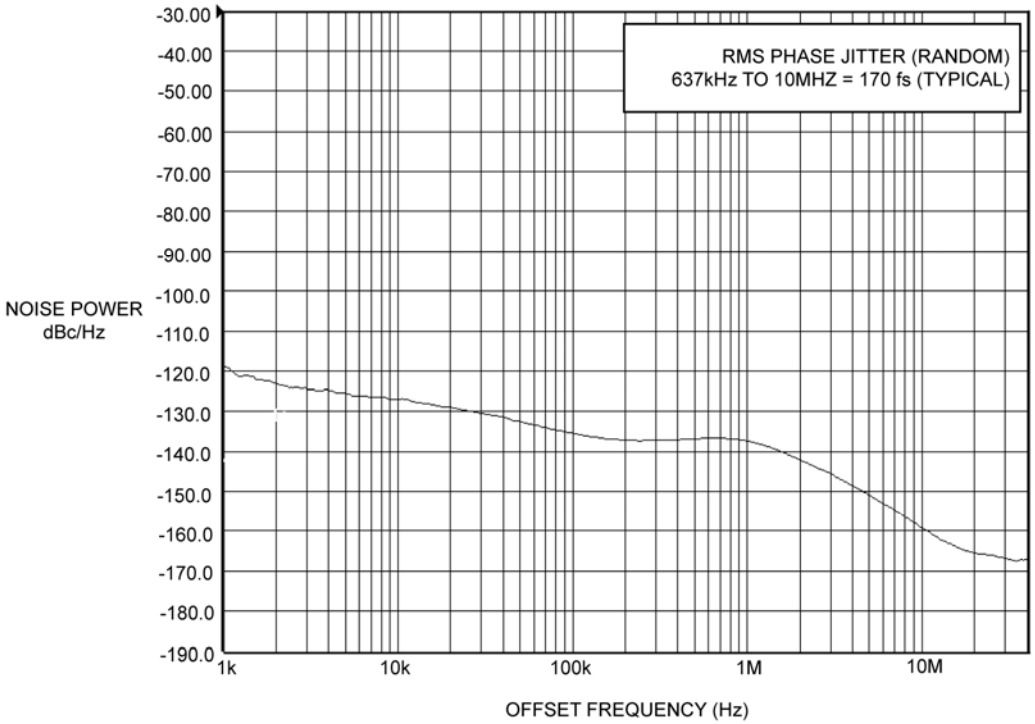
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
F_{OUT}	Output Frequency	26.5625MHz Crystal		212.5		MHz
t_{JITTER}	RMS Phase Jitter (Output = 212.5 MHz)	Integration Range: 637kHz to 10MHz		170		fs
t_R / t_F	Output rise/fall time	20% to 80%	80	150	350	ps
O_{DC}	Output Duty Cycle		48	50	52	%

Note:

5. The circuit is designed to meet the AC specifications shown in the above table(s) after thermal equilibrium has been established with a transverse airflow greater than 500 lfpm.

Crystal Characteristics

Parameter	Condition	Min.	Typ.	Max.	Units
Mode of Oscillation	12pF Load	Fundamental, Parallel Resonant			
Frequency			26.5625		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitor, C0			3	7	pF
Correlation Drive Level			100	300	uW



PHASE NOISE PLOT: 212.5MHz @ 3.3V

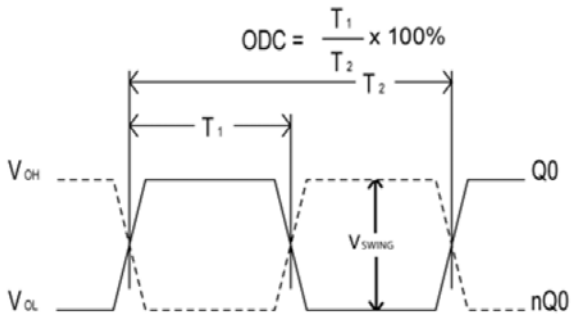


Figure 1. Duty Cycle Timing

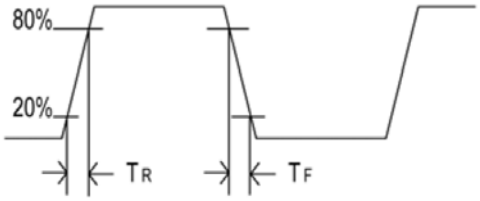


Figure 2. All Outputs Rise/Fall Time

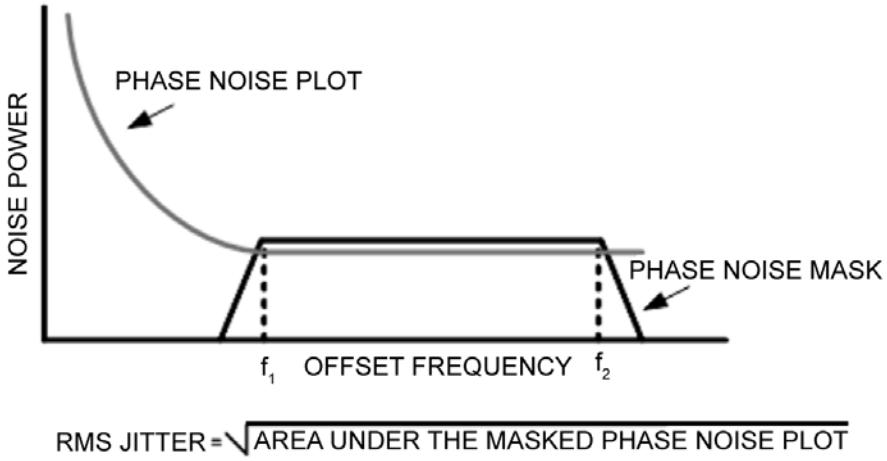


Figure 3. RMS Phase Noise/Jitter

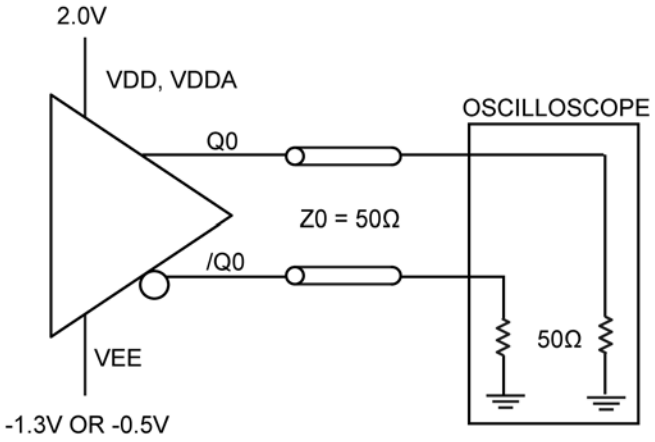


Figure 4. LVPECL Output Load and Test Circuit

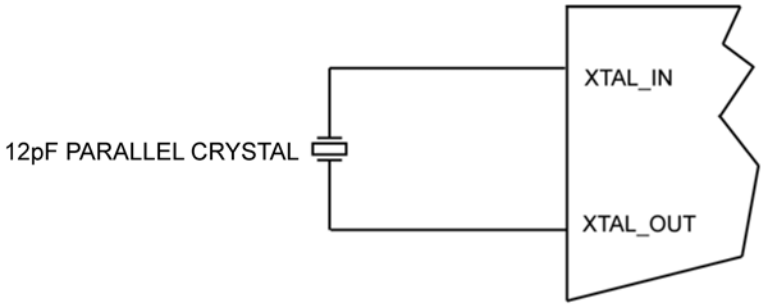
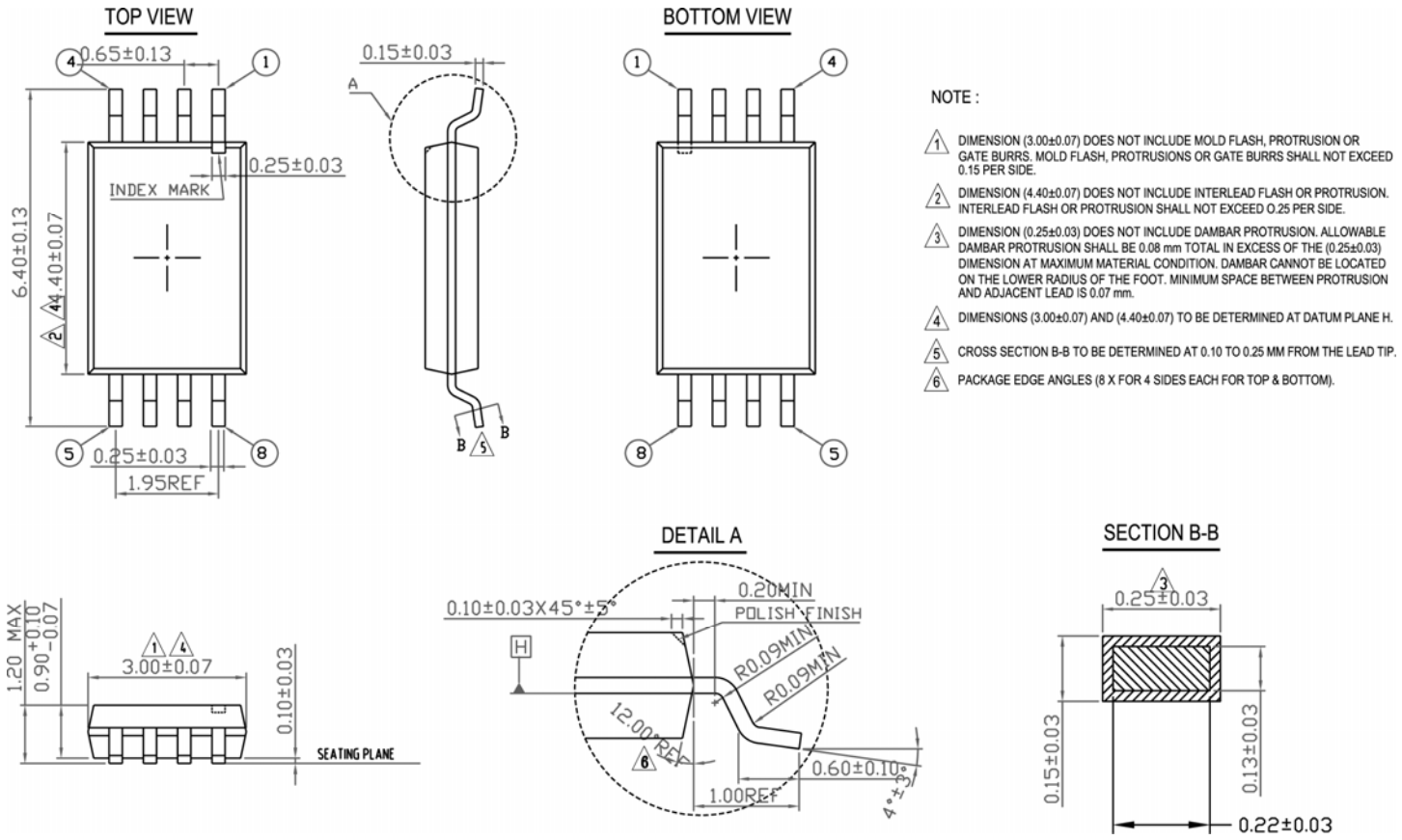


Figure 5. Crystal Input Interface

Package Information



8-Pin TSSOP (K-8)

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