

## Vishay High Power Products

# Phase Control Thyristors (Hockey PUK Version), 720 A



TO-200AB (E-PUK)

720 A

**PRODUCT SUMMARY** 

 $I_{T(AV)}$ 

#### **FEATURES**

- · Center amplifying gate
- · Metal case with ceramic insulator
- International standard case TO-200AB (E-PUK)



• Designed and qualified for industrial level





#### **TYPICAL APPLICATIONS**

- DC motor controls
- · Controlled DC power supplies
- · AC controllers

PARAMETER	TEST CONDITIONS	VALUES	UNITS	
1		720	А	
$I_{T(AV)}$	T <sub>hs</sub>	55	°C	
		1420	А	
I <sub>T(RMS)</sub>	T <sub>hs</sub>	25	°C	
I <sub>TSM</sub>	50 Hz	9000	Α	
	60 Hz	9420		
2t	50 Hz	405	- kA <sup>2</sup> s	
i-t	60 Hz	370		
V <sub>DRM</sub> /V <sub>RRM</sub>		400 to 1600	V	
tq	Typical	100	μѕ	
T <sub>J</sub>		- 40 to 125	°C	

#### **ELECTRICAL SPECIFICATIONS**

VOLTAGE RATINGS								
TYPE NUMBER	VOLTAGE CODE	V <sub>DRM</sub> /V <sub>RRM</sub> , MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	V <sub>RSM</sub> , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	$I_{DRM}/I_{RRM}$ MAXIMUM AT $T_J = T_J$ MAXIMUM mA				
	04	400	500					
	08	800	900					
ST330CC	12	1200	1300	50				
	14	1400	1500					
	16	1600	1700					

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# ST330CPbF Series

# Vishay High Power Products Phase Control Thyristors (Hockey PUK Version), 720 A



ABSOLUTE MAXIMUM RATIN	GS					
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum average on-state current	I	180° condu	180° conduction, half sine wave double side (single side) cooled		720 (350)	Α
at heatsink temperature	I <sub>T(AV)</sub>	double side			55 (75)	°C
Maximum RMS on-state current	I <sub>T(RMS)</sub>	DC at 25 °C	DC at 25 °C heatsink temperature double side cooled			
		t = 10 ms	No voltage		9000	A kA <sup>2</sup> s
Maximum peak, one-cycle		t = 8.3 ms	reapplied		9420	
non-repetitive surge current	I <sub>TSM</sub>	t = 10 ms	100 % V <sub>RRM</sub>		7570	
		t = 8.3 ms	reapplied	Sinusoidal half wave,	7920	
	l <sup>2</sup> t	t = 10 ms	No voltage reapplied	initial T <sub>J</sub> = T <sub>J</sub> maximum	405	
Maximum 12t for fusing		t = 8.3 ms			370	
Maximum I <sup>2</sup> t for fusing		t = 10 ms			287	
		t = 8.3 ms	reapplied		262	
Maximum I <sup>2</sup> √t for fusing	l²√t	t = 0.1 to 10 ms, no voltage reapplied			4050	kA²√s
Low level value of threshold voltage	V <sub>T(TO)1</sub>	(16.7 % x π	$(16.7 \% \text{ x } \pi \text{ x }  _{T(AV)} < I < \pi \text{ x }  _{T(AV)}), T_J = T_J \text{ maximum}$			V
High level value of threshold voltage	V <sub>T(TO)2</sub>	$(I > \pi \times I_{T(AV)}), T_J = T_J \text{ maximum}$			0.92	V
Low level value of on-state slope resistance	r <sub>t1</sub>	$(16.7 \% \text{ x } \pi \text{ x }  _{T(AV)} < I < \pi \text{ x }  _{T(AV)}), T_J = T_J \text{ maximum}$			0.58	<b>m</b> 0
High level value of on-state slope resistance	r <sub>t2</sub>	$(I > \pi \times I_{T(AV)}), T_J = T_J \text{ maximum}$			0.57	mΩ
Maximum on-state voltage	$V_{TM}$	$I_{pk} = 1810 \text{ A}, T_J = T_J \text{ maximum}, t_p = 10 \text{ ms sine pulse}$			1.96	V
Maximum holding current	I <sub>H</sub>	T _ 05 °C	anada aunnis 1	2 V registive lead	600	mA
Typical latching current	ΙL	T <sub>J</sub> = 25 °C, anode supply 12 V resistive load			1000	] '''A

SWITCHING						
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS		
Maximum non-repetitive rate of rise of turned-on current	dl/dt	Gate drive 20 V, 20 $\Omega$ , $t_r \le 1~\mu s$ $T_J = T_J$ maximum, anode voltage $\le 80~\%~V_{DRM}$	1000	A/µs		
Typical delay time	t <sub>d</sub>	Gate current 1 A, $dl_g/dt = 1$ A/ $\mu$ s $V_d = 0.67 \% V_{DRM}$ , $T_J = 25 \ ^{\circ}C$	1.0	110		
Typical turn-off time	t <sub>q</sub>	$I_{TM}$ = 550 A, $T_J$ = $T_J$ maximum, dl/dt = 40 A/μs, $V_R$ = 50 V, dV/dt = 20 V/μs, gate 0 V 100 $\Omega$ , $t_p$ = 500 μs	100	μs		

BLOCKING						
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS		
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum linear to 80 % rated $V_{DRM}$	500	V/µs		
Maximum peak reverse and off-state leakage current	I <sub>RRM</sub> , I <sub>DRM</sub>	$T_J = T_J$ maximum, rated $V_{DRM}/V_{RRM}$ applied	50	mA		

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# Phase Control Thyristors Vishay High Power Products (Hockey PUK Version), 720 A

TRIGGERING						
PARAMETER	SYMBOL	TEST COMPITIONS			UES	UNITS
PARAMETER	STIVIBUL	SYMBOL TEST CONDITIONS		TYP.	MAX.	UNITS
Maximum peak gate power	$P_{GM}$	$T_J = T_J$ maximum,	$t_p \leq 5 \text{ ms}$	10.0		W
Maximum average gate power	P <sub>G(AV)</sub>	$T_J = T_J$ maximum,	f = 50 Hz, d% = 50	2	.0	VV
Maximum peak positive gate current	I <sub>GM</sub>	$T_J = T_J$ maximum,	$t_p \leq 5 \; ms$	3	.0	Α
Maximum peak positive gate voltage	+ V <sub>GM</sub>			20		V
Maximum peak negative gate voltage	- V <sub>GM</sub>	$T_J = T_J$ maximum, $t_p \le 5$ ms			.0	]
		T <sub>J</sub> = - 40 °C	Maximum required gate trigger/current/voltage are the lowest	200	-	mA V
DC gate current required to trigger	I <sub>GT</sub>	T <sub>J</sub> = 25 °C		100	200	
		T <sub>J</sub> = 125 °C		50	-	
		T <sub>J</sub> = - 40 °C	value which will trigger all units	2.5	-	
DC gate voltage required to trigger	$V_{GT}$	T <sub>J</sub> = 25 °C	12 V anode to cathode applied	1.8	3.0	
		T <sub>J</sub> = 125 °C		1.1	-	
DC gate current not to trigger	I <sub>GD</sub>	T」= T」maximum	Maximum gate current/voltage not to trigger is the maximum value which will not trigger any	1	0	mA
DC gate voltage not to trigger	V <sub>GD</sub>	ij= ijillaxiillulli	unit with rated V <sub>DRM</sub> anode to cathode applied	0.25		٧

THERMAL AND MECHANICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS	
Maximum operating junction temperature range	TJ		- 40 to 125	°C	
Maximum storage temperature range	T <sub>Stg</sub>		- 40 to 150		
Maximum thormal registeres junction to heataink	D	DC operation single side cooled	0.09	K/W	
Maximum thermal resistance, junction to heatsink	R <sub>thJ-hs</sub>	DC operation double side cooled	0.04		
Maximum thermal resistance, case to heatsink	R <sub>thC-hs</sub>	DC operation single side cooled	0.02		
maximum thermal resistance, case to neatsink		DC operation double side cooled	0.01	] .	
Mounting force, ± 10 %			9800 (1000)	N (kg)	
Approximate weight			83	g	
Case style		See dimensions - link at the end of datasheet	TO-200AB (I	E-PUK)	

△R <sub>thJ-hs</sub> CONDUCTION							
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION		RECTANGULAR CONDUCTION		TEST CONDITIONS	UNITS	
CONDUCTION ANGLE	SINGLE SIDE	DOUBLE SIDE	SINGLE SIDE	DOUBLE SIDE	TEST CONDITIONS	UNITS	
180°	0.012	0.011	0.008	0.007	$T_J = T_J$ maximum		
120°	0.014	0.012	0.014	0.013			
90°	0.017	0.015	0.019	0.017		K/W	
60°	0.025	0.022	0.026	0.023			
30°	0.043	0.036	0.043	0.037			

#### Note

<sup>•</sup> The table above shows the increment of thermal resistance R<sub>thJ-hs</sub> when devices operate at different conduction angles than DC

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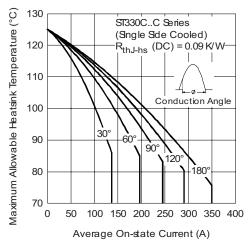


Fig. 1 - Current Ratings Characteristics

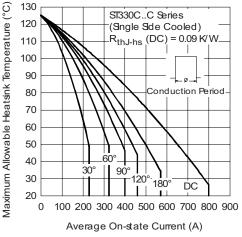


Fig. 2 - Current Ratings Characteristics

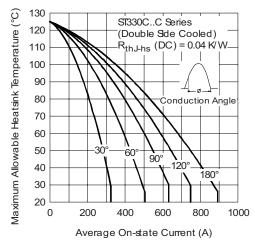


Fig. 3 - Current Ratings Characteristics

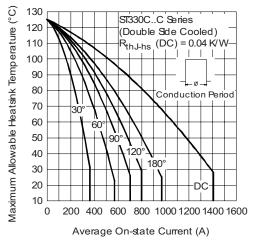


Fig. 4 - Current Ratings Characteristics

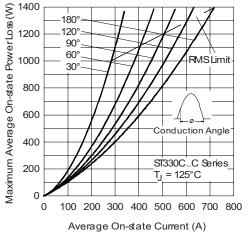


Fig. 5 - On-State Power Loss Characteristics

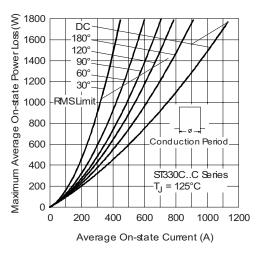


Fig. 6 - On-State Power Loss Characteristics



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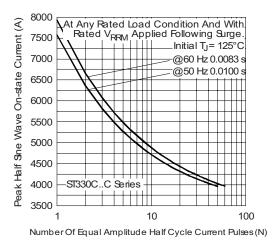


Fig. 7 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

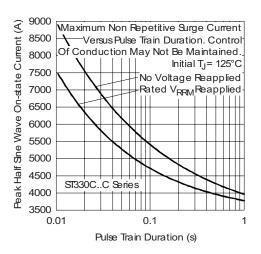


Fig. 8 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

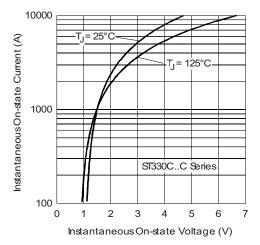


Fig. 9 - On-State Voltage Drop Characteristics

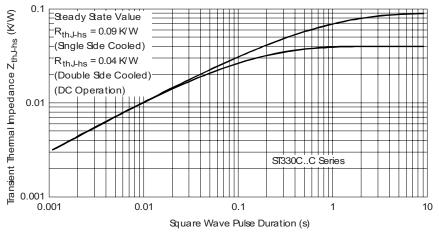


Fig. 10 - Thermal Impedance  $Z_{thJ\text{-}hs}$  Characteristics

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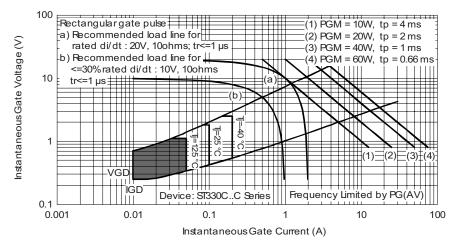
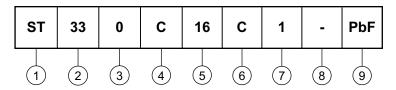


Fig. 11 - Gate Characteristics

Device code

**ORDERING INFORMATION TABLE** 



- 1 Thyristor
- 2 Essential part number
- <u>3</u> 0 = Converter grade
- 4 C = Ceramic PUK
- Voltage code x 100 = V<sub>RRM</sub> (see Voltage Ratings table)
- 6 C = PUK case TO-200AB (E-PUK)
- 7 0 = Eyelet terminals (gate and auxiliary cathode unsoldered leads)
  - 1 = Fast-on terminals (gate and auxiliary cathode unsoldered leads)
  - 2 = Eyelet terminals (gate and auxiliary cathode soldered leads)
  - 3 = Fast-on terminals (gate and auxiliary cathode soldered leads)
- 8 Critical dV/dt: None = 500 V/µs (standard selection)
  - L = 1000 V/µs (special selection)
- 9 Lead (Pb)-free

LINKS TO RELATED DOCUMENTS				
Dimensions	http://www.vishay.com/doc?95075			

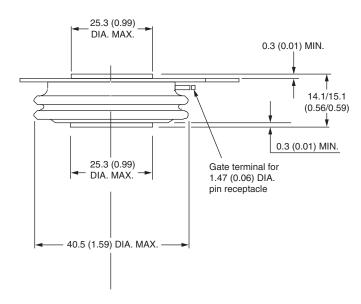
## Vishay Semiconductors

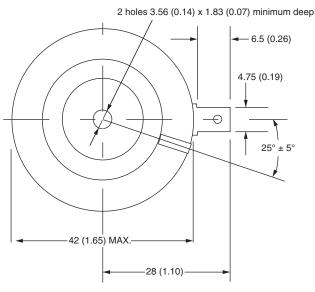
# **TO-200AB (E-PUK)**

#### **DIMENSIONS** in millimeters (inches)

Anode to gate

Creepage distance: 11.18 (0.44) minimum Strike distance: 7.62 (0.30) minimum





Quote between upper and lower pole pieces has to be considered after application of mounting force (see thermal and mechanical specification)



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