Introduction

DESCRIPTION

Microsemi's PD69104B Power over Ethernet (PoE) Manager enables network devices to share power and data over a single cable. The PD69104B PoE Manager chip is employed by both Ethernet switches and Midspans. The device integrates power, analog circuitry and state of the art control logic into a single 48-pin plastic QFN package.

The PD69104B device is a 4 port, mixed-signal, high-voltage PoE Manager. The PD69104B supports 3 modes of operation:

- MSCC Extended Auto mode – this is a stand-alone mode in which the PD69104B detects IEEE802.3af-2003 compliant PDs (Powered Devices) and IEEE802.3at-2009 High Power devices, ensuring safe power feeding and disconnection of ports based on a power management algorithm while employing a minimum of external components.
- Semi Auto mode – allows the host to control which devices are powered and which are not, as well as to communicate with the PD69104B and to configure it
- Auto mode – allows turning PDs on and off automatically. Used for systems with a full power supply.

The PD69104B executes all real time functions as specified in the IEEE802.3af-2003 ("AF") and IEEE802.3at High Power ("AT") standards, including load detection, "AF" and "AT" classifications, and using Multiple Classification Attempts (MCA).

The PD69104B, supports detect legacy/pre-standard PD devices. It also provides PD real-time protection through the following mechanisms: overload, under-load, over-voltage, over-temperature, and short-circuit. The PD69104B supports supply voltages between 44V and 57V with no need for additional power supply sources and has a built-in thermal protection.

The PD69104B is a low power device that uses internal MOSFETs and external 0.36Ω sense resistors.

The PD69104B is available in 48 leads, 8 mm x 8 mm QFN package.

KEY FEATURES

- Supports IEEE802.3af and IEEE802.3at, including two-event classification
- MSCC Extended Auto, Semi Auto, and Auto modes
- Supports pre-standard PD detection
- Supports Cisco devices detection
- Single DC voltage input (44V to 57V)
- Wide temperature range: -10° to +85°C
- Low power dissipation (0.36Ω sense resistor)
- Drives independent 2-pair power port
- Supports Extended PoE Protocol and Register Map
- Includes 2 selectable communication modes (I2C and UART)
- Includes Reset command pin
- Continuous monitoring port and system data
- Parameter setting using input pins
- Parameters setting from external serial EEPROM device
- Built-in Dynamic Power Management and Emergency Power Management mechanisms with 4 x Power Supply Power Good pins
- Power soft start mechanism
- On-chip thermal protection
- On-chip continual thermal monitoring
- Voltage/current and temperature monitoring/protection
- Built-in 3.3V and 5V regulators
- Internal power on reset
- MSL1, RoHS compliant

IMPORTANT: For the most current data, consult MICROSEMI's website: http://www.microsemi.com

PACKAGE ORDER INFO

T_A (°C)	Plastic 48 pin QFN 8x8 mm RoHS Compliant / Pb-free, MSL1
-10 to +85	**PD69104BILQ**

Note: Available in Tape and Reel. Append the letters "TR" to the part number. (i.e PD69104BILQ-TR)

THERMAL DATA

THERMAL RESISTANCE-JUNCTION TO AMBIENT 25° C/W

THERMAL RESISTANCE-JUNCTION TO CASE 4° C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.

The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

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TYPICAL POWER DISSIPATION INFORMATION

R_{sense} Power Dissipation: 0.36Ω x I_{port}^2
R_{ds_ON} Power Dissipation: 0.3Ω x I_{port}^2
P_{port_AF} = 15.4W ==> Port Power Dissipation @ R_{sense} = 37mW (320mA)
Port Power Dissipation @ R_{ds_ON} = 31mW (320mA)
P_{port_AT} = 30W ==> Port Power Dissipation @ R_{sense} = 130mW (600mA)
Port Power Dissipation @ R_{ds_ON} = 108mW (600mA)

Using Internal 3.3V regulator

Typical PD69104B self power dissipation (including internal regulations) = 0.5W (50V)

Typical PD69104B @ 4 x Port AF application power dissipation = 0.5W + 4 x 31mW + 4 x 37mW = 0.77W

Typical PD69104B @ 4 x Port AT application power dissipation = 0.5W + 4 x 108mW + 4 x 130mW = 1.45W

Using External 3.3V regulator

Typical PD69104B self power dissipation (external 3.3V source) = 0.25W (50V)

Typical PD69104B @ 4 x Port AF application power dissipation = 0.25W + 4 x 31mW + 4 x 37mW = 0.52W

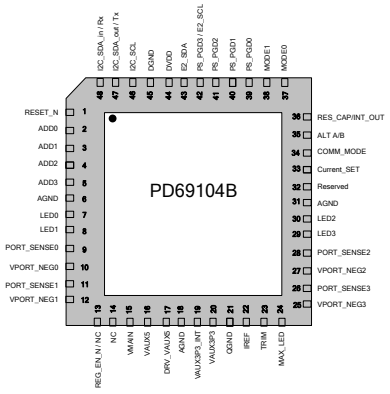
Typical PD69104B @ 4 x Port AT application power dissipation = 0.25W + 4 x 108mW + 4 x 130mW = 1.2W

ABSOLUTE MAXIMUM RATINGS

Supply Input Voltage (V_{MAIN})	-0.3V_{DC} to 74V_{DC}
Port_Neg[0..7] pins	-0.3V_{DC} to 74V_{DC}
LED pins	-0.3V_{DC} to 74V_{DC}
Port_Sense[0..7] pins	-0.3V_{DC} to 3.6V_{DC}
QGND, GND pins	-0.3V_{DC} to 0.3V_{DC}
VAUX5, DRV_VAUX5	-0.3V_{DC} to 5.5V_{DC}
All other pins	-0.3V_{DC} to 3.6V_{DC}
Operating Ambient Temperature Range	-10° to +85°C
Maximum Operating Junction Temperature	+160°C
ESD Protection at all I/O pins	± 2KV HBM
Storage Temperature Range	-65° to +150°C

Notes:
1. Exceeding these ratings can cause damage to the device. All voltages are with respect to ground. Currents are marked positive when flowing into specified terminals and marked negative when flowing out of specified terminals.

PACKAGE PIN OUT



(Top View)

RoHS / Pb-free 100% Matte Tin Finish

Electrical Characteristics

Unless otherwise specified, the following specifications apply to the operating ambient temperature, -10° to +85°C.

PARAMETER	SYMBOL	TEST CONDITIONS / COMMENT	PD69104B MANAGER MIN	PD69104B MANAGER TYP	PD69104B MANAGER MAX	UNITS
POWER SUPPLY						
Input Voltage	V_{MAIN}	Supports Full IEEE802.3 functionality	44	55	57	V_{DC}
Power Supply Current @ Operating Mode	I_{MAIN}	V_{MAIN} = 55V		10		mA
5V Output Voltage	V_{AUX5}		4.5	5	5.5	V_{DC}
3.3V Output Voltage	V_{AUX3P3}		2.97	3.3	3.63	V_{DC}
3.3V Output Current		Without external NPN			5	mA
		With external NPN transistor on VAUX5			30	mA
3.3V Input Voltage	V_{AUX3P3}	REG_EN_N pin = 3.3V (internal reg. is disabled) VAUX3P3_INT=5V	3	3.3	3.6	V_{DC}
POWER ON RESET (POR)						
Threshold			2.575	2.775	2.975	V_{DC}
Hysteresis			0.2	0.25	0.3	V_{DC}
Delay			10	50	100	µS
DIGITAL I/O						
Input Logic High Threshold	V_{IH}		2			V_{DC}
Input Logic Low Threshold	V_{IL}				0.8	V_{DC}
Input Hysteresis Voltage			0.4	0.6	0.8	V_{DC}
Input High Current	I_{IH}		-10		10	µA
Input Low Current	I_{IL}		-10		10	µA
Output High Voltage	V_{OH}	For I_{OH} = -1 mA	2.4			V_{DC}
Output Low Voltage	V_{OL}	I_{OH} = 1 mA			0.4	V_{DC}

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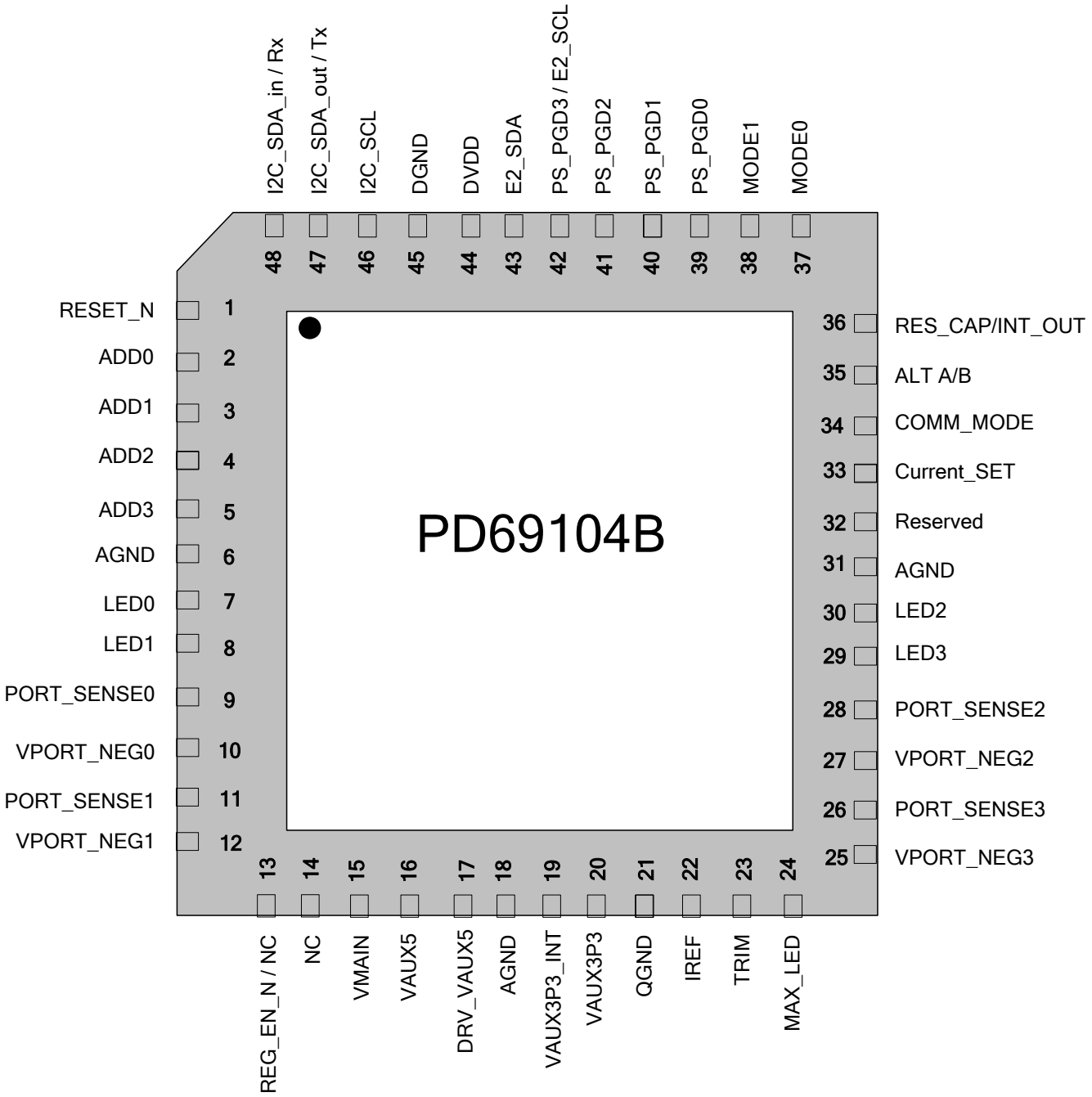
PARAMETER	SYMBOL	TEST CONDITIONS / COMMENT	PD69104B MANAGER MIN	PD69104B MANAGER TYP	PD69104B MANAGER MAX	UNITS
POE LOAD CURRENTS						
AT Limit Mode	AT_LIM_LOW	Tested With Sense resistance = 0.366 Ω (Rsense+Traces = 0.36 Ω+6mΩ=0.366 Ω) connected at port_sense pin	706	722	767	mA
	AT_LIM_HIGH		847	874	919	mA
	AT configurable		537		1200	mA
AF Limit Mode	AF_LIM		410	425	448	mA
PoE Tech High Power Port			808	850	892	mA
MAIN POWER SWITCHING FET						
On Resistance	R_{DSON}			0.3		Ω
Internal Thermal Protection Threshold				200		°C
LINE DETECTION						
Range		According to IEEE802.3 standard	19		26.5	KΩ
CLASSIFICATION						
Class Event Output Voltage		Measured between VMAIN and VPORT_NEG pins	16.5	18	19.5	V_{DC}
Mark Event Output Voltage		Measured between VMAIN and VPORT_NEG pins	7.5	8.5	9.5	V_{DC}
LED0 TO 3, POE_MAX DRIVERS						
Current Sink	I sink (from VMAIN to AGND)			3	5	mA
3 STATES ANALOG INPUT PINS (CURRENT SET, COMM_MODE)						
High Level input voltage			80% V_{AUX3P3}			V_{DC}
Open		Not Connected	40% V_{AUX3P3}		60% V_{AUX3P3}	V_{DC}
Low level input voltage					20% V_{AUX3P3}	V_{DC}

Package and Pinout



Detailed Pinout Description

PIN	PIN NAME	PIN TYPE	DESCRIPTION
0.	PAD	Analog GND	Exposed PAD: Connect to analog ground. A decent ground plane should be deployed around this pin whenever possible (refer to PD69104B Layout Design Guidelines)
1.	RESET_N	Digital Input	Reset input – active low ('0' = reset)
2.	ADDR0	Digital Input	Address bus for setting the address of the chip. See Table 1.
3.	ADDR1	Digital Input	Address bus for setting the address of the chip. See Table 1.
4.	ADDR2	Digital Input	Address bus for setting the address of the chip. See Table 1.
5.	ADDR3	Digital Input	Address bus for setting the address of the chip. See Table 1.
6.	AGND	Power	Analog ground
7.	LED0	Analog output	Port 0 LED indication – active low ('0' = LED on) See Table 3
8.	LED1	Analog output	Port 1 LED indication – active low ('0' = LED on) See Table 3
9.	PORT_SENSE0	Analog Input	Sense resistor port input(Connected to 0.36 Ω, 1% resistor to QGND with ~12 mΩ trace for measurements accuracy).
10.	VPORT_NEG0	Analog I/O	Negative port output
11.	PORT_SENSE1	Analog Input	Sense resistor port input(Connected to 0.36 Ω, 1% resistor to QGND with ~12 mΩ trace for measurements accuracy).
12.	VPORT_NEG1	Analog I/O	Negative port output
13.	REG_EN_N	Analog I/O	An input pin that enables control of the $3.3V_{DC}$ internal regulator. Disables internal $3.3V_{DC}$ regulator in case external $3.3V_{DC}$ is used to supply the chip. If connected to GND – internal regulator is enabled. If connected to $3.3V_{DC}$ – internal regulator is disabled
14.	NC	Analog I/O	A test pin used only during production. Keep unconnected.
15.	VMAIN	Power	Supplies voltage for the internal analog circuitry. A 1µF (or higher) low ESR bypass capacitor, connected to AGND, should be placed as close as possible to this pin through low resistance traces.
16.	VAUX5	Power	Regulated $5V_{DC}$ output voltage source, needs to be connected to a filtering capacitor of 4.7µF or higher. If an external NPN is used to regulate the voltage, connect this pin to the "Emitter" (the "collector" should be connected to VMAIN).
17.	DRV_VAUX5	Power	Driven outputs for $5V_{DC}$ external regulations. In case internal regulation is used, connect to pin 16. In case an external NPN is used to regulate the voltage, connect this pin to the "Base".
18.	AGND	Power	Analog ground
19.	VAUX3P3_INT	Power	In case internal 3.3 V_{DC} regulator is used, connected to VAX3P3 (pin 20). In case external $3.3V_{DC}$ regulator is used, connect to VAUX5 (pin 16).

20.	VAUX3P3	Power	Regulated 3.3V_{DC} output voltage source. A 4.7µF or higher filtering capacitor should be connected between this pin and AGND. When an external 3.3V_{DC} regulator is used, connect it to this pin to supply the chip.
21.	QGND	Power	Quiet analog ground
22.	IREF	Analog Input	A reference resistor pin. A 30.1kΩ, 1% resistor should be connected between this pin and QGND.
23.	TRIM	Test Input	Trimming input for IC production. Should be connected to VAUX3P3.
24.	MAX_LED	Analog output	MAX LED analog output. Indicates the device has exceeded maximum power budget. See Table 3.
25.	VPORT_NEG3	Analog I/O	Negative port output
26.	PORT_SENSE3	Analog Input	Sense resistor port input(Connected to 0.36 Ω, 1% resistor to QGND with ~12 mΩ trace for measurements accuracy).
27.	VPORT_NEG2	Analog I/O	Negative port output
28.	PORT_SENSE2	Analog Input	Sense resistor port input(Connected to 0.36 Ω, 1% resistor to QGND with ~12 mΩ trace for measurements accuracy).
29.	LED3	Analog output	Port 3 LED indication – active low ('0' = LED on) See Table 3
30.	LED2	Analog output	Port 2 LED indication – active low ('0' = LED on) See Table 3
31.	AGND	Power	Analog ground
32.	Reserved	Analog Input	Reserved pin. Must be connected to AGND.
33.	Current_SET	Analog Input	3 state input pin, used for selecting output current and AF/AT mode. • "0" (AGND) – AF mode • "open" (N.C) – Low AT mode 600mA • "1" (V_{DD}) – High AT mode 720mA
34.	COMM_MODE	Analog Input	3 state input pin communication. Following options are available: • "0" (AGND) – UART active • "open" (N.C) – E2PROM connected • "1" (V_{DD}) – I2C active
35.	ALT A/B	Digital Input	Configuration Input Pin, used for setting PD69104B working mode. • GND – ALT B mode = Midspan mode (midsp [0:3] bits ="1") • DVDD – ALT A mode = Endspan mode (midsp [0:3] bits ="0")

36.	RES_CAP / INT_OUT	Digital I/O	In MSCC Extended Auto mode: User input pin. Used for setting the chip legacy detection mode: • "1" (V_{DD}) – IEEE802.3af compliant resistor detection only • "0" (GND) – AF / AT Detection and Legacy (non-standard) line detection In Auto or Semi-Auto modes: Interrupt out pin. Indicates an interruption event has occurred. An external 10K pull-up resistor should be connected between this pin and DVDD.
37.	Mode0	Digital Input	Used for IC operational mode selection – see Table 2.
38.	Mode1	Digital Input	Used for IC operational mode selection – See Table 2.
39.	PS_PGD0	Digital input	Power Supply Power Good 0; Power Budget Set pin – for Fast Power Control (See Table 4)
40.	PS_PGD1	Digital input	Power Supply Power Good 1; Power Budget Set pin – for Fast Power Control (See Table 4)
41.	PS_PGD2	Digital input	Power Supply Power Good 2; Power Budget Set pin – for Fast Power Control (See Table 4)
42.	PS_PGD3 / E2_SCL	Digital I/O (open drain)	Power Supply Power good 3; Power Budget Set Pin – for initial configuration (See Table 4) *Or (refer to COMM MODE PIN)* E2_SCL: I2C Clock Out to EEPROM When working with EPROM - An external 10K pull-up resistor should be connected between this pin and DVDD.
43.	E2 SDA	Digital I/O (open drain)	EEPROM I2C data I/O pin. Used for Power Up configuration in Stand Alone Auto-Mode systems. An external 10K pull-up resistor should be connected between this pin and DVDD.
44.	DVDD	Power	Digital 3.3V_{DC} power input
45.	DGND	Power	Digital GND
46.	I2C SCL	Digital Input	I2C bus, serial clock input. An external 10K pull-up resistor should be connected between this pin and DVDD.
47.	I2C_SDA_out / Tx	Digital I/O (open drain)	I2C bus, data output / UART Tx output An external 10K pull-up resistor should be connected between this pin and DVDD.
48.	I2C_SDA_in / Rx	Digital I/O (open drain)	I2C bus, data input / UART Rx input An external 10K pull-up resistor should be connected between this pin and DVDD.

Note:

- "0" = Connect to DGND
- "1" = Connect to DVDD

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Table 1: I2C and UART Address Selection Table

CONST BITS	ADDR3 SLAVE 1 BIT	ADDR2 SLAVE 0 BIT	ADDR1 ID1 BIT	ADDR0 ID0 BIT	I2C/ UART ADDRESS
0 1 0	0	0	0	0	0100000b
0 1 0	0	0	0	1	0100001b
0 1 0	0	0	1	0	0100010b
0 1 0	0	0	1	1	0100011b
0 1 0	0	1	0	0	0100100b
0 1 0	0	1	0	1	0100101b
0 1 0	0	1	1	0	0100110b
0 1 0	0	1	1	1	0100111b
0 1 0	1	0	0	0	0101000b
0 1 0	1	0	0	1	0101001b
0 1 0	1	0	1	0	0101010b
0 1 0	1	0	1	1	0101011b
0 1 0	1	1	0	0	0101100b
0 1 0	1	1	0	1	0101101b
0 1 0	1	1	1	0	0101110b
0 1 0	1	1	1	1	0101111b

Notes:

- Address 0000000b is the global address in Extended mode operation I2C/UART (MODE<1:0>='00')
- Address 0110000b is the global address in Auto mode and Semi Auto mode operations (MODE<1:0>='01' or '11')
- All the slaves respond to the global address
- Avoid global read transactions
- Address 0001100b is used for Extended POE address (Alert Response address) in Auto mode and Semi Auto mode operations
- When reading from this Alert Response address, only slaves that assert the Int_out pin will send bytes that consist of their own addresses

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Table 2: Mode of Operation

Mode 1	Mode 0	Mode	Comm. to the IC	Functionality	Remarks
0	0	MSCC Extended Auto Mode	I2C or UART (see COMM_MODE pin)	Fully autonomous operation without a need for Host Controller (MCU) This Mode Supports Extended Registers Map. Default Operation: With No Interrupt Function (Interrupt can be enabled by communication command)	I2C or UART Protocol to Host with extended register map and PM (Power Management) support
0	1	Semi Auto mode	I2C or UART (see COMM_MODE pin)	Host should manage the ports	I2C Protocol to Host
1	0	Test mode			For internal use only
1	1	Auto mode	I2C or UART (see COMM_MODE pin)	Fully autonomous operation without a need for Host Controller. Default Operation: Interrupt Out Function – Enabled (Supported)	I2C Protocol to Host

Table 3: LED Indications

PIN	Status	LED
LED<3:0>	Port Power On	On
	Power Management event	0.4Hz Blink
	Port Over Load Port Short Circuit Port failed at Startup	0.8Hz Blink
	Vmain_Out of Range or Over Temp	All LEDs :3.3Hz Blink
	Port Off	Off
MAX_LED	Total power consumption is below Power Guard Band determined by the user	Off
	Total power consumption is above Power Guard Band but below total budget.	On
	Total power consumption is above total budget, or Power Integral is still positive	Blink

Notes:

MAX_LED:

- Both Max Power Budget and Max LED Guard Band (GB) can be configured through internal registers :
  - Max Power Budget registers: PWR_BNK0 to PWR_BNK7 (address 0x89 to 0x90)
  - Max LED Guard Band register: PoE_MAX_LED_GB (address 0x9F)
- PoE_MAX_LED_GB Register LSB = 1 watt
- Max LED reflects total power for all 4 ports
- When Total Power consumption < (Max Power - Guard Band) Max LED is OFF (below the bottom line)
- When Total Power consumption > (Max Power - Guard Band) Max LED is ON (Between the lines)

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- When Total Power consumption > (Max Power) => LED is BLINKING (above top line)
- Also, when Total Power > Budget (above top line):
  - An internal Digital Power Integration Calc. machine starts integrating power
  - When this Integrated total power is larger than Budget + 12.5% (RED LINE) => lowest priority port is turned OFF
  - This specific port LED is OFF
  - Max LED will reflect the NEW Total Power status
  - If ports turn off due to PM their per port LEDs will blink (in PM frequency) and MAX_LED will turn off
  - Timing to shut down this port is proportional to the Over Power (above budget) but limited to max. of 2 sec. – see example:

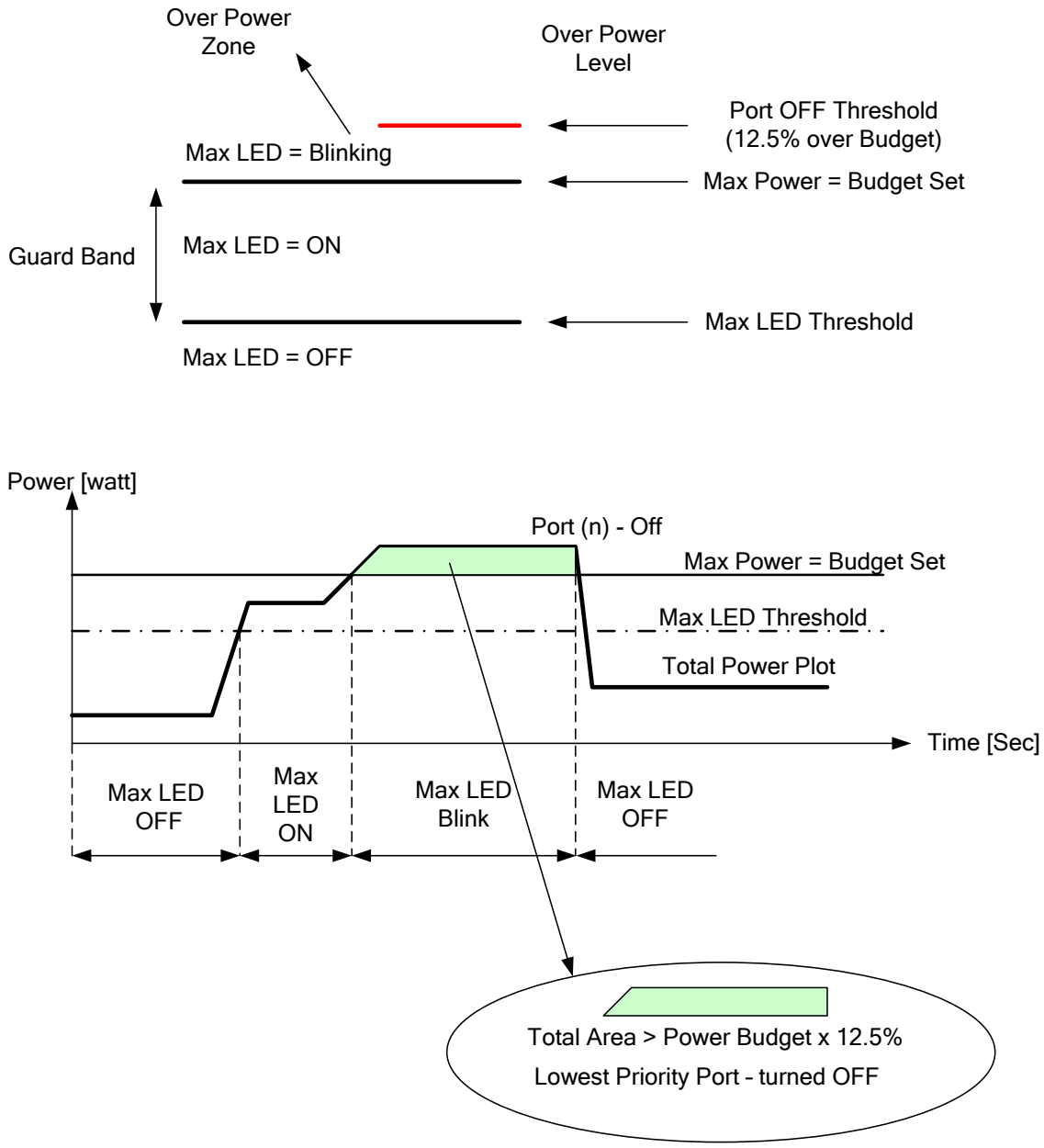

Figure 1: MAX_LED Behavior Description

- For Example:

- Budget = 100w, GB = 20w
- When total power = 70w – MAX LED is OFF
- When total power = 85w – MAX LED is ON (Power Integrator is NOT activated)
- When total power = 110w – MAX LED BLINKS (Power Integrator is activated) – Port at Lowest Priority is shut off
- Timing to shut off is based on : **delta(P) x T_{off} = Power Budget x 1.125**
- In this example **10watt x T_{off} = 100watt x 0.125** T_{off} = 1.25 sec.
- If Total Power = 105 watt delta (P) = 5 Then T_{off} = 2 sec. (which is the Max Timer)

Table 4: Power Budget:

PS_PG3 / Bank Range Select	PS_PG2	PS_PG1	PS_PG0	Total Power Budget [W]	Remarks
0	0	0	0	144 (default value in AT low mode) 176 (default value in AT high mode)	Register PWR_BNK0
0	0	0	1	140 (default value)	Register PWR_BNK1
0	0	1	0	136 (default value)	Register PWR_BNK2
0	0	1	1	132 (default value)	Register PWR_BNK3
0	1	0	0	128 (default value)	Register PWR_BNK4
0	1	0	1	124 (default value)	Register PWR_BNK5
0	1	1	0	120 (default value)	Register PWR_BNK6
0	1	1	1	116 (default value)	Register PWR_BNK7
1	0	0	0	112	Constant
1	0	0	1	108	Constant
1	0	1	0	104	Constant
1	0	1	1	100	Constant
1	1	0	0	96	Constant
1	1	0	1	92	Constant
1	1	1	0	88	Constant
1	1	1	1	84	Constant

- There are 16 power levels, whereas the first 8 levels are registers that can be configured by users.
- During operation a change in one of the PG pins will change PD69104B's total power budget and may result in turning off ports.
- The power level can be set either by PS_PG0 to PS_PG3 pins or by Host via communication.

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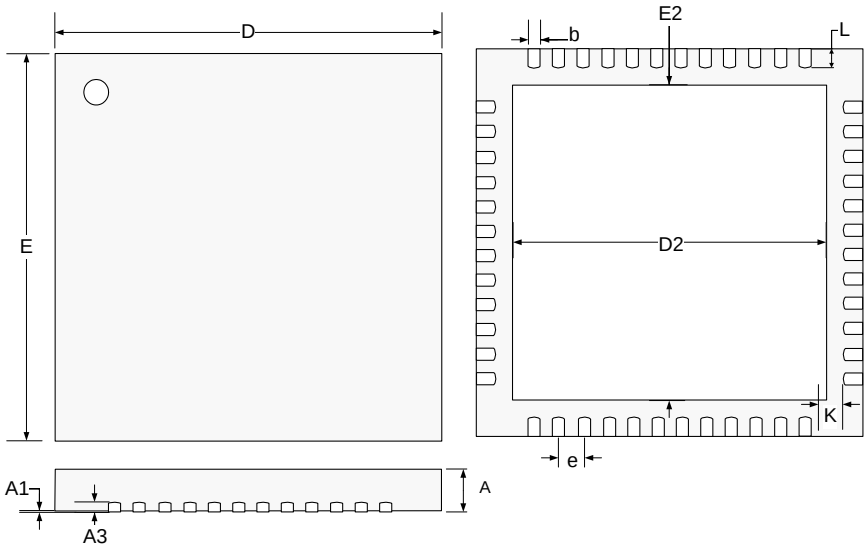
PACKAGE DRAWING



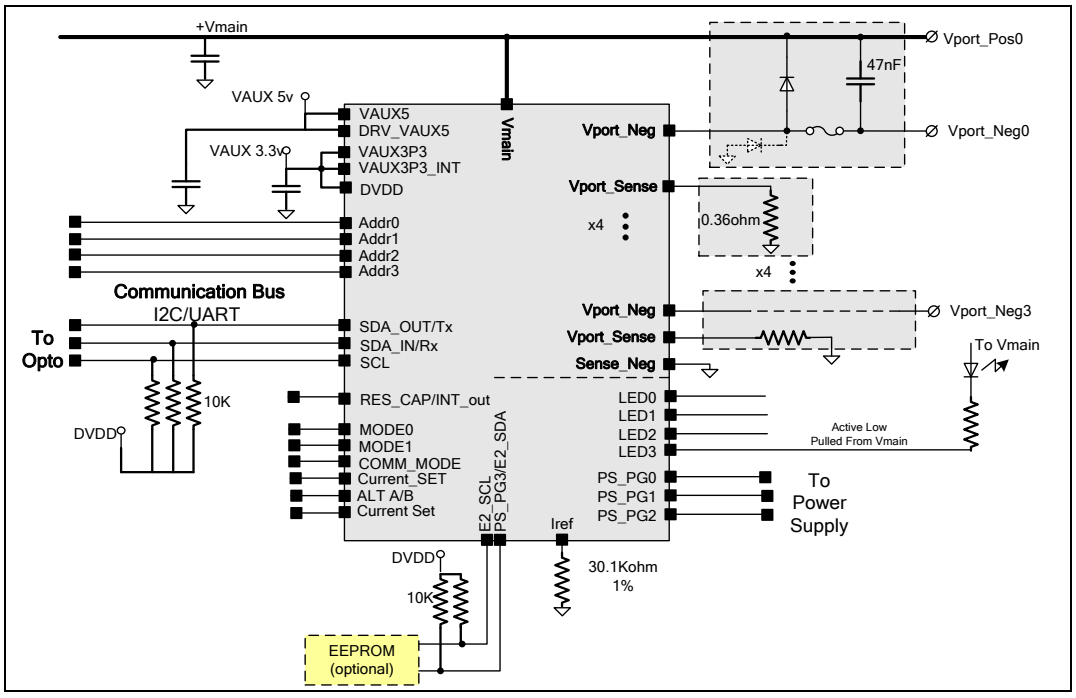
Dim	MILLIMETERS		INCHES	
	Min.	Max.	Min.	Max.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
A3	0.20 Ref.		0.008 Ref.	
K	0.20 Min.		0.008 Min.	
e	0.50 BSC		0.02 BSC	
L	0.30	0.50	0.012	0.02
b	0.18	0.30	0.007	0.012
D2	6.35	6.60	0.250	0.260
E2	6.35	6.60	0.250	0.260
D	8.00 BSC		0.315 BSC	
E	8.00 BSC		0.315 BSC	

Note:
1. Dimensions do not include protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.

TYPICAL APPLICATION

This typical application illustrates a simple “plug and play” Power over Ethernet solution for a single Ethernet port, switch or hub.

1. Plug the “POS” and “NEG” signals into the RJ45 switch jack.
2. Set the AF and AT operation modes through AF/AT and the current set pins (DGND or DVDD).



* For detailed schematics of application and layout recommendations contact sales_AMSG@microsemi.com.

PD69104B

Serial EEPROM Load Mechanism

The PD69104B is capable of loading its registers values from an external serial EEPROM during a boot slot time.

To utilize the EEPROM boot, the COMM_MODE pin must be set to E2PROM_MODE (not connected).

Features List:

- The PD69104B utilizes MASTER I2C communication.
- 7 bit addressing
- 250KHz frequency
- EEPROM constant address: 7'hA0
- EEPROM must support read byte and read after read.
- Two repeated transactions in case the EEPROM does not acknowledge the transaction
- A FIR filter for glitches cancelling

There are 5 consecutive read transaction (MASTER transactions) made by the PD69104B for reading data from the EEPROM and uploading it to the PD69104B registers.
The first transaction reads all registers from address 8'h70 to address 8'h9F.
The second transaction reads registers HPEN and HPMD1 (from addresses 8'h44 and 8'h46)
The third transaction reads register HPMD2 (from address 8'h4b)
The fourth transaction reads register HPMD3 (from address 8'h50)
The fifth transaction reads register `mp_hpmd4 (from address 8'h55)
The read transaction format is as follows:

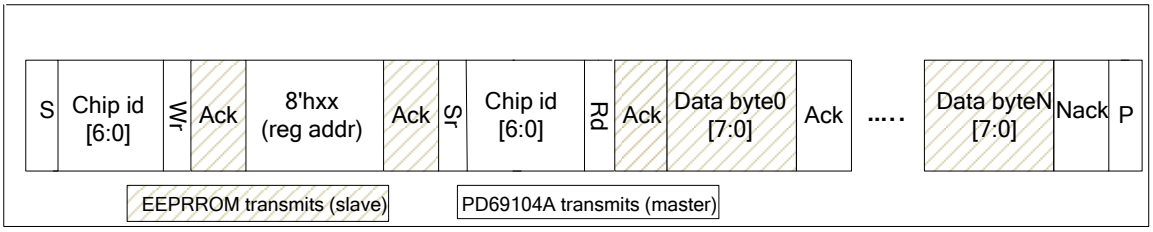


Figure 2: I2C EEPROM High Level Packet Structure.

For the I2C timing constraint, refer to **Error! Reference source not found.**

The EEPROM registers mapping should be identical to the PD69104B registers mapping.

Reset Mechanism

To reset the PD69104B, the RESET line should be pulled low for more than 16µs.

Revision History

Revision Level / Date	Para. Affected	Description
0.1 / June 2010		Preliminary Draft Release
0.2 / July 2010		Updated Pinout and Package to 7x7
0.3 / Aug 2010		Updated Pinout and Package to 8x8
0.4 / Aug 2010		Update Pinout Locations
0.5 / Sep 2010		Create generic version and customer specific version
0.6 / Oct 2010		Updates
1.0 / Oct 2011		Paging and Pinout Description TYPOs Fix
1.1 / Dec 2011		Paging and TYPOs Fix
1.2 / Dec 2011		Adding 3.3v Current
1.3 / Jan 2012		PS_PG Pins Name Change

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