GM71C(S)17403C/CL

4,194,304 WORDS x 4 BIT
CMOS DYNAMIC RAM

Description

The GM71C(S)17403C/CL is the new generation dynamic RAM organized 4,194,304 words x 4 bit. GM71C(S)17403C/CL has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The GM71C(S)17403C/CL offers Extended Data Out (EDO) Mode as a high speed access mode. Multiplexed address inputs permit the GM71C(S)17403C/CL to be packaged in a standard 300 mil 24(26) pin SOJ and a standard 300mil 24(26) pin plastic TSOP II. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply 5V+/-10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

Features

* 4,194,304 Words x 4 Bit Organization
* Extended Data Out Mode Capability
* Single Power Supply (5V+/-10%)
* Fast Access Time & Cycle Time

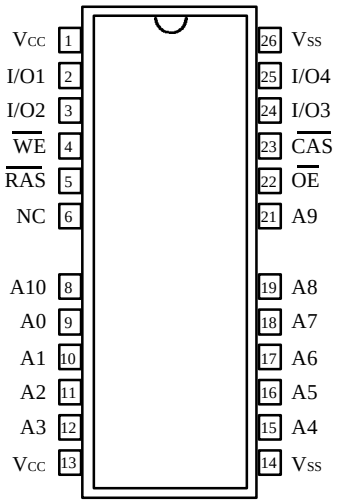
(Unit: ns)

	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
GM71C(S)17403C/CL-5	50	13	84	20
GM71C(S)17403C/CL-6	60	15	104	25
GM71C(S)17403C/CL-7	70	18	124	30

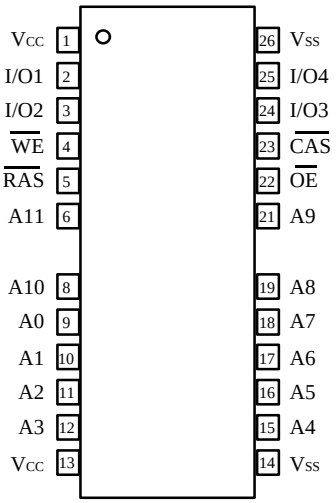
* Low Power
  Active : 660/605/550mW (MAX)
  Standby : 11mW (CMOS level : MAX)
  : 0.83mW (L-version : MAX)
* $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh Capability
* All inputs and outputs TTL Compatible
* 2048 Refresh Cycles/32ms
* 2048 Refresh Cycles/128ms (L-version)
* Battery Backup Operation (L-version)
* Test Function : 16bit parallel test mode

Pin Configuration

24(26) SOJ



24(26) TSOP II



(Top View)

Pin Description

Pin	Function	Pin	Function
A0-A10	Address Inputs	$\overline{WE}$	Read/Write Enable
A0-A10	Refresh Address Inputs	$\overline{OE}$	Output Enable
I/O1-I/O4	Data-input/Data-output	V_{CC}	Power (+5V)
$\overline{RAS}$	Row Address Strobe	V_{SS}	Ground
$\overline{CAS}$	Column Address Strobe	NC	No Connection

Ordering Information

Type No.	Access Time	Package
GM71C(S)17403CJ/CLJ-5 GM71C(S)17403CJ/CLJ-6 GM71C(S)17403CJ/CLJ-7	50ns 60ns 70ns	300 Mil 24(26) Pin Plastic SOJ
GM71C(S)17403CT/CLT-5 GM71C(S)17403CT/CLT-6 GM71C(S)17403CT/CLT-7	50ns 60ns 70ns	300 Mil 24(26) Pin Plastic TSOP II

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0 ~ 70	C
T_{STG}	Storage Temperature (Plastic)	-55 ~ 125	C
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	-1.0 ~ 7.0	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	-1.0 ~ 7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1.0	W

Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

Recommended DC Operating Conditions (T_A = 0 ~ 70C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	6.5	V
V_{IL}	Input Low Voltage	-1.0	-	0.8	V

DC Electrical Characteristics (V_{CC} = 5.0V+/-10%, V_{SS} = 0V, T_{OPR} = 0 ~ 70C)

Symbol	Parameter		Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = -2mA)		2.0	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 2mA)		0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling : t_{RC} = t_{RC} min)	50ns	-	120	mA	1, 2
		60ns	-	110		
		70ns	-	100		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{OUT} = High-Z)		-	2	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Refresh Mode (t_{RC} = t_{RC} min)	50ns	-	100	mA	2
		60ns	-	90		
		70ns	-	80		
I_{CC4}	EDO Page Mode Current Average Power Supply Current EDO Page Mode (t_{HPC} = t_{HPC} min)	50ns	-	90	mA	1, 3
		60ns	-	80		
		70ns	-	70		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ >= V_{CC} - 0.2V, D_{OUT} = High-Z)		-	1	mA	
			-	150	uA	5
I_{CC6}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	50ns	-	100	mA	
		60ns	-	90		
		70ns	-	80		
I_{CC7}	Battery Backup Operating Current(Standby with CBR Refresh) (CBR refresh, t_{RC} = 62.5us, t_{RAS} <= 0.3us, D_{OUT} = High-Z, CMOS interface)		-	350	uA	4,5
I_{CC8}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable		-	5	mA	1
$I_{L(I)}$	Input Leakage Current Any Input (0V<=V_{IN}<= 6V)		-10	10	uA	
$I_{L(O)}$	Output Leakage Current (D_{OUT} is Disabled, 0V<=V_{OUT}<= 6V)		-10	10	uA	

Note: 1. I_{CC} depends on output load condition when the device is selected.
I_{CC}(max) is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. $\overline{CAS}$ = L (<=0.2) while $\overline{RAS}$ = L (<=0.2).
5. L-version.

Capacitance (V_{CC} = 5V+/-10%, T_A = 25C)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (Address)	-	5	pF	1
C_{I2}	Input Capacitance (Clocks)	-	7	pF	1
$C_{I/O}$	Output Capacitance (Data-In/Out)	-	7	pF	1, 2

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

AC Characteristics (V_{CC} = 5V+/-10%, T_A = 0 ~ 70C, Notes 1, 2, 18, 19)

Test Conditions

Input rise and fall times: 2 ns
Input timing reference levels: 0.8V, 2.4V
Output timing reference levels: 0.8V, 2.0V
Output load : 1 TTL gate + C_L (100pF)
(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GM71C(S)17403 C/CL-5		GM71C(S)17403 C/CL-6		GM71C(S)17403 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	84	-	104	-	124	-	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	30	-	40	-	50	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	7	-	10	-	13	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	50	10,000	60	10,000	70	10,000	ns	21
t_{CAS}	$\overline{CAS}$ Pulse Width	7	10,000	10	10,000	13	10,000	ns	22
t_{ASR}	Row Address Set up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	7	-	10	-	10	-	ns	
t_{ASC}	Column Address Set-up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	7	-	10	-	13	-	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11	37	14	45	14	52	ns	3
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	9	25	12	30	12	35	ns	4
t_{RSH}	$\overline{RAS}$ Hold Time	10	-	13	-	13	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	35	-	40	-	45	-	ns	24
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	13	-	15	-	18	-	ns	5
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	0	-	0	-	0	-	ns	6
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	-	0	-	0	-	ns	6
t_T	Transition Time (Rise and Fall)	2	50	2	50	2	50	ns	7

Read Cycle

Symbol	Parameter	GM71C(S)17403C/CL-5		GM71C(S)17403C/CL-6		GM71C(S)17403C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	-	50	-	60	-	70	ns	8,9,19
t_{CAC}	Access Time from $\overline{CAS}$	-	13	-	15	-	18	ns	9,10,17,19
t_{AA}	Access Time from Address	-	25	-	30	-	35	ns	9,11,17,19
t_{OAC}	Access Time from $\overline{OE}$	-	13	-	15	-	18	ns	9
t_{RCS}	Read Command Setup Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	-	0	-	0	-	ns	12
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	-	5	-	5	-	ns	12
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	25	-	30	-	35	-	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	15	-	18	-	23	-	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	0	-	ns	
t_{OH}	Output Data Hold Time	3	-	3	-	3	-	ns	
t_{OHO}	Output Data Hold Time from $\overline{OE}$	3	-	3	-	3	-	ns	
t_{OFF}	Output Buffer Turn-off Time	-	13	-	15	-	15	ns	13
t_{OEZ}	Output Buffer Turn-off Time to $\overline{OE}$	-	13	-	15	-	15	ns	13,23
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	13	-	15	-	18	-	ns	5
t_{RCHR}	Read Command Hold Time from $\overline{RAS}$	50	-	60	-	70	-	ns	
t_{OHR}	Output Data hold Time from $\overline{RAS}$	3	-	3	-	3	-	ns	
t_{OFR}	Output Buffer turn off to $\overline{RAS}$	-	13	-	15	-	15	ns	13,23
t_{WEZ}	Output Buffer turn off to $\overline{WE}$	-	13	-	15	-	15	ns	13
t_{WDD}	$\overline{WE}$ to D_{IN} Delay Time	13	-	15	-	18	-	ns	
t_{RDD}	$\overline{RAS}$ to D_{IN} Delay Time	13	-	15	-	18	-	ns	

Write Cycle

Symbol	Parameter	GM71C(S)17403C/CL-5		GM71C(S)17403C/CL-6		GM71C(S)17403C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{WCS}	Write Command Setup Time	0	-	0	-	0	-	ns	14
t_{WCH}	Write Command Hold Time	7	-	10	-	13	-	ns	
t_{WP}	Write Command Pulse Width	7	-	10	-	10	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	7	-	10	-	13	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	7	-	10	-	13	-	ns	
t_{DS}	Data-in Setup Time	0	-	0	-	0	-	ns	15
t_{DH}	Data-in Hold Time	7	-	10	-	13	-	ns	15

Read- Modify-Write Cycle

Symbol	Parameter	GM71C(S)17403C/CL-5		GM71C(S)17403C/CL-6		GM71C(S)17403C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	111	-	136	-	161	-	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	67	-	79	-	92	-	ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	30	-	34	-	40	-	ns	14
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	42	-	49	-	57	-	ns	14
t_{OEH}	$\overline{OE}$ Hold Time from $\overline{WE}$	13	-	15	-	18	-	ns	

Refresh Cycle

Symbol	Parameter	GM71C(S)17403C/CL-5		GM71C(S)17403C/CL-6		GM71C(S)17403C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	5	-	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	7	-	10	-	10	-	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	0	-	0	-	0	-	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	-	10	-	10	-	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	5	-	5	-	5	-	ns	

EDO Page Mode Cycle

Symbol	Parameter	GM71C(S)17403 C/CL-5		GM71C(S)17403 C/CL-6		GM71C(S)17403 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{HPC}	EDO Page Mode Cycle Time	20	-	25	-	30	-	ns	20
t_{RASP}	EDO Page Mode $\overline{RAS}$ Pulse Width	-	100,000	-	100,000	-	100,000	ns	16
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	-	30	-	35	-	40	ns	9,17,19
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	30	-	35	-	40	-	ns	
t_{DOH}	Output data Hold Time from $\overline{CAS}$ low	3	-	3	-	3		ns	9
t_{COL}	$\overline{CAS}$ Hold Time referred $\overline{OE}$	7	-	10	-	13		ns	
t_{COP}	$\overline{CAS}$ to $\overline{OE}$ Setup Time	5	-	5	-	5		ns	
t_{RCHP}	Read command Hold Time from $\overline{CAS}$ Precharge	30	-	35	-	40		ns	

EDO Page Mode Read-Modify-Write Cycle

Symbol	Parameter	GM71C(S)17403 C/CL-5		GM71C(S)17403 C/CL-6		GM71C(S)17403 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{HPRWC}	EDO Page Mode Read-Modify-Write Cycle Time	57	-	68	-	79	-	ns	
t_{CPW}	$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	45	-	54	-	62	-	ns	14

Refresh

Symbol	Parameter	GM71C(S)17403 C/CL-5		GM71C(S)17403 C/CL-6		GM71C(S)17403 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{REF}	Refresh period	-	32	-	32	-	32	ms	2048 cycles
t_{REF}	Refresh period (L -Series)	-	128	-	128	-	128	ms	2048 cycles

Test Mode Cycle *19

Symbol	Parameter	GM71C(S)17403 C/CL-5		GM71C(S)17403 C/CL-6		GM71C(S)17403 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{WTS}	Test Mode $\overline{WE}$ Setup Time	0	-	0	-	0	-	ns	
t_{WTH}	Test Mode $\overline{WE}$ Hold Time	10	-	10	-	10	-	ns	

Notes:

1. AC Measurements assume t_T = 2ns.
2. An initial pause of 200us is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing RAS-only refresh or CAS-before-RAS refresh). If the internal refresh counter is used, a minimum of eight CAS-before-RAS refresh cycles are required.
3. Operation with the t_{RCD}(max) limit insures that t_{RAC}(max) can be met, t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD}(max) limit insures that t_{RAC}(max) can be met, t_{RAD}(max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.
5. Either t_{ODD} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.
7. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH}(min) and V_{IL}(max).
8. Assume that t_{RCD}<=t_{RCD}(max) and t_{RAD}<=t_{RAD}(max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. Measured with a load circuit equivalent to 1 TTL loads and 100pF.
10. Assume that t_{RCD}>=t_{RCD}(max) and t_{RAD}<=t_{RAD}(max).
11. Assume that t_{RCD}<=t_{RCD}(max) and t_{RAD}>=t_{RAD}(max).
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. t_{OFF}(max) and t_{OEZ}(max) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if t_{WCS}>=t_{WCS}(min), the cycles is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if t_{RWD}>=t_{RWD}(min), the t_{CWD}>=t_{CWD}(min), and t_{AWD}>=t_{AWD}(min), or t_{CWD}>=t_{CWD}(min), t_{AWD}>= t_{AWD}(min) and t_{CPW}>=t_{CPW}(min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{RASP} defines $\overline{RAS}$ pulse width in fast page mode cycles.
17. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}

18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device. After $\overline{RAS}$ is reset, if $t_{OEH} >= t_{CWL}$, the I/O pin will remain open circuit (high impedance); if $t_{OEH} <= t_{CWL}$, invalid data will be out at each I/O.

19. The 16M DRAM offers a 16-bit time saving parallel test mode. Address CA0 and CA1 for the 4M x 4 are don't care during test mode. Test mode is set by performing a $\overline{WE}$-and-$\overline{CAS}$-before-$\overline{RAS}$ (WCBR) cycle. In 16-bit parallel test mode, data is written into 4 bits in parallel at each I/O (I/O1 to I/O4) and read out from each I/O. If 4 bits of each I/O are equal (all 1s or 0s), data output pin is high state during test mode read cycle, then the device has passed. If they are not equal, data output pin is a low state, then the device has failed. Refresh during test mode operation can be performed by normal read cycles or by WCBR refresh cycles. To get out of test mode and enter a normal operation mode, perform either a regular $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle or $\overline{RAS}$-only refresh cycle.

20. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} and t_{ACP} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

21. $t_{RAS}(min) = t_{RWD}(min) + t_{RWL}(min) + t_T$ in Read - Modify - Write cycle.

22. $t_{CAS}(min) = t_{CWD}(min) + t_{CWL}(min) + t_T$ in Read - Modify - Write cycle.

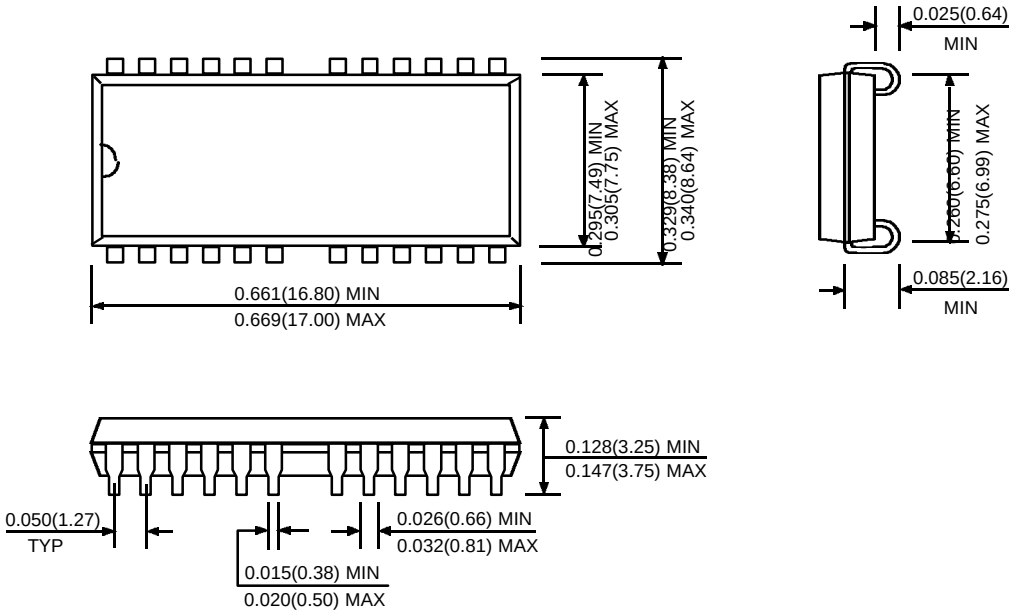
23. t_{OFF} and t_{OFR} are determined by the later rising edge of $\overline{RAS}$ or $\overline{CAS}$.

24. $t_{CSH}(min)$ can be achieved when $t_{RCD} <= t_{CSH}(min) - t_{CAS}(min)$.

Package Dimension

Unit: Inches (mm)

24(26) SOJ



24(26) TSOP (TYPE II)